

# TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

## Plastic Medium-Power Complementary Silicon Transistors

Designed for general-purpose amplifier and low-speed switching applications.

### Features

- High DC Current Gain –  
 $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Collector–Emitter Sustaining Voltage – @ 100 mAdc  
 $V_{CEO(sus)} = 60$  Vdc (Min) – TIP120, TIP125  
 $= 80$  Vdc (Min) – TIP121, TIP126  
 $= 100$  Vdc (Min) – TIP122, TIP127
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C = 3.0$  Adc  
 $= 4.0$  Vdc (Max) @  $I_C = 5.0$  Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- Pb–Free Packages are Available\*



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### DARLINGTON 5 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80–100 VOLTS, 65 WATTS



TO-220AB  
CASE 221A  
STYLE 1

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### MARKING DIAGRAM



TIP12x = Device Code  
x = 0, 1, 2, 5, 6, or 7  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb–Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

## MAXIMUM RATINGS

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	100	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current – Continuous – Peak	$I_C$	5.0 8.0			Adc
Base Current	$I_B$	120			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52			W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016			W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	50			mJ
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	–65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $I_C = 1\text{ A}$ ,  $L = 100\text{ mH}$ , P.R.F. = 10 Hz,  $V_{CC} = 20\text{ V}$ ,  $R_{BE} = 100\ \Omega$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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## OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 2) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	$V_{CEO(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	$I_{CEO}$	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ )	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	$I_{CBO}$	– – –	0.2 0.2 0.2	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	2.0	mAdc

## ON CHARACTERISTICS (Note 2)

DC Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )		$h_{FE}$	1000 1000	– –	–
Collector–Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 12\text{ mAdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $I_B = 20\text{ mAdc}$ )		$V_{CE(sat)}$	– –	2.0 4.0	Vdc
Base–Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )		$V_{BE(on)}$	–	2.5	Vdc

## DYNAMIC CHARACTERISTICS

Small–Signal Current Gain ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )		$h_{fe}$	4.0	–	–
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )	TIP125, TIP126, TIP127 TIP120, TIP121, TIP122	$C_{ob}$	– –	300 200	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$

# TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)



Figure 1. Darlington Circuit Schematic

## ORDERING INFORMATION

Device	Package	Shipping
TIP120	TO-220	50 Units / Rail
TIP120G	TO-220 (Pb-Free)	50 Units / Rail
TIP121	TO-220	50 Units / Rail
TIP121G	TO-220 (Pb-Free)	50 Units / Rail
TIP122	TO-220	50 Units / Rail
TIP122G	TO-220 (Pb-Free)	50 Units / Rail
TIP125	TO-220	50 Units / Rail
TIP125G	TO-220 (Pb-Free)	50 Units / Rail
TIP126	TO-220	50 Units / Rail
TIP126G	TO-220 (Pb-Free)	50 Units / Rail
TIP127	TO-220	50 Units / Rail
TIP127G	TO-220 (Pb-Free)	50 Units / Rail



Figure 2. Power Derating

# TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

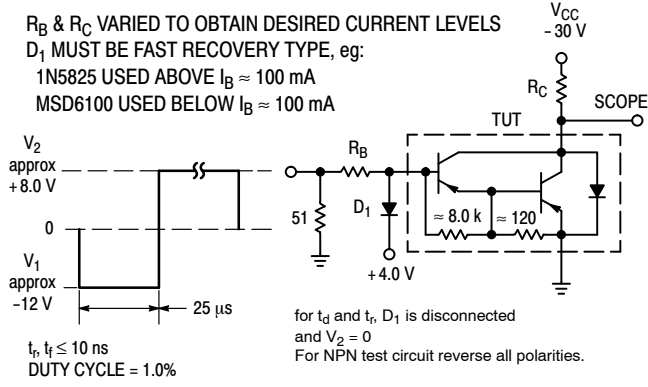


Figure 3. Switching Times Test Circuit



Figure 4. Switching Times

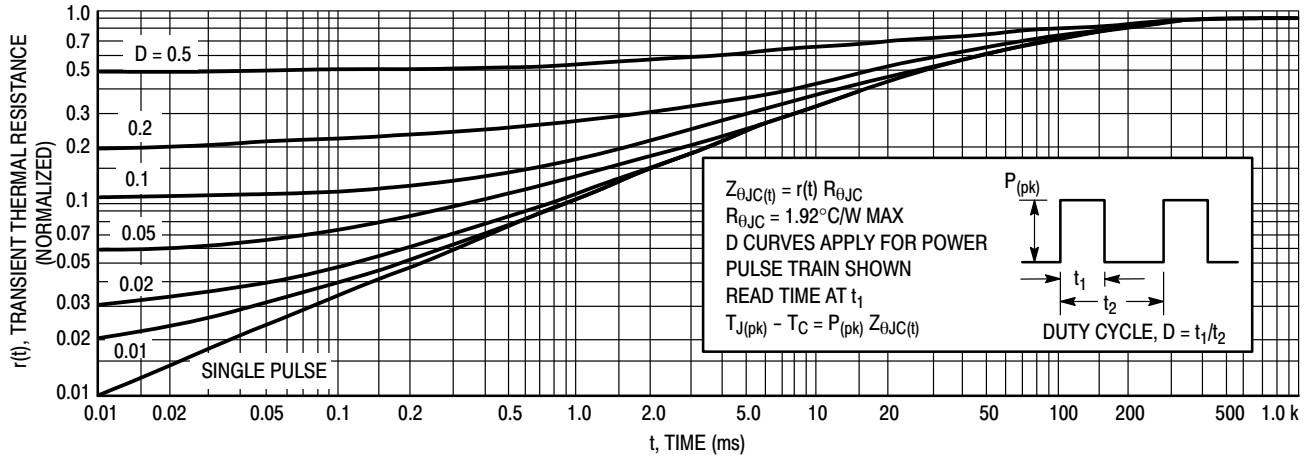


Figure 5. Thermal Response

## TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)

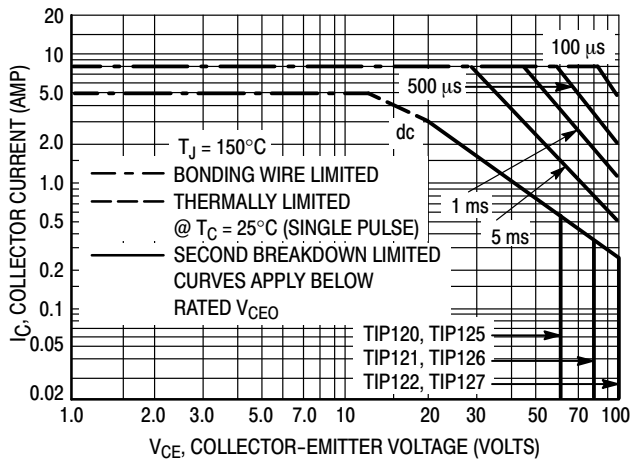


Figure 6. Active-Region Safe Operating Area

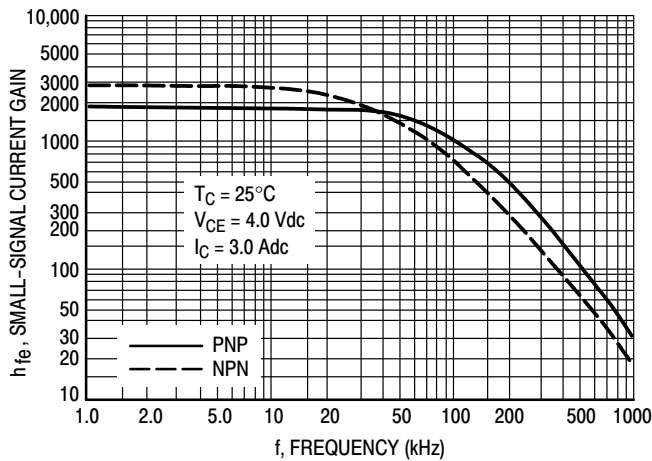


Figure 7. Small-Signal Current Gain

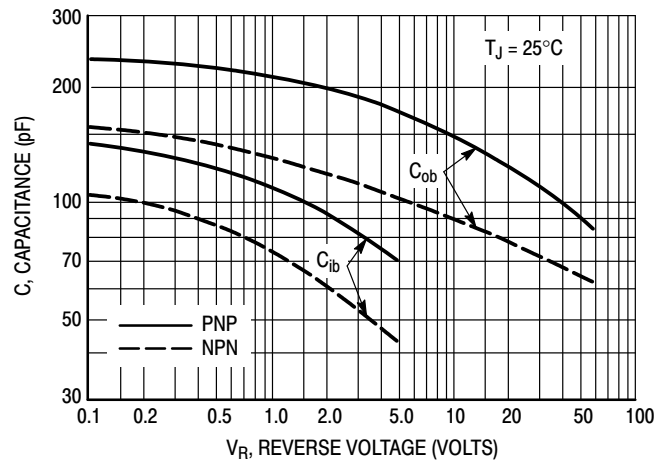


Figure 8. Capacitance

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

TIP120, TIP121, TIP122 (NPN); TIP125, TIP126, TIP127 (PNP)



Figure 9. DC Current Gain



Figure 10. Collector Saturation Region

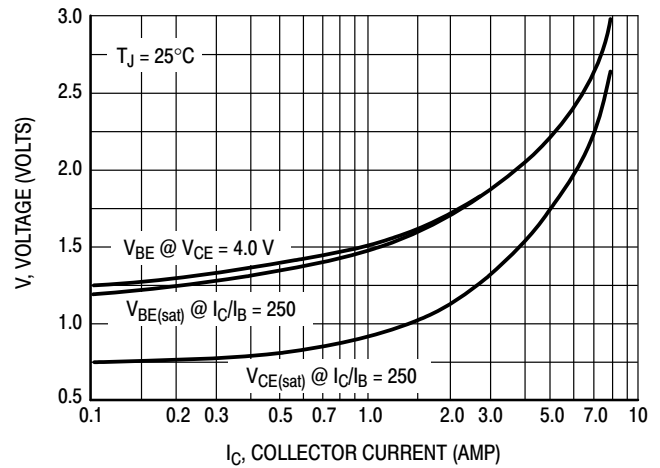
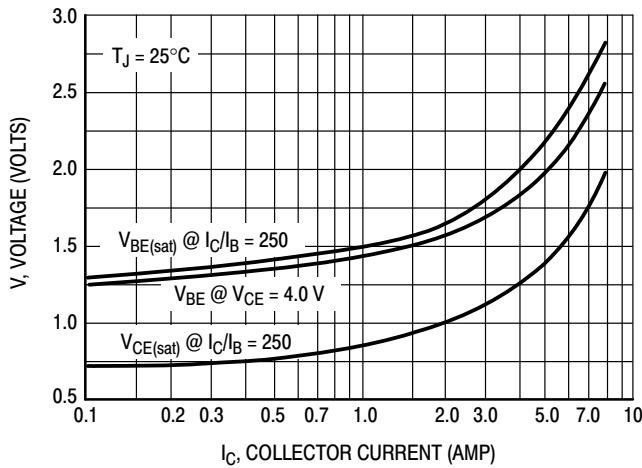
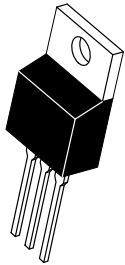


Figure 11. "On" Voltages

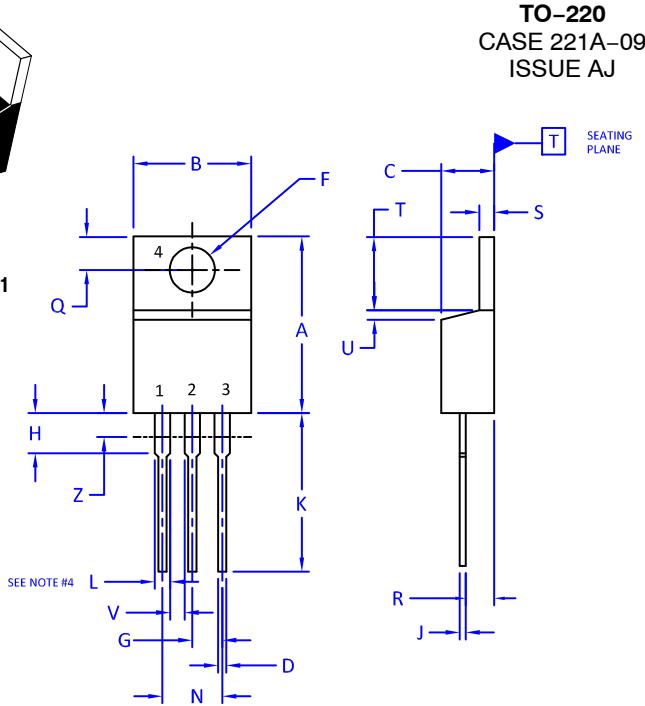
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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SCALE 1:1



**TO-220**  
CASE 221A-09  
ISSUE AJ

DATE 05 NOV 2019

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

**STYLE 1:**

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 2:**

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

**STYLE 3:**

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

**STYLE 4:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

**STYLE 5:**

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

**STYLE 6:**

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

**STYLE 7:**

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

**STYLE 8:**

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

**STYLE 9:**

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 10:**

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

**STYLE 11:**

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

**STYLE 12:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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