# **Complementary Silicon Plastic Power Transistors**

Designed for use as high-frequency drivers in audio amplifiers.

#### **Features**

- High DC Current Gain
- High Current Gain Bandwidth Product
- TO-220 Compact Package
- Epoxy Meets UL 94 V-0 @ 0.125 in
- These Devices are Pb-Free and are RoHS Compliant\*

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	250	Vdc
Collector-Base Voltage	V <sub>CB</sub>	250	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	5.0	Vdc
Collector Current – Continuous	I <sub>C</sub>	8.0	Adc
Collector Current – Peak	I <sub>CM</sub>	16	Adc
Base Current	Ι <sub>Β</sub>	2.0	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	50 0.40	W W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2.0 0.016	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	°C
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	С	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

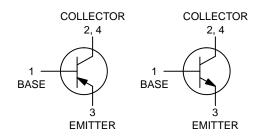


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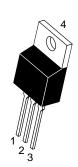
http://onsemi.com

# 8.0 AMPERES POWER TRANSISTORS COMPLEMENTARY SILICON 250 VOLTS, 50 WATTS

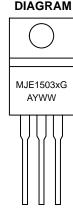
#### **COMPLEMENTARY**



#### MARKING DIAGRAM



TO-220 CASE 221A STYLE 1



MJE1503x = Specific Device Code

= 2 or 3

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

#### **ORDERING INFORMATION**

Device	Package	Shipping
MJE15032G	TO-220 (Pb-Free)	50 Units/Rail
MJE15033G	TO-220 (Pb-Free)	50 Units/Rail

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 1) (I <sub>C</sub> = 10 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	_	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 250 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	10	μAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	10	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain $(I_C = 0.5 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc})$ $(I_C = 1.0 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc})$ $(I_C = 2.0 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc})$	h <sub>FE</sub>	70 50 10	- - -	-
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.1 Adc)	V <sub>CE(sat)</sub>	-	0.5	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 5.0 Vdc)	V <sub>BE(on)</sub>	-	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (Note 2) (I <sub>C</sub> = 500 mAdc, V <sub>CE</sub> = 10 Vdc, f <sub>test</sub> = 1.0 MHz)	fΤ	30	_	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.

2.  $f_T = |h_{fe}| \bullet f_{test}$ .

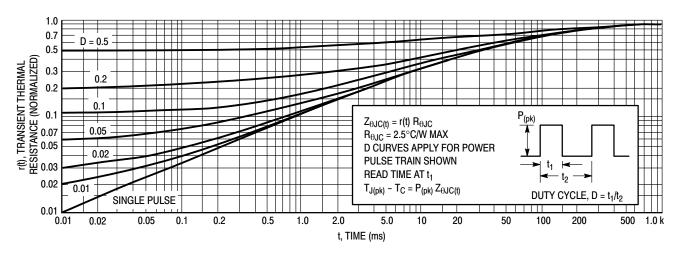


Figure 1. Thermal Response

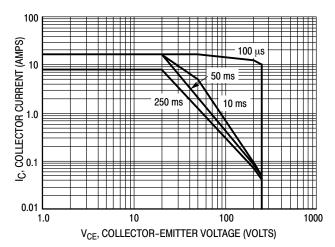


Figure 2. MJE15032 & MJE15033 Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 2 and 4 is based on  $T_{J(pk)}=150^{\circ} C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)}$  < 150°C.  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

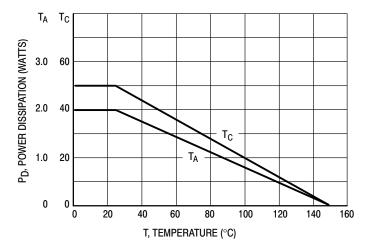
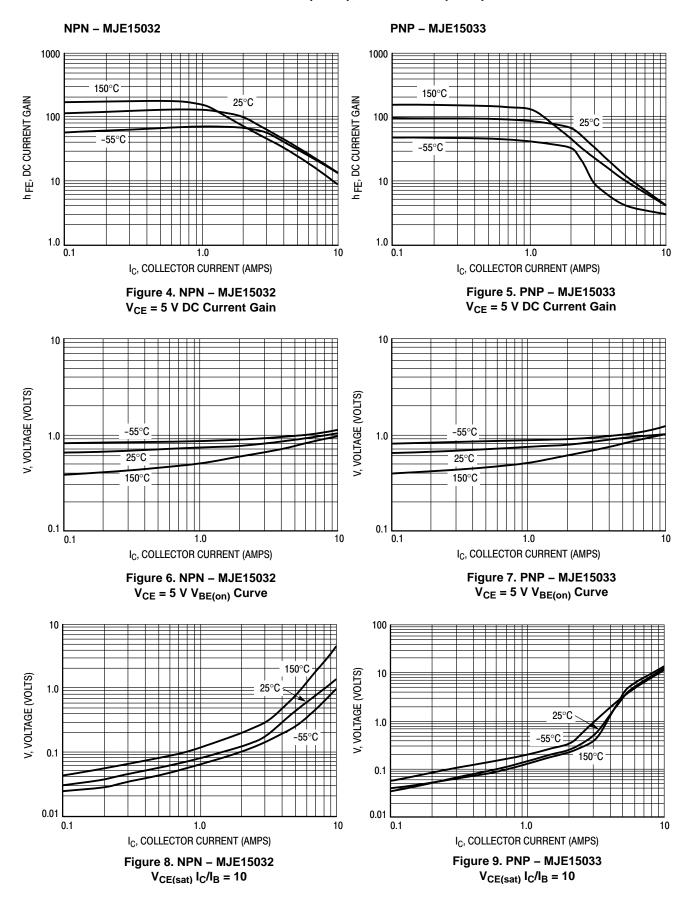
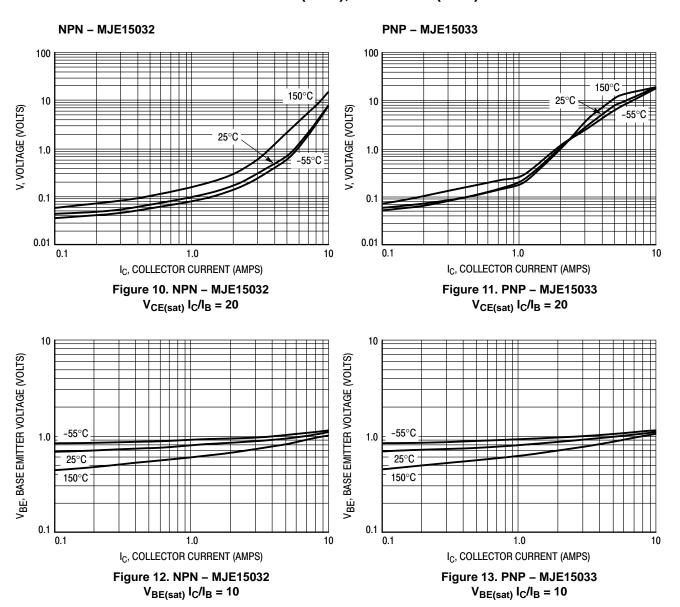
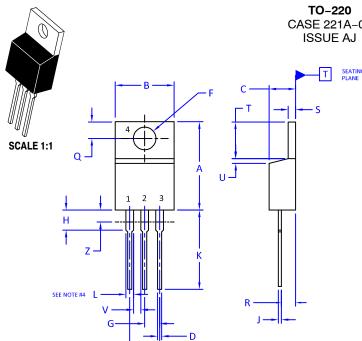


Figure 3. Power Derating





# **MECHANICAL CASE OUTLINE**



CASE 221A-09

**DATE 05 NOV 2019** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: INCHES
- 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

#### 4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS		
DIM	MIN.	MAX.	MIN.	MAX.	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.415	9.66	10.53	
С	0.160	0.190	4.07	4.83	
D	0.025	0.038	0.64	0.96	
F	0.142	0.161	3.60	4.09	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.161	2.80	4.10	
J	0.014	0.024	0.36	0.61	
К	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.41	
Т	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
V	0.045		1.15		
Z		0.080		2.04	

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	BASE	PIN 1.	BASE	PIN 1.	CATHODE	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	EMITTER	2.	ANODE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	COLLECTOR	3.	GATE	3.	GATE
4.	COLLECTOR	4.	EMITTER	4.	ANODE	4.	MAIN TERMINAL 2
STYLE 5:		STYLE 6:		STYLE 7:		STYLE 8:	
PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	CATHODE
2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE
3.	SOURCE	3.	ANODE	3.	CATHODE	3.	EXTERNAL TRIP/DELAY
4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE
STYLE 9:		STYLE 10:		STYLE 11	:	STYLE 12	:
PIN 1.	GATE	PIN 1.	GATE	PIN 1.	DRAIN	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	SOURCE	2.	SOURCE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	DRAIN	3.	GATE	3.	GATE
4.	COLLECTOR	4.	SOURCE	4.	SOURCE	4.	NOT CONNECTED

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