Click here for production status of specific part numbers.

MAX25611A/MAX25611B/ MAX25611C/MAX25611D

Automotive High-Voltage HB LED Controller

General Description

The MAX25611A/MAX25611B/MAX25611C/MAX25611D are single-channel HBLED drivers for automotive front light applications such as high beam, low beam, daytime running light (DRL), turn indicator, fog light, and other LED lights. It can take an input voltage from 5V to 36V and can drive a string of LEDs with a maximum output voltage of 65V.

The MAX25611A/B/C/D sense output current at the high side of the LED string. High-side current sensing is required to protect for shorts from the output to the ground or battery input. It is also the most flexible scheme for driving LEDs, allowing boost, high-side buck, SEPIC mode, or buck-boost mode configurations. The PWM input provides LED dimming ratios of up to 5000:1, and the REFI input provides additional analog dimming capability in the MAX25611A/B/C/D. The MAX25611A/B/C/D have built-in spread-spectrum modulation for improved electromagnetic compatibility performance. The MAX25611A/B/C/D can also be used in zeta and Cuk converter configurations if it is necessary in some applications.

The MAX25611A/B/C/D are available in a space-saving 12-pin SWTQFN-EP package. They are specified to operate over the -40°C to +125°C automotive temperature range. The switching frequency is internally set at 350kHz for the MAX25611A/MAX25611C and 2.2MHz for the MAX25611B/MAX25611D.

Applications

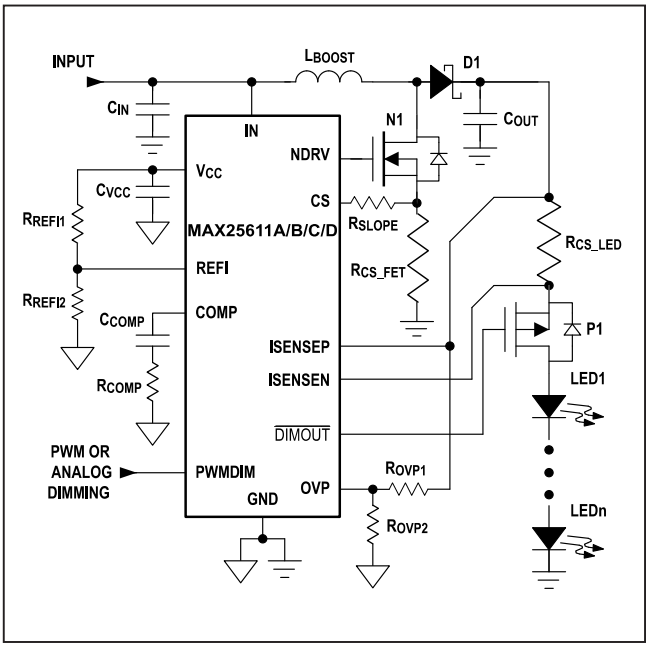
- Automotive Exterior Lighting
- High Beam/Low Beam/Signal/Position Lights
- Daytime Running Lights (DRLs)
- Fog Lights and Adaptive Front-Light Assemblies
- Head-Up Displays
- Commercial, Industrial, and Architectural Lighting

Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Integration Minimizes BOM for High-Brightness LED Driver
  - Integrated pMOS Dimming FET Gate Driver Allows Single-Wire Connection to LED String
  - PWM, Analog-to-PWM and Analog Dimming
  - Integrated High-Side, Current-Sense Amplifier
  - 12-Pin SWTQFN-EP Package
- Flexible Application Configurations
  - +5V to +36V Wide Input Voltage Range with a Maximum +65V Boost Output
  - Boost, Buck-Boost, High-Side Buck, SEPIC, Zeta, and Cuk Single-Channel LED Drivers
- Protection Features and Wide Temperature Range Increase System Reliability
  - Short-Circuit, Overvoltage, and Thermal Protection
  - -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



maxim integrated™

Absolute Maximum Ratings

IN to GND (MAX25611A/B) ..... -0.3V to +40V
IN to GND (MAX25611C/D) ..... -0.3V to +52V
ISENSEP, ISENSEN, $\overline{DIMOUT}$ to GND ..... -0.3V to +70V
$\overline{DIMOUT}$ to ISENSEP ..... -6V to +0.3V
ISENSEP to ISENSEN ..... -0.3V to +0.6V
V_{CC} to GND ..... -0.3V to +6V
NDRV to GND ..... -0.3V to V_{CC} + 0.3V
PWMDIM, REFI, OVP to GND ..... -0.3V to +6V
COMP, CS to GND ..... -0.3V to V_{CC} + 0.3V
Continuous Current on IN 100mA
Peak Current on NDRV ..... ±1A
Continuous Current on NDRV ..... +50mA
Short-Circuit Duration on V_{CC} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Multilayer Board
TQFN (derate 25mW/°C above +70°C) 1951mW
TSSOP (derate 10mW/°C above +70°C) 796.80mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering, 10s) ..... +300ºC
Storage Temperature Range ..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12-Pin, SWTQFN-EP

Package Code	T1244Y+4C
Outline Number	**21-100312**
Land Pattern Number	**90-0068**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	59.3°C/W
Junction to Case (θ_{JC})	6°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.4°C/W
Junction to Case (θ_{JC})	41°C/W

14-Pin, TSSOP

Package Code	U14+5C
Outline Number	**21-0066**
Land Pattern Number	
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	110°C/W
Junction to Case (θ_{JC})	30°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	100.4°C/W
Junction to Case (θ_{JC})	30°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = unconnected, V_{CS} = V_{OVP} = V_{GND} = 0V, $V_{ISENSEP}$ = $V_{ISENSEN}$ = 45V, V_{REFI} = 1.20V. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES AND SUPPLY CURRENT						
Input Voltage Range	V_{IN}	MAX25611A/B	5		36	V
	V_{IN_MAX}	t < 1s, MAX25611A/B			40	
	V_{IN}	MAX25611C/D	5		48	
	V_{IN_MAX}	t < 1s, MAX25611C/D			52	
Quiescient Supply Current	I_{INQ}	V_{OVP} = 1.5V, no switching, T_A = +25°C		1.8	3.5	mA
V_{CC} REGULATOR						
Output Voltage	V_{CC}	Load = 0.1mA to 15mA	4.875	5	5.125	V
VCC UVLO Rising	VCC_{UVLOR}	Rising, 1V (typ) hysteresis		4.3		V
Short-Circuit Current Limit	I_{VCC_SC}	V_{CC} shorted to GND		50		mA
SWITCHING FREQUENCY						
Switching Frequency	f_{SW}	MAX25611A	315	350	385	kHz
		MAX25611B	1980	2200	2420	
Frequency Dither	f_{SW_DITH}	Dither enable		±6		%
SLOPE COMPENSATION						
Slope Compensation Current Ramp Height	I_{SLOPE}	Peak current ramp out from CS pin per switching period	42.5	50	57.5	µA
ANALOG DIMMING						
REFI Input Control Voltage Range	V_{REFI_RNG}		0.2		1.2	V
REFI Zero Current Threshold	V_{REFI_ZTH}	($V_{ISENSEP}$ - $V_{ISENSEN}$) < 5mV	0.16	0.18	0.20	V
REFI Internal Clamp Voltage	V_{REFI_CLMP}	REFI sink = 1µA	1.25	1.3	1.35	V
REFI Input Bias Current	I_{REFI}	V_{REFI} = 0V to 5.5V		20	500	nA
LED CURRENT SENSE AMP						
Common-Mode Input Range			-0.2		+65	V
Differential Signal Range			0		200	mV
ISENSEP Input Bias Current	$I_{B\_ISENSEP}$	($V_{ISENSEP}$ - $V_{ISENSEN}$) = 200mV, $V_{ISENSEP}$ = 60V		350	550	µA
ISENSEN Input Bias Current	$I_{B\_ISENSEN}$	($V_{ISENSEP}$ - $V_{ISENSEN}$) = 200mV, $V_{ISENSEN}$ = 60V		22	60	µA

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = unconnected, V_{CS} = V_{OVP} = V_{GND} = 0V, $V_{ISENSEP}$ = $V_{ISENSEN}$ = 45V, V_{REFI} = 1.20V. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain		($V_{ISENSEP}$ - $V_{ISENSEN}$) = 200mV, 3V < ($V_{ISENSEP}$, $V_{ISENSEN}$) < 60V	4.9	5	5.1	V/V
LED Current-Sense Regulation Voltage	V_{SENSE}	V_{REFI} = 1.3V, 3V < ($V_{ISENSEP}$, $V_{ISENSEN}$) < 60V	214	220	226	mV
		V_{REFI} = 1.2V, 3V < ($V_{ISENSEP}$, $V_{ISENSEN}$) < 60V	194	200	206	
		V_{REFI} = 0.4V, 3V < ($V_{ISENSEP}$, $V_{ISENSEN}$) < 60V	36	40	44	
LED Current-Sense Regulation Voltage (Low Range)	V_{SENSE_LOW}	V_{REFI} = 1.2V, 0V < $V_{ISENSEP}$, $V_{ISENSEN}$ < 3V	193	200	207	mV
		V_{REFI} = 0.4V, 0V < $V_{ISENSEP}$, $V_{ISENSEN}$ < 3V	35	40	45	
Common-Mode Input Range Selector	RNG_{SEL}	$V_{ISENSEP}$ rising	2.72	2.85	2.98	V
	RNGSEL	$V_{ISENSEP}$ falling	2.48	2.6	2.72	
ERROR AMP						
Transconductance	g_M	($V_{ISENSEP}$ - $V_{ISENSEN}$) = 200mV	1170	1800	2430	µS
COMP Sink Current	$COMP_{ISINK}$	V_{COMP} = 5V		300		µA
COMP Source Current	$COMP_{ISRC}$	V_{COMP} = 0V		300		µA
PWM COMPARATOR						
Input Offset Voltage				1		V
PWM to NDRV Propagation Delay		Includes leading edge blanking time		90		ns
CURRENT LIMIT COMPARATOR						
Current Limit Threshold	V_{CS_LIMIT}		388	418	448	mV
GATE DRIVER (NDRV)						
RDSon Pullup pMOS	R_{NDRV_HIGH}			1.5		Ω
RDSon Pulldown nMOS	R_{NDRV_LOW}	V_{COMP} = 0V, I_{SINK} = 100mA		1.5		Ω
Rise Time	t_R	C_{NDRV} = 10nF		100		ns
Fall Time	t_F	C_{NDRV} = 10nF		100		ns
PWM DIMMING						
Internal Ramp Frequency	f_{RAMP}		160	200	240	Hz
External Sync Frequency Range	f_{DIM}		60		2000	Hz
External Sync Low-Level Voltage	V_{PWMDIM_L}				0.4	V
External Sync High-Level Voltage	V_{PWMDIM_H}		2			V

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = unconnected, V_{CS} = V_{OVP} = V_{GND} = 0V, $V_{ISENSEP}$ = $V_{ISENSEN}$ = 45V, V_{REFI} = 1.20V. Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIM Comparator Offset Voltage	V_{PWMDIM_OFS}		170	200	230	mV
DIM Voltage for 100% Duty Cycle			3.1			V
PWMDIM Low to NDRV Low Delay				120		ns
PWMDIM High to NDRV High Delay				88		ns
PWMDIM to LED Turn-Off Time		PWMDIM falling edge to rising edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 7nF		4.2		µs
PWMDIM to LED Turn-On Time		PWMDIM rising edge to falling edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 7nF		3.9		µs
DIMMING MOSFET GATE DRIVER ($\overline{DIMOUT}$)						
Peak Pullup Current	$I_{\overline{DIMOUT}\_PU}$	PWMDIM = low, ($V_{ISENSEP}$ - $V_{\overline{DIMOUT}}$) = 5V (Note 2)	25	50	80	mA
Peak Pulldown Current	$I_{\overline{DIMOUT}\_PD}$	PWMDIM = high, ($V_{ISENSEP}$ - $V_{\overline{DIMOUT}}$) = 0V (Note 2)	10	25	50	mA
$\overline{DIMOUT}$ Low Voltage with Respect to ISENSEP			-5.4	-5	-4.6	V
SHORT-CIRCUIT HICCUP MODE						
Short-Circuit Current Threshold	V_{IOUT_SHRT}	($V_{ISENSEP}$ - $V_{ISENSEN}$)	369	398	427	mV
Short-Circuit Voltage Detect Threshold	V_{VOUT_SHRT}	($V_{ISENSEP}$ - V_{IN}) falling, V_{IN} = 12V	1.15	1.55	1.95	V
Hiccup Time	t_{HICCUP}	After (V_{IOUT_SHRT} and V_{VOUT_SHRT}) detected		8192		Clock Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising		165		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
OVERVOLTAGE PROTECTION (OVP)						
OVP Threshold Rising	V_{OVP_TH}	Output rising, 70mV hysteresis	1.17	1.23	1.29	V
OVP Input Bias Current	I_{OVP}	V_{OVP} = 1.235V	-500		+500	nA

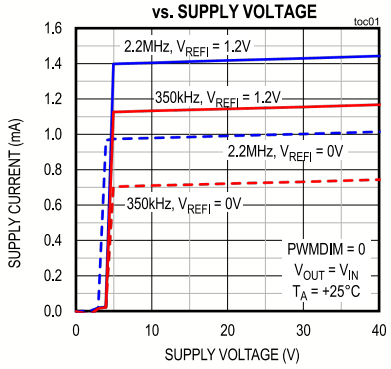
Note 1: Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design. Not production tested.

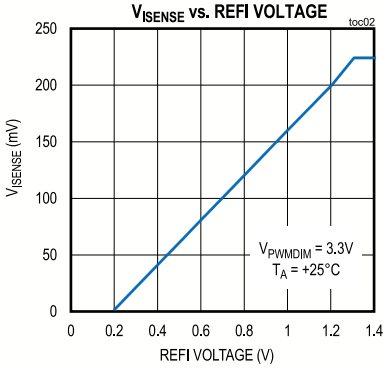
Typical Operating Characteristics

(*Typical Operating Circuit*, V_{IN} = 12V, 8x LEDs, T_A = +25°C, unless otherwise noted.)

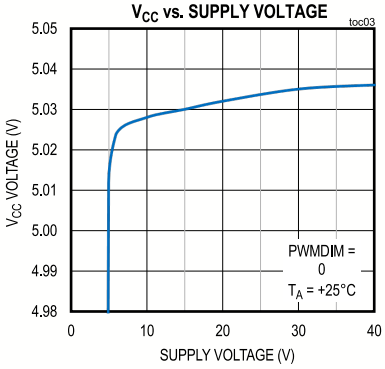
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



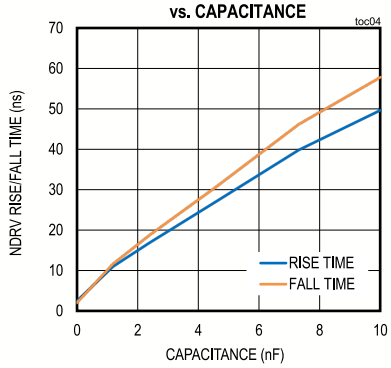
VISENSE vs. REFI VOLTAGE



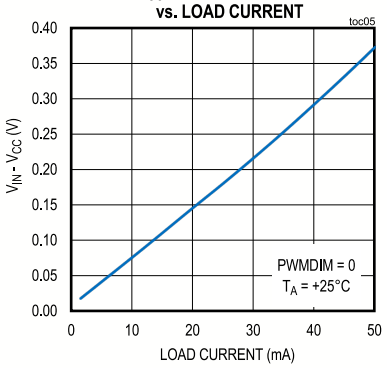
VCC vs. SUPPLY VOLTAGE



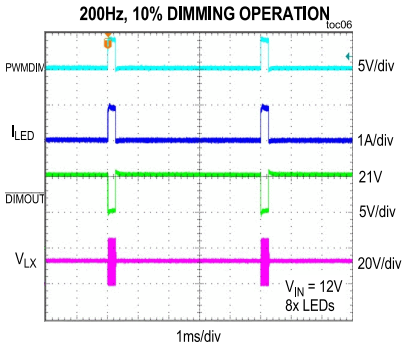
NDRV RISE/FALL TIM vs. CAPACITANCE



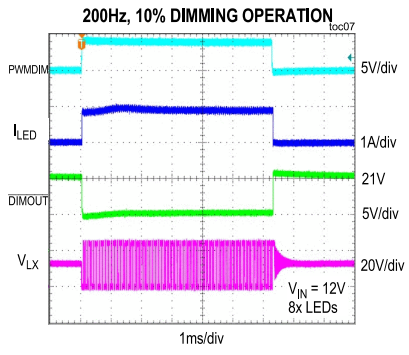
VCC DROPOUT VOLTAGE vs. LOAD CURRENT



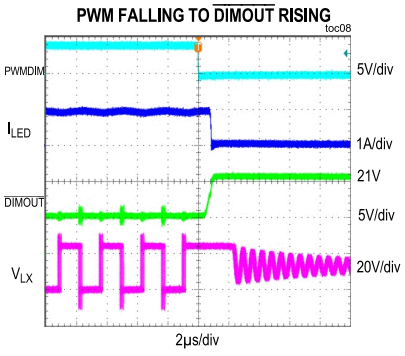
200Hz, 10% DIMMING OPERATION



200Hz, 10% DIMMING OPERATION



PWM FALLING TO $\overline{DIMOUT}$ RISING

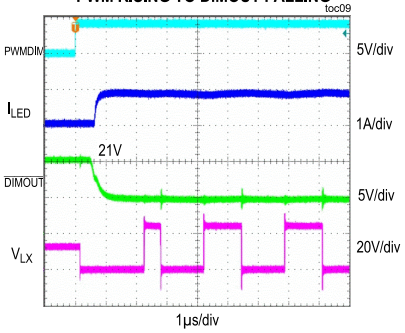


PRELIMINARY

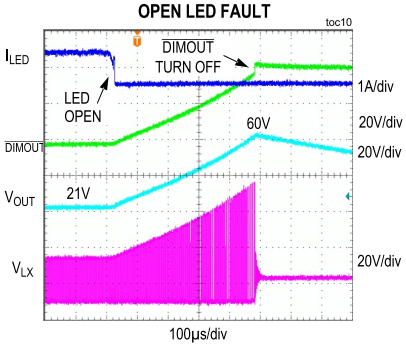
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN} = 12V, 8x LEDs, T_A = +25°C, unless otherwise noted.)

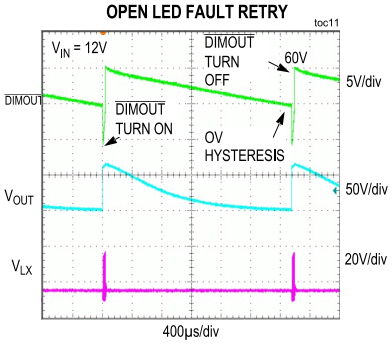
PWM RISING TO $\overline{DIMOUT}$ FALLING



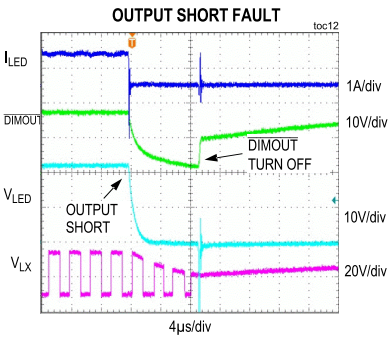
OPEN LED FAULT



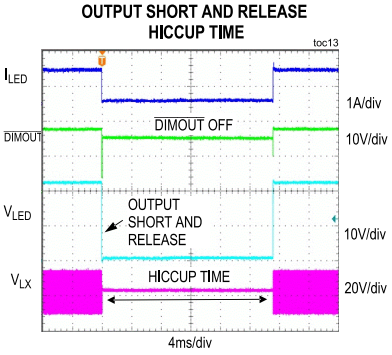
OPEN LED FAULT RETRY



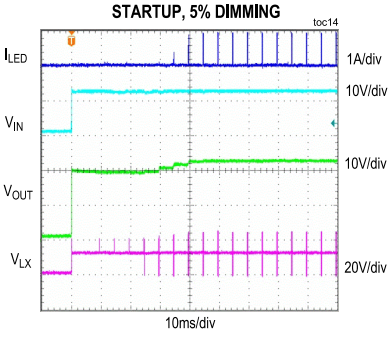
OUTPUT SHORT FAULT



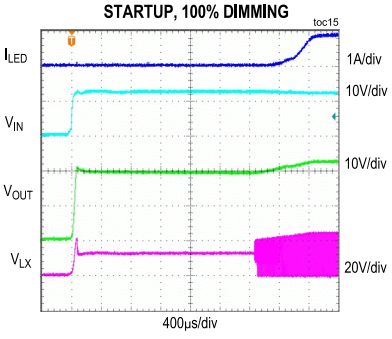
OUTPUT SHORT AND RELEASE HICCUP TIME



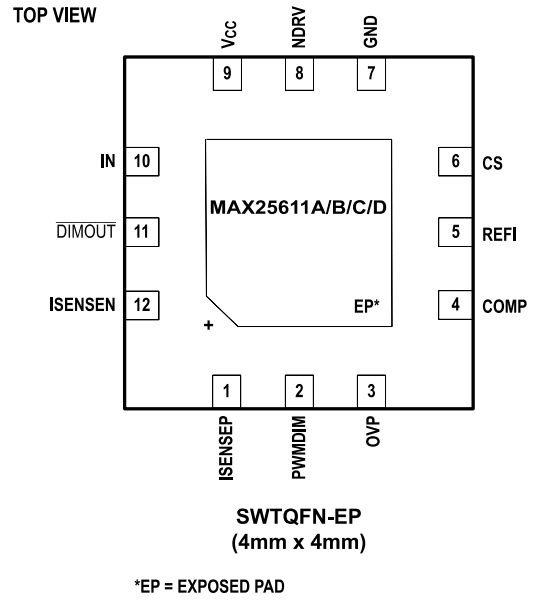
STARTUP, 5% DIMMING



STARTUP, 100% DIMMING

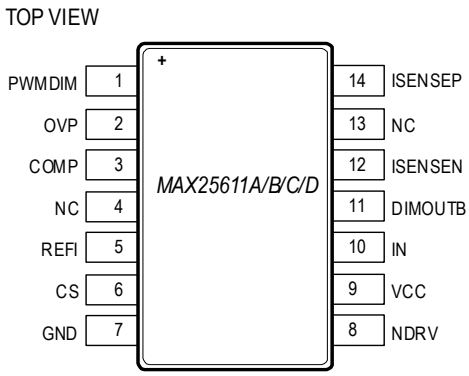


Pin Configuration



SWTQFN-EP
(4mm x 4mm)

*EP = EXPOSED PAD



TSSOP

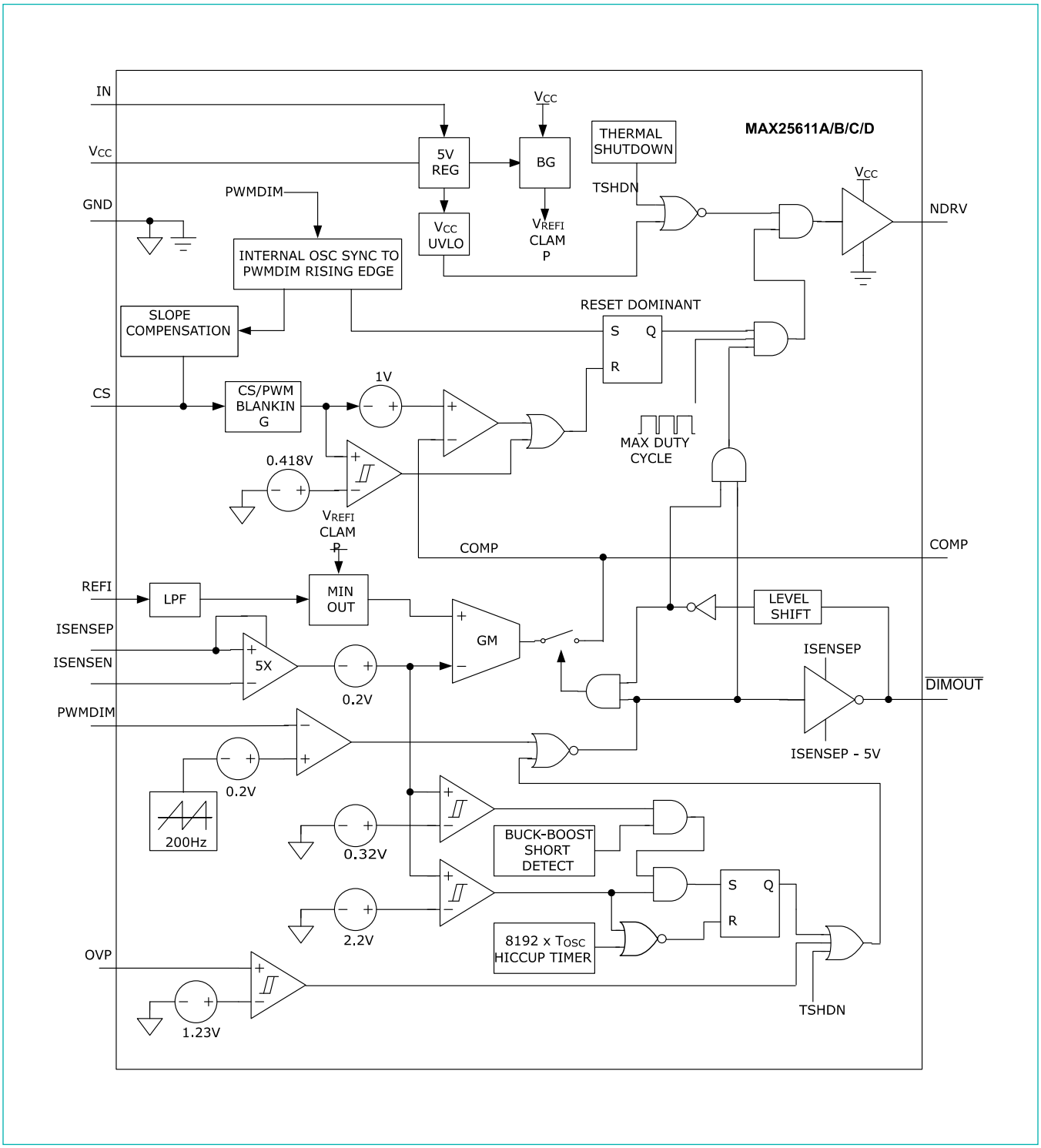
Pin Description

TSSOP 14-PIN	SW-TQFN 12-PIN	NAME	FUNCTION
14	1	ISENSEP	Positive LED Current-Sense Input. Place a 0.1µF common-mode filter capacitor from ISENSEP to GND near the IC. Place a 100pF differential mode filter capacitor across ISENSEP and ISENSEN near the IC.
1	2	PWMDIM	Dimming Control Input. Connect PWMDIM to an external 3.3V or 5V PWM signal for PWM dimming. For analog voltage controlled PWM dimming, connect PWMDIM to V_{CC} through a resistive voltage-divider with voltage between 0.2V and 3V. The dimming frequency is 200Hz under these conditions, and the duty cycle is (V_{PWMDIM} - 0.2)/2.8V. Connect PWMDIM to GND to turn off the LEDs. Connect PWMDIM to V_{CC} for 100% duty cycle. Bypass PWMDIM to GND with a 0.1µF ceramic capacitor when using analog PWMDIM.
2	3	OVP	Overvoltage-Protection Input for the LED String. Connect a resistor-divider between the boost output, OVP, and GND. When the voltage on OVP exceeds 1.23V, a fast-acting comparator immediately stops PWM switching and pulls $\overline{DIMOUT}$ high to disconnect the LED string from the boost output. $$V_{OVP} = 1.23\frac{(R_{OVP1} + R_{OVP2})}{R_{OVP2}}$$

Pin Description (continued)

<table>
<tr><th>TSSOP 14-PIN</th><th>SW-TQFN 12-PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>3</td><td>4</td><td>COMP</td><td>Compensation Network Connection. For proper compensation, connect a suitable RC network from
COMP to GND.</td></tr>
<tr><td>5</td><td>5</td><td>REFI</td><td>Analog Dimming Control Input. The voltage at REFI sets the LED current level when V_{REFI} < 1.3V.
This voltage reference can be set using a voltage divider from V_{CC} to GND. For V_{REFI} > 1.3V, the internal reference sets the LED current.
$$I_{LED} = \frac{(V_{REFI} - 0.2V)}{5 \times R_{CS\_LED}}$$
Bypass REFI to GND with at least a 10nF ceramic capacitor for noise filter. Not needed if V_{REFI} > 1.3V.</td></tr>
<tr><td>6</td><td>6</td><td>CS</td><td>Current-Sense Amplifier Positive Input for the Switching Regulator. Add a resistor from CS to the
switching MOSFET current-sense resistor terminal to program the slope compensation.</td></tr>
<tr><td>7</td><td>7</td><td>GND</td><td>Power and Analog Ground. Star point connection for power ground and analog ground.</td></tr>
<tr><td>8</td><td>8</td><td>NDRV</td><td>External n-Channel Gate Driver Output</td></tr>
<tr><td>9</td><td>9</td><td>V_{CC}</td><td>5V Low-Dropout Voltage Regulator Output. V_{CC} supplies the bias for the gate drive and internal control logic. Bypass V_{CC} to GND with a 4.7µF and 0.1µF ceramic capacitor.</td></tr>
<tr><td>10</td><td>10</td><td>IN</td><td>Positive Power-Supply Input. Bypass IN to GND with at least a 1µF ceramic capacitor.</td></tr>
<tr><td rowspan="4">11</td><td rowspan="4">11</td><td rowspan="4">$\overline{DIMOUT}$</td><td>External Dimming p-Channel MOSFET Gate Driver. $\overline{DIMOUT}$ drives the gate of the external p-Channel MOSFET based on the signal at PWMDIM.</td></tr>
<tr><td>
<table>
<tr><th>PWMDIM</th><th>$\overline{DIMOUT}$</th><th>APPLICATION FUNCTION</th></tr>
<tr><td>Low</td><td>High, pulled up to ISENSEP</td><td>External PFET off. LEDs disabled (dimmed).</td></tr>
<tr><td>High</td><td>Low, pulled down to ISENSEP-5V</td><td>External PFET on. LEDs enabled.</td></tr>
</table>
</td></tr></tr>
<tr><td>12</td><td>12</td><td>ISENSEN</td><td>Negative LED Current-Sense Input. A 100Ω series resistor protects against large differential voltages across ISENSEP and ISENSEN that might occur during an output short.v</td></tr>
<tr><td>13</td><td>–</td><td>NC</td><td>No Connection</td></tr>
<tr><td>14</td><td>–</td><td>NC</td><td>No Connection</td></tr>
</table>

Functional Diagram



Detailed Description

Functional Operation of the MAX25611A/B/C/D

The MAX25611A/B/C/D is a constant-frequency, current-mode controller with a low-side nMOS gate driver. The operation of the devices is best understood by seeing the *Functional Diagram*. The devices are enabled when the 5V regulator is above its UVLO limit of 4.5V (typ), before switching on NDRV can begin. The nMOS gate-drive voltage and the control circuitry inside the device uses the 5V supply.

When PWMDIM goes high, switching is initiated. The internal oscillator runs at either 350kHz (MAX25611A) or 2.2MHz (MAX25611B). Additional spread-spectrum dithering is added to the oscillator to alleviate EMI problems in the LED driver. The internal oscillator is synchronized to the positive going edge of the PWMDIM pulse. This means that the NDRV pulse goes high at the same instant as the positive-going pulse on PWMDIM. This guarantees that the switching frequency variation over a period of a PWMDIM pulse is the same from one PWMDIM pulse to the next. This prevents flicker during PWM dimming especially for short PWMDIM pulse widths.

Once PWMDIM goes high, the external switching MOSFET is turned on. Current flows through the external switching MOSFET and this current is sensed by the voltage across the current-sense resistor from the source of the external MOSFET to GND. The source of the external MOSFET is connected to the CS pin of the device through a slope-compensation resistor (R_{SLOPE}). See the *Typical Boost Application Circuit*. The slope-compensation current flows out of the CS pin into the R_{SLOPE} resistor. The voltage on CS is the voltage across the current-sense resistor (R_{CS_FET}) + slope-compensation current x R_{SLOPE}. The slope compensation prevents subharmonic oscillation when duty cycles exceed 50%.

The voltage on CS is fed to a current-limit comparator. This current-limit comparator is used to protect the external switch from overcurrents and causes switching to stop for that particular cycle if the CS voltage exceeds 0.418V (typ). An offset of 1.0V is added to the CS voltage, and this voltage is fed to the positive input of a PWM comparator. The negative input of this comparator is a control voltage from the error amplifier that regulates the LED current. When the positive input of the PWM comparator exceeds the control voltage from the error amplifier, the switching is stopped for that particular cycle and the external nMOS stays off until the next switching cycle.

When the external MOSFET is turned off, the inductor current is transferred to the output. When the next switching cycle starts and the external MOSFET is turned on, the inductor current starts ramping back up. Through this repetitive action, the PWM-control algorithm establishes a switching duty cycle to regulate current to the LED load.

The external pMOS is turned on when PWMDIM is high and is turned off when PWMDIM is low. This external dimming MOSFET is a p-channel MOSFET and is connected on the high side. The source of this pMOS is connected to ISENSEN and the gate is connected to $\overline{DIMOUT}$. The drain of this MOSFET is connected to the anode of the external LED string. In certain applications, it is not necessary to use this dimming MOSFET and in these cases, the $\overline{DIMOUT}$ pin is left open. During normal operation when PWMDIM is high, the voltage across the resistor from ISENSEP to ISENSEN is regulated to a programmed voltage set by REFI.

The external pMOS switch is also used for fault protection as well. Once a fault condition is detected, the $\overline{DIMOUT}$ pin is pulled high to turn off the pMOS switch. This isolates the LED string from the fault condition and prevents excessive voltage or current from damaging the LEDs.

Input Voltage (IN)

The input supply pin (IN) must be locally bypassed with a minimum of 1µF capacitance close to the pin. All the input current drawn by the device goes through this pin. The positive terminal of the bypass capacitor must be placed as close as possible to this pin and the negative terminal of the bypass capacitor must be placed as close as possible to the GND pin.

V_{CC} Linear Regulator

The devices feature a 5V linear regulator (V_{CC}) with IN as its source. Use a 4.7µF and a 0.1µF low-ESR ceramic capacitor from V_{CC} to GND for stable operation. The V_{CC} regulator provides power to all the internal logic, control circuitry and the MOSFET gate drive. The devices are enabled when V_{CC} is above its UVLO threshold of 4.3V (typ).

The overcurrent limit on the V_{CC} regulator is 150mA (typ) and the foldback short to GND current limit is 50mA (typ). It is also possible to apply an external voltage on the V_{CC} regulator output and save its power dissipation. The maximum externally applied voltage on V_{CC} should not exceed its absolute maximum rating.

Dimming MOSFET Driver ($\overline{DIMOUT}$)

The devices require an external p-channel MOSFET for PWM dimming. For normal operation, connect the gate of the MOSFET to the output of the dimming driver ($\overline{DIMOUT}$). The dimming driver can sink up to 25mA or source up to 50mA of peak current for fast charging and discharging of the pMOS gate. When the PWMDIM signal is high, this driver pulls the pMOS gate to 5V below the ISENSEP pin to completely turn on the p-channel dimming MOSFET. The $\overline{DIMOUT}$ pin inverts and level shifts the signal on PWMDIM to drive the gate of the external pMOS. In some applications, the pMOS dimming MOSFET is not required, and the $\overline{DIMOUT}$ pin can be left open.

LED Current-Sense Inputs (ISENSEP, ISENSEN)

The differential voltage from ISENSEP to ISENSEN is fed to an internal current-sense amplifier. This amplified signal is then connected to the negative input of the transconductance error amplifier. The voltage-gain factor of this amplifier is 5. The resistor connected between ISENSEP and ISENSEN to programs the maximum LED current. The full-scale signal is 220mV when the REFI voltage is 1.3V or higher.

Switching Frequency

The internal oscillator runs at either 350kHz (MAX25611A/MAX25611C) or 2.2MHz (MAX25611B/MAX25611D). The devices have built-in frequency dithering of ±6% of the programmed frequency to alleviate EMI problems.

The internal oscillator is synchronized to the positive going edge of the PWMDIM pulse. This means that the NDRV pulse goes high at the same instant as the positive-going pulse on PWMDIM. This guarantees that the switching frequency variation over a period of a PWMDIM pulse is the same from one PWMDIM pulse to the next. This prevents flicker during PWM dimming especially for short PWMDIM pulse widths.

Spread Spectrum

The device has an internal spread-spectrum option to optimize EMI performance. The switching frequency is varied ±6%, centered on the oscillator frequency (f_{OSC}). The modulation signal is a triangular wave with a period of 418 clocks. Therefore, f_{OSC} ramps down 6% and back to the set frequency in 418 clocks, and also ramps up 6% and back to the set frequency in another 418 clocks. The total modulation period is 2.4ms for 350kHz and 380µs for 2.2MHz.

n-Channel Switching-MOSFET Driver (NDRV)

The device drives an external n-channel switching MOSFET (NDRV). NDRV swings between V_{CC} and GND. NDRV can sink/source 1A of peak current, allowing the ICs to switch MOSFETs in high-power applications. The average current demanded from the supply to drive the external MOSFET depends on the total gate charge (Qg) and the operating frequency of the converter (f_{SW}). Use the following equation to calculate the driver supply current (INDRV) required for the switching MOSFET:

$$I_{NDRV} = Qg \times f_{SW}$$

Switching-MOSFET Current-Sense Input (CS)

CS is part of the current-mode-control loop. The switching control uses the voltage on CS, set by R_{CS_FET} and R_{SLOPE} to terminate the on-pulse width of the switching cycle, thus achieving peak current-mode control. Internal leading-edge blanking of 66ns is provided to prevent premature turn-off of the switching MOSFET in each switching cycle. Resistor R_{CS_FET} is connected between the source of the n-channel switching MOSFET and GND. During switching, a current ramp with a slope of 50µA x f_{SW} is sourced from the CS pin. This current ramp, along with resistor R_{SLOPE}, programs the amount of slope compensation.

Overvoltage Protection (OVP)

OVP sets the overvoltage-threshold limit across the LEDs. Use a resistor-divider between ISENSEP to OVP and GND to set the overvoltage-threshold limit. An internal overvoltage-protection comparator senses the differential voltage across OVP and GND. If the differential voltage is greater than 1.23V, the device stops switching, NDRV goes low, and $\overline{DIMOUT}$ goes high. When the differential voltage drops by 70mV, NDRV is enabled if PWMDIM is high and $\overline{DIMOUT}$ goes low.

Output Short-Circuit Protection

The MAX25611A/B/C/D feature output short-circuit protection. This feature is most useful where the LEDs are connected over long cables and there is possibility of shorts occurring when connectors are exposed.

A short circuit is detected when the following two conditions are met:

- $V_{ISENSEP}$ is lower than V_{IN} by the V_{OUT_SHRT} threshold, -1.55V (typ)
- The current sense voltage across $V_{ISENSEP}$ - $V_{ISENSEN}$ exceeds the V_{IOUT_SHRT} threshold, 398mV (typ)

The MAX25611A/B/C/D respond by stopping NDRV and pulling $\overline{DIMOUT}$ high to ISENSEP to turn off the DIM FET, disconnecting the output capacitors from the shorted output.

Current Limited Short-Circuit Protection

Faster current limited output short-circuit protection can be achieved by adding a small-signal PNP transistor across R_{CS_LED} as shown in Figure 1. The current is limited to V_{BE}/R_{CS_LED}, which is roughly three times the maximum programmed current. When this limit is reached, the PNP pulls up on the gate of the DIM FET P1, reducing the gate voltage that increases the drain-source resistance to limit the current. A 1kΩ resistor on $\overline{DIMOUT}$ allows the PNP to drive the DIM FET gate high while $\overline{DIMOUT}$ is still low.

Internal Transconductance Amplifier

The devices have a built-in transconductance amplifier used to amplify the error signal inside the feedback loop. The typical transconductance is 1800µS.

Analog Dimming

The device offers an analog dimming-control input pin (REFI). The voltage at REFI sets the LED current level linearly from zero with up to maximum when V_{REFI} = 1.3V. For V_{REFI} > 1.3V, an internal reference sets the LED current. The maximum withstand voltage of this input is 6V. The LED current is guaranteed to be at zero when the REFI voltage is at or below the zero current threshold of 0.18V (typ). The LED current can be linearly adjusted from zero to full scale for the REFI voltage in the range of 0.2V to 1.3V.

Pulsed-Dimming Input (PWMDIM)

PWMDIM functions with either analog or PWM control signals. Once the internal pulse detector detects three successive edges of a PWM signal with a frequency between 60Hz and 2kHz, the device synchronizes to the external signal and pulse-width modulates the LED current at the external PWMDIM input frequency, with the same duty cycle as the PWMDIM input. If an analog control signal is applied to PWMDIM, the device compares the DC input to an internally generated 200Hz ramp to pulse-width-modulate the LED current (f_{DIM} = 200Hz). The output-current duty cycle is linearly adjustable from 0% to 100% (0.2V < V_{PWMDIM} < 3V). Use the following formula to calculate the voltage (V_{PWMDIM}), necessary for a given output-current duty cycle (D):

$$V_{PWMDIM} = (D \times 2.8V) + 0.2V$$

where V_{PWMDIM} is the voltage applied to the PWMDIM pin.

Rearranged to calculate duty cycle:

$$Duty\text{-}Cycle = \frac{\left(V_{PWMDIM} - 0.2V\right)}{2.8V}$$

Ground (GND)

This pin is both the power ground and the analog ground. Place the negative terminal of the IN and V_{CC} bypass capacitors as close as possible to the GND pin. The negative terminals for other decoupling capacitors on REFI, PWMDIM, and COMP should be connected together and connected to the GND pin through a path that does not carry any high switching current.

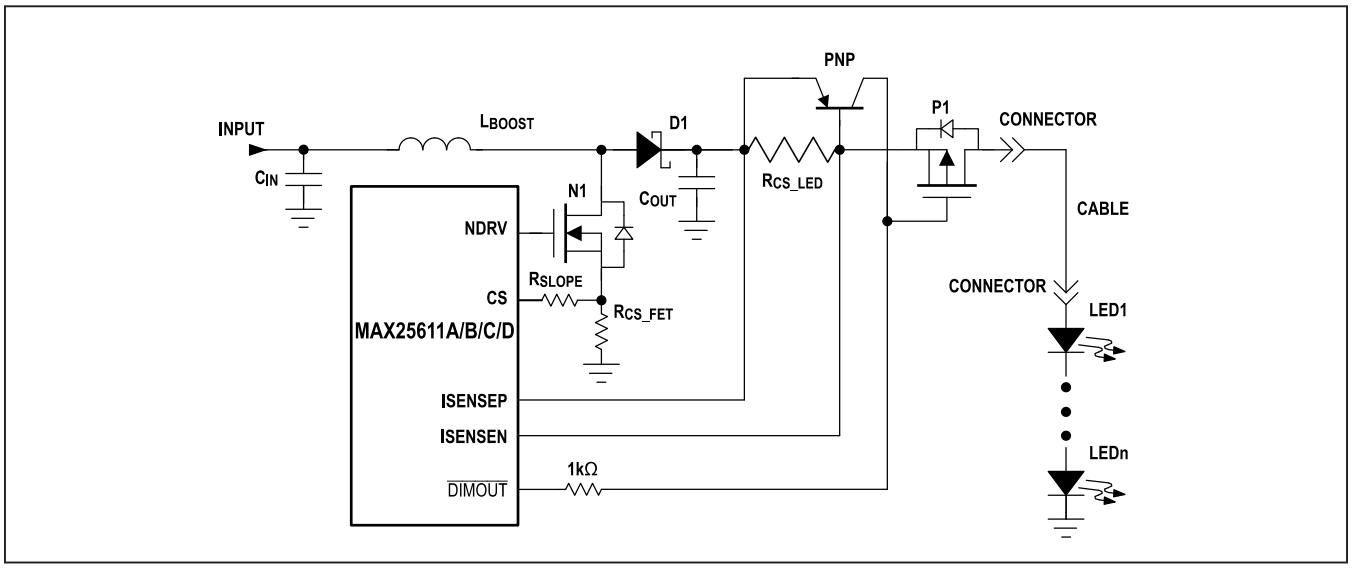


Figure 1. Current Limited Short-Circuit Protection

Thermal Shutdown

Internal thermal-shutdown circuitry is provided to protect the device in the event the maximum junction temperature is exceeded. The threshold for thermal shutdown is +165°C (typ) with 15°C (typ) hysteresis. The part returns to regulation mode once the junction temperature goes below +150°C (typ). This results in a cycled output during continuous thermal-overload conditions.

Fault Protection

The device shuts down when one of the following conditions occur:

- Overvoltage or open across the LED string. The device restarts after the output voltage drops below the OVP hysteresis (70mV (typ) at the OVP pin).
- Short-circuit condition across the LED string. The device enters hiccup mode and restarts after the hiccup timer has expired. The hiccup timer is 8192 clock cycles.
- Overtemperature condition. The device restarts after the die temperature falls below the 15°C (typ) hysteresis.

Exposed Pad

The MAX25611A/B/C/D package features an exposed thermal pad on its underside that should be used as a heat sink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and GND to the system ground using a large pad or ground plane, or multiple vias to the ground plane layer.

Applications Information

Programming the LED Current

Normal sensing of the LED current should be done on the high side where the LED current-sense resistor is connected to the anode of the LED string. The LED current is programmed using resistor R_{CS_LED}. See the *Simplified Application Circuit*.

The LED current can also be programmed adjusting the voltage on REFI when $V_{REFI} \le 1.3V$ (analog dimming). The current is given by:

$$I_{LED} = \frac{\left(V_{REFI} - 0.2V\right)}{5 \times R_{CS\_LED}}$$

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors ROVP1 and ROVP2. See the *Simplified Application Circuit*. The overvoltage circuit in the device is activated when the voltage on OVP with respect to GND exceeds 1.23V. Use the following equation to set the desired overvoltage threshold:

$$V_{OVP} = 1.23\frac{\left(R_{OVP1} + R_{OVP2}\right)}{R_{OVP2}}$$

Inductor Selection

Boost and Buck-Boost Configurations

Boost and buck-boost configurations are similar in that the total output voltage seen by the inductor is always higher than the input voltage. The difference being that for the boost configuration, the total output voltage is dependent on the total LED voltage, while for the buck-boost configuration, the total output voltage is dependent on the sum of the LED voltage and the input voltage.

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage.

For the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the following equation:

$$D_{MAX} = \frac{\left(V_{LED} + V_D + V_{RCS\_LED} + V_{PFET} - V_{INMIN}\right)}{\left(V_{LED} + V_D + V_{RCS\_LED} + V_{PFET} - V_{NFET} - V_{RCS\_FET}\right)}$$

where:

- V_{LED} is the forward voltage of the LED string
- V_D is the forward drop of rectifier diode D1 (approximately 0.6V)
- V_{RCS_LED} is the voltage across the LED current sense resistor R_{CS_LED} (use 0.2V)
- V_{PFET} is the average drain-to source voltage of MOSFET P1 when it is on (use 0.2V initially)
- V_{INMIN} is the minimum input supply voltage
- V_{NFET} is the average drain-to source voltage of MOSFET N1 when it is on (use 0.2V initially)
- V_{RCS_FET} is the voltage across the NFET current sense resistor R_{CS_FET} (use 0.3V initially)

Actual voltages for the above can be determined once component selection is completed.

In the buck-boost LED driver, the average inductor current is equal to the input current plus the LED current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = \frac{\left(V_{LED} + V_D + V_{RCS\_LED} + V_{PFET}\right)}{\left(\begin{matrix} V_{LED} + V_D + V_{RCS\_LED} + V_{PFET} - \\ V_{NFET} - V_{RCS\_FET} + V_{INMIN} \end{matrix}\right)}$$

with the variables being the same as defined in the calculation of the boost configuration.

For both boost and buck-boost configurations, use the following equations to calculate the maximum average inductor current (IL_{DC_MAX}), peak-to-peak inductor current ripple (ΔIL), and the peak inductor current (IL_{PK}):

$$IL_{DC\_MAX} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL, the peak inductor current is given by:

$$IL_{PK} = IL_{DC\_MAX} + 0.5 \times \Delta IL$$

The inductance value of inductor L_{BOOST} or $L_{BUCK\text{-}BOOST}$ is calculated as:

$$L = \frac{\left(V_{INMIN} - V_{NFET} - V_{RCS\_FET}\right) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where f_{SW} is the switching frequency, V_{INMIN}, V_{NFET}, V_{RCS_FET} and ΔIL are defined above. Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than IL_{PK} at the operating temperature.

High-Side Buck Configuration

In the high-side buck LED driver, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum:

$$D_{MIN} = \frac{\left(V_{LED} + V_D + V_{RCS\_LED}\right)}{\left(V_{INMAX} - V_{NFET} - V_{RCS\_FET} + V_D\right)}$$

where:

- V_{LED} is the forward voltage of the LED string
- V_D is the forward drop of rectifier diode D1 (approximately 0.6V)
- V_{RCS_LED} is the voltage across the LED current sense resistor R_{CS_LED} (use 0.2V)
- V_{INMAX} is the maximum input supply voltage
- V_{NFET} is the average drain-to source voltage of MOSFET N1 when it is on (use 0.2V initially)
- V_{RCS_FET} is the voltage across the NFET current sense resistor R_{CS_FET} (use 0.3V initially)

The maximum peak-to-peak inductor ripple (ΔIL) occurs at the maximum input line. The peak inductor current is given by:

$$IL_{PK} = I_{LED} + 0.5 \times \Delta IL$$

The inductance value of inductor L_{BUCK} is calculated as:

$$L_{BUCK} = \frac{\left(V_{INMIN} - V_{NFET} - V_{RCS\_FET}\right) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where f_{SW} is the switching frequency, V_{INMAX}, V_{NFET}, V_{RCS_FET}, V_{LED}, V_{RCS_LED} and ΔIL are defined above. Choose an inductor that has a minimum inductance greater than the calculated value.

SEPIC, Zeta, and Cuk Configurations

In the SEPIC, zeta, and Cuk converters, there are separate inductors for L1 and L2. Neglecting the drops in the switching MOSFET and diode, the maximum duty cycle (D_{MAX}) occurs at low line and is given by:

$$D_{MAX} = \frac{V_{LED}}{\left(V_{INMIN} + V_{LED}\right)}$$

where V_{LED} is the LED string voltage and V_{INMIN} is the minimum input voltage. If the desired maximum input current ripple is ΔIL_{IN}, then the inductor value of L1 is given by:

$$L1 = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} \times \Delta IL_{IN}}$$

The peak inductor current in L1 is IL_{INPK} and is given by:

$$IL_{INPK} = I_{LED}\frac{D_{MAX}}{\left(1 - D_{MAX}\right)} + 0.5 \times \Delta IL_{IN}$$

To account for current transients, the peak saturation rating of the inductor should be 1.2 times the calculated value above.

The average output current in inductor L2 is the same as the LED current. The desired maximum peak-to-peak output current ripple is ΔIL_{OUT}. The value of the inductor L2 is given by:

$$L2 = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} \times \Delta IL_{OUT}}$$

The peak inductor current in L2 is IL_{OUTPK} and is given by:

$$IL_{OUTPK} = I_{LED} + 0.5 \times \Delta IL_{OUT}$$

Slope Compensation

Slope compensation should be added to converters with peak current-mode-control operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and subharmonic oscillations. The minimum amount of slope compensation required for stability is:

$V_{SLOPE(MIN)}$ = 0.5 x (inductor current downslope - inductor current upslope) x R_{CS_FET}

In the MAX25611A/B/C/D, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a resistor (R_{SLOPE}) from CS to the switch current-sense resistor terminal for programming the amount of slope compensation.

The device generates a current ramp with a slope of 50µA/t_{OSC} for slope compensation. The current-ramp signal is forced into an external resistor (R_{SLOPE}) connected between CS and the source of the external MOSFET, thereby adding a programmable slope-compensating voltage (V_{SLOPE}) at the current-sense input CS. Therefore:

$$dV_{SLOPE})/dt = (R_{SLOPE} \times 50\mu A)/t_{OSC}$$

The slope-compensation voltage that needs to be added to the current signal at minimum line voltage, with margin of 1.5x, is:

Boost configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(V_{LED} - 2 \times V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.5$$

Buck-boost configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.5$$

High-side buck configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(2 \times V_{LED} - V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L \times f_{SW}\right)} \times 1.5$$

SEPIC configuration:

$$V_{SLOPE} = D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right) \times R_{CS\_FET}}{\left(2 \times L_{SEPIC} \times f_{SW}\right)} \times 1.5$$

where L_{SEPIC} = SQRT (L1 x L2) where L1 and L2 are the two inductors in the SEPIC configuration.

MOSFET Current-Sense Resistor

The minimum value of the peak current-limit comparator is 0.388V. The current-sense resistor value is given by:

$$R_{CS\_FET} = (0.388 - D_{MAX} \times V_{SLOPE})/IL_{PK}$$

where IL_{PK} is the peak inductor current that occurs at low line in the boost, SEPIC, and buck-boost configurations.

For boost configuration:

$$R_{CS\_FET} = \frac{0.388}{\left[IL_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - 2V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

For buck-boost configuration:

$$R_{CS\_FET} = \frac{0.388}{\left[IL_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right)}{L \times f_{SW}}\right]}$$

For SEPIC configuration:

$$R_{CS\_FET} = \frac{0.388}{\left[IL1_{PK} + IL2_{PK} + 0.75D_{MAX}\frac{\left(V_{LED} - V_{INMIN}\right)}{f_{SW}\sqrt{(L1 \times L2)}}\right]}$$

Input Capacitor

The input-filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply.

The ESR, ESL, and bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter. For the boost configuration, the input current is the same as the inductor current. For buck-boost configuration, the input current is the inductor current minus the LED current. However, for both configurations, the ripple current that the input filter capacitor has to supply is the same as the inductor ripple current with the condition that the output filter capacitor should be connected to ground for buck-boost configuration. Neglecting the effect of LED current ripple, the calculation of the input capacitor for boost, as well as buck-boost configurations is the same. Neglecting the effect of the ESL, ESR, and bulk capacitance at the input contributes to the input-voltage ripple. For simplicity, assume that the contribution from the ESR and the bulk capacitance is equal. This allows 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{IN} = \frac{\Delta IL}{4 \times f_{SW} \times \Delta V_{IN}}$$

The remaining 50% of allowable ripple is for the ESR of the output capacitor.

Use X7R ceramic capacitors for optimal performance. The selected capacitor should have the minimum required capacitance at the operating voltage.

In the buck mode, the input capacitor has large pulsed currents due to the current flowing in the freewheeling diode when the switching MOSFET is off. It is very important to consider the ripple-current rating of the input capacitor in this application.

Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

Boost and Buck-Boost Configurations

The calculation of the output capacitance is the same for both boost and buck-boost configurations. The output ripple is caused by the ESR and bulk capacitance of the output capacitor if the ESL effect is considered negligible. For simplicity, assume that the contributions from ESR and bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{OUT} = \frac{I_{LED} \times 2 \times D_{MAX}}{VOUT_{RIPPLE} \times f_{SW}}$$

The remaining 50% of allowable ripple is for the ESR of the output capacitor.

Based on this, the ESR of the output capacitor is given by:

$$ESR_{COUT} = \frac{VOUT_{RIPPLE}}{IL_{PK} \times 2}$$

Rectifier Diode Selection

Use a Schottky diode as the rectifier (D1) for fast switching and to reduce power dissipation. Select a Schottky diode with a voltage rating higher than that calculated by the following equations:

Boost configuration:

$$V_{D(KA)} \geq (V_{LED} + V_D + V_{RCS\_LED} + V_{PFET}) \times 1.2$$

Buck-boost configuration:

$$V_{D(KA)} \geq (V_{LED} + V_{INMAX} + V_D + V_{RCS\_LED} + V_{PFET}) \times 1.2$$

where $V_{D(KA)}$ is the diode cathode to anode voltage rating. The factor 1.2 provides 20% safety margin.

The current rating of the diode should be greater than I_D in the following equation:

$$I_D \geq IL_{DCMAX} (1 - D_{MAX}) \times 1.5$$

where IL_{DCMAX} is the average inductor current at V_{INMIN}. The factor 1.5 provides 50% safety margin.

Switching MOSFET Selection

The switching MOSFET (N1) should have a voltage rating sufficient to withstand the maximum output voltage together with the diode drop of rectifier diode D1, and any possible overshoot due to ringing caused by parasitic inductances and capacitances. Use a MOSFET with a drain-to-source voltage rating higher than that calculated by the following equations:

Boost configuration:

$$V_{DS} = (V_{LED} + V_D + V_{RCS\_LED} + V_{PFET}) \times 1.2$$

Buck-boost configuration:

$$V_{DS} = (V_{LED} + V_{INMAX} + V_D + V_{RCS\_LED} + V_{PFET}) \times 1.2$$

The factor 1.2 provides 20% safety margin.

Dimming MOSFET Selection

Select a dimming MOSFET (P1) with continuous current rating at the operating temperature higher than the LED current by 30%. The drain-to-source voltage rating of the dimming MOSFET must be higher than V_{LED} by 20%.

Feedback Compensation

The LED current-control loop comprising the switching converter, LED current amplifier, and the error amplifier should be compensated for stable control of the LED current. The switching converter small-signal transfer function has a right half-plane (RHP) zero for both boost and buck-boost configurations, as the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

Buck-boost configuration:

$$f_{ZRHP} = \frac{\left(V_{LED} + V_{INMIN}\right) \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

The switching converter small-signal transfer function also has an output pole for both boost and buck-boost configurations. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = \frac{\left(R_{LED} + R_{CS\_LED}\right) \times V_{LED}}{\left(R_{LED} + R_{CS\_LED}\right) \times I_{LED} + V_{LED}}$$

Buck-boost configuration:

$$R_{OUT} = \frac{\left(R_{LED} + R_{CS\_LED}\right) \times V_{LED}}{\left(R_{LED} + R_{CS\_LED}\right) \times I_{LED} \times D_{MAX} + V_{LED}}$$

where R_{LED} is the dynamic impedance of the LED string at the operating current.

The output pole frequency for both boost and buck-boost configurations is calculated as follows:

$$f_P = \frac{1}{2\pi R_{OUT} C_{OUT}}$$

The feedback-loop compensation is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to GND. R_{COMP} is chosen to set the highfrequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$f_C = 0.2 \times f_{ZRHP}$$

The value of R_{COMP} and C_{COMP} can be calculated as:

$$R_{COMP} = \frac{2 \times f_{ZRHP} \times R_{CS\_FET}}{f \times (1 - D_{MAX}) \times R_{CS\_LED} \times 5 \times G_M}$$

$$C_{COMP} = \frac{25}{\pi \times f_{ZRHP} \times R_{COMP}}$$

PCB Layout

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dV/dt source; therefore, minimize the surface area of the heatsink as much as is compatible with the MOSFET power dissipation, or shield it. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short:

   a) The anode of D1 must be connected very close to the drain of MOSFET N1.

   b) The cathode of D1 must be connected very close to C_{OUT}.

   c) C_{OUT} and current-sense resistor R_{CS_FET} must be connected directly to the ground plane.
4) Connect the power GND of the high current switching components to a star-point configuration.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
6) Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB GND plane as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.

Voltage Regulator Configuration

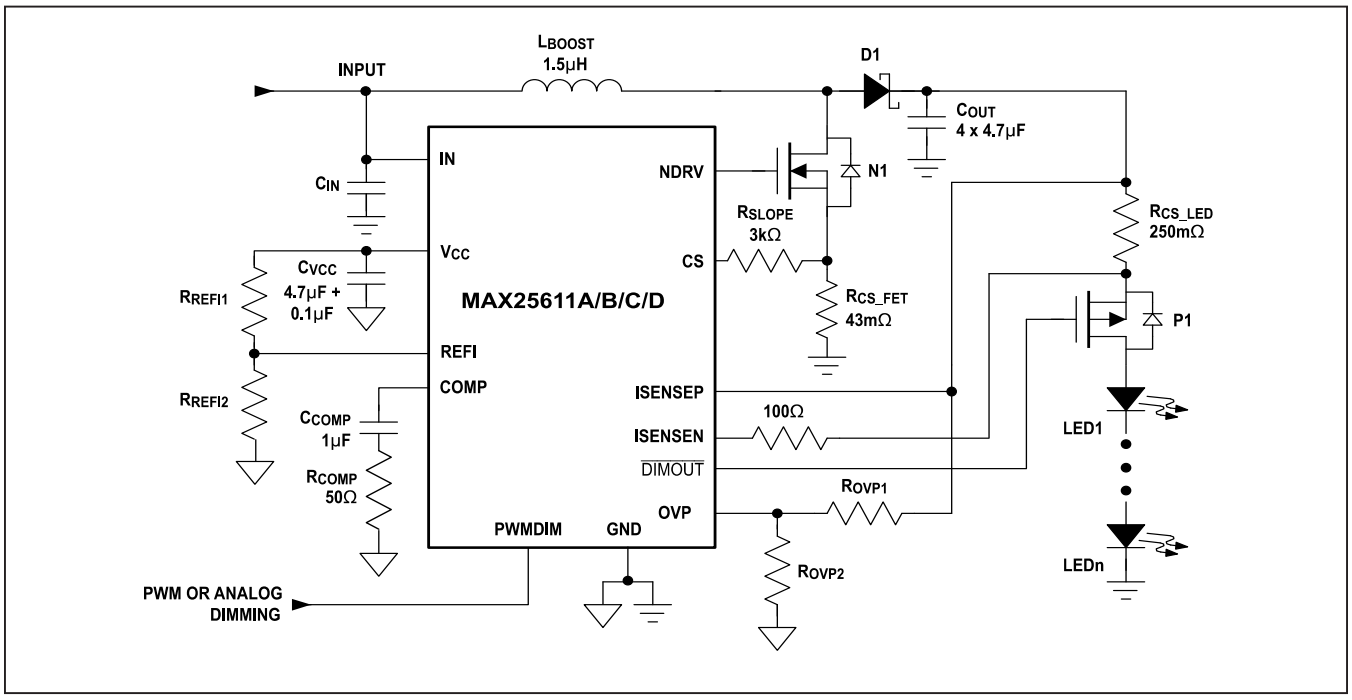
The MAX25611A/B/C/D can be configured as voltage regulators by using the voltage across ISENSEP and ISENSEN as the feedback input for the output voltage feedback divider.

$$V_{OUT} = \frac{\left(V_{REFI} - 0.2\right)}{5} \times \frac{\left(R_{VOUT1} + R_{VOUT2}\right)}{R_{VOUT1}}$$

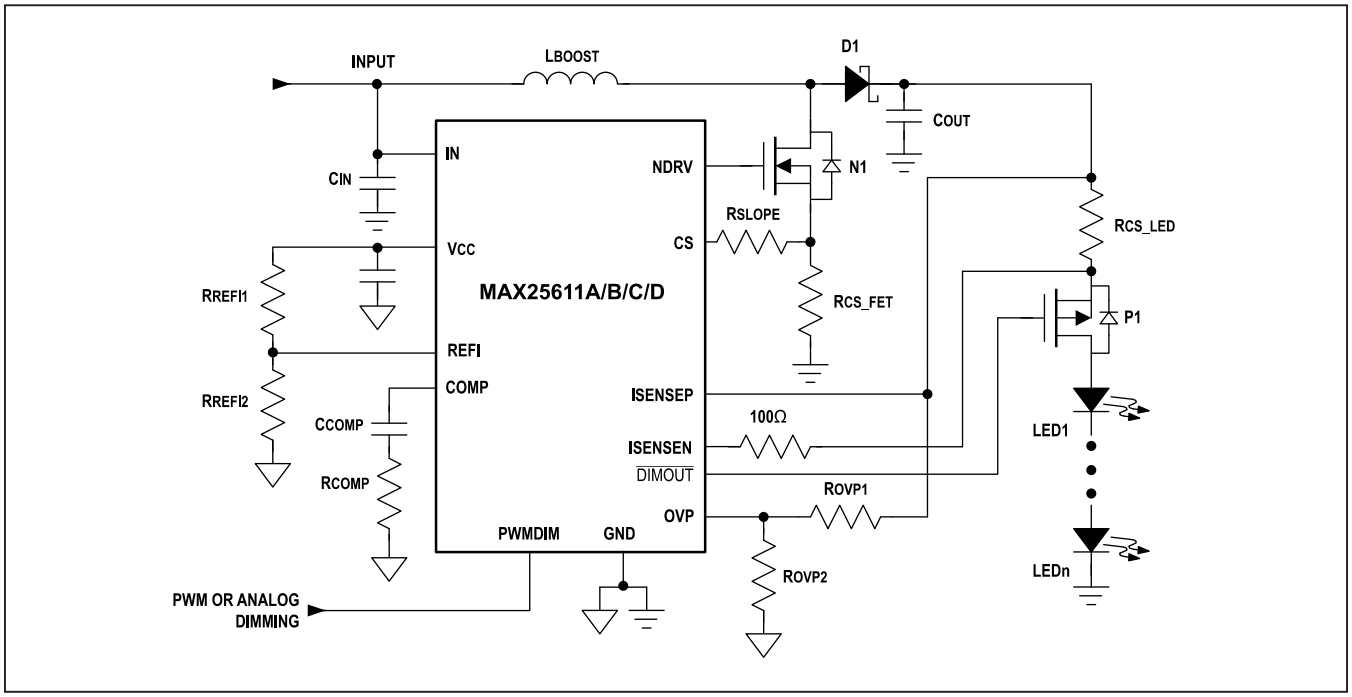
Setting V_{REFI} = 1.2V selects a large feedback signal that improves accuracy and noise immunity.

Typical Application Circuits

Typical Operating Circuit

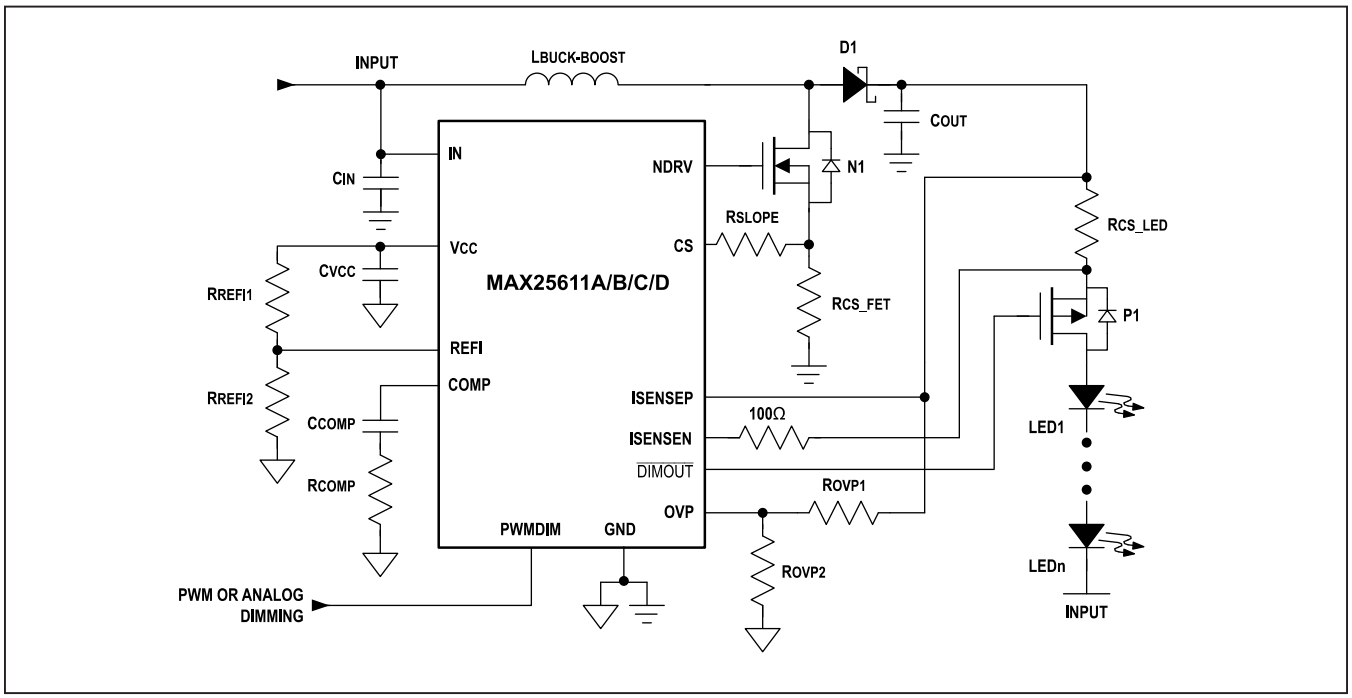


Typical Boost Application Circuit

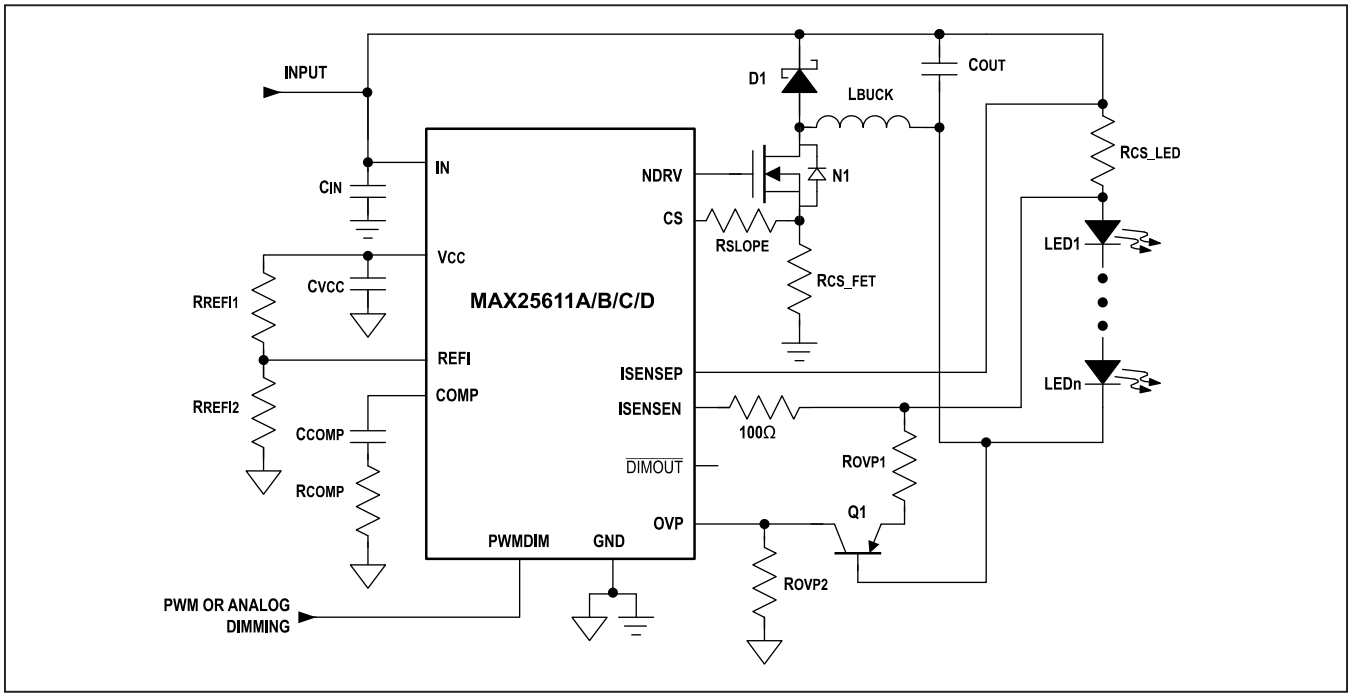


Typical Application Circuits (continued)

Typical Buck-Boost Application Circuit

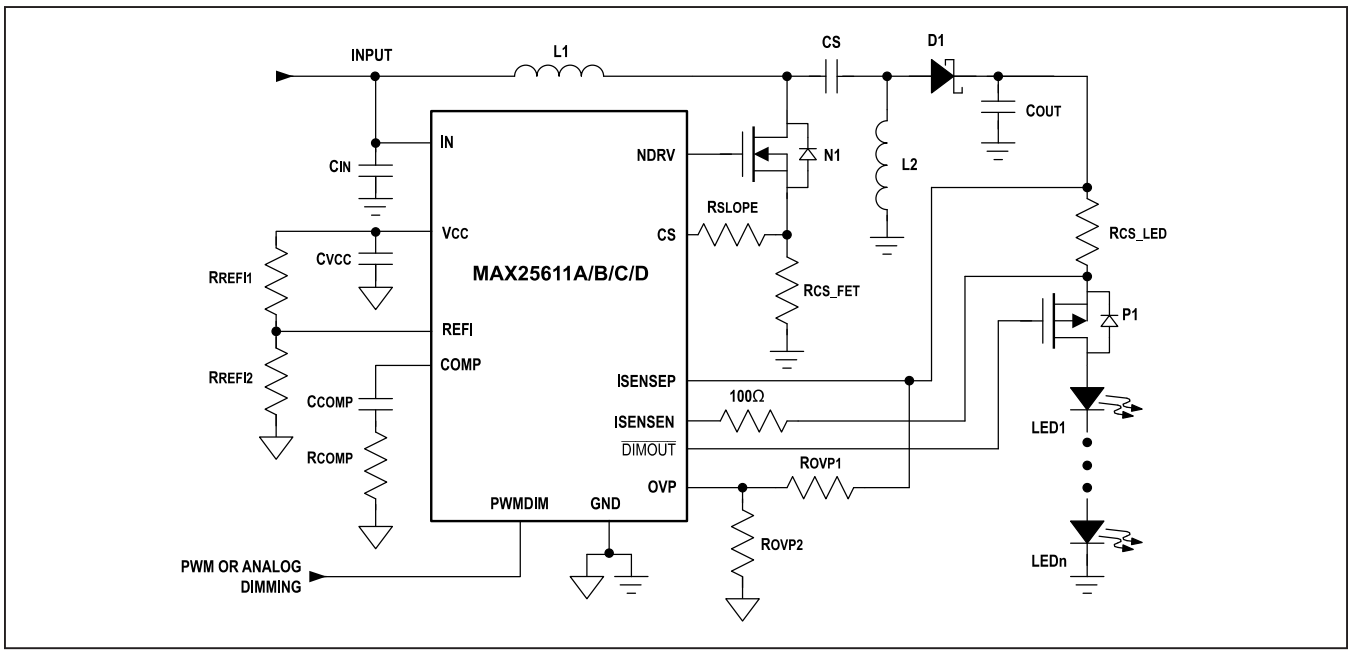


Typical High-Side Buck Application Circuit

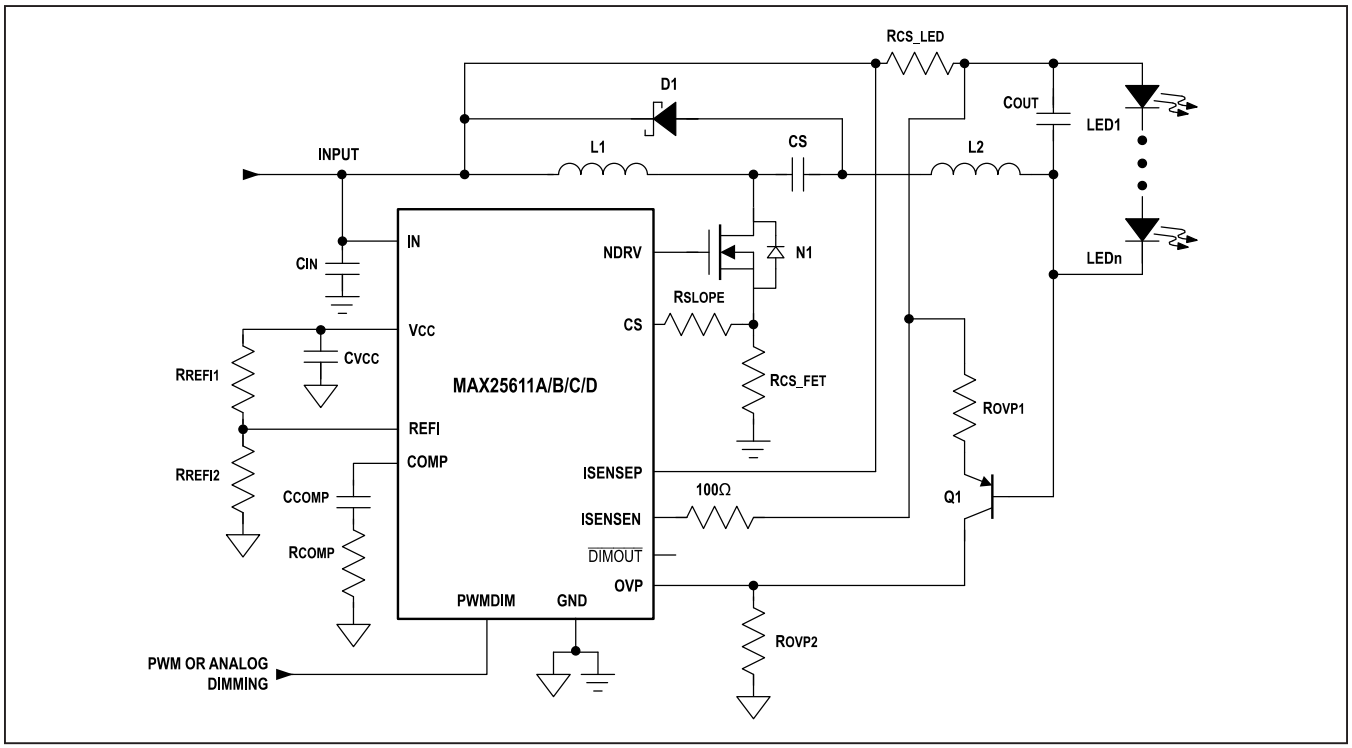


Typical Application Circuits (continued)

Typical SEPIC Application Circuit

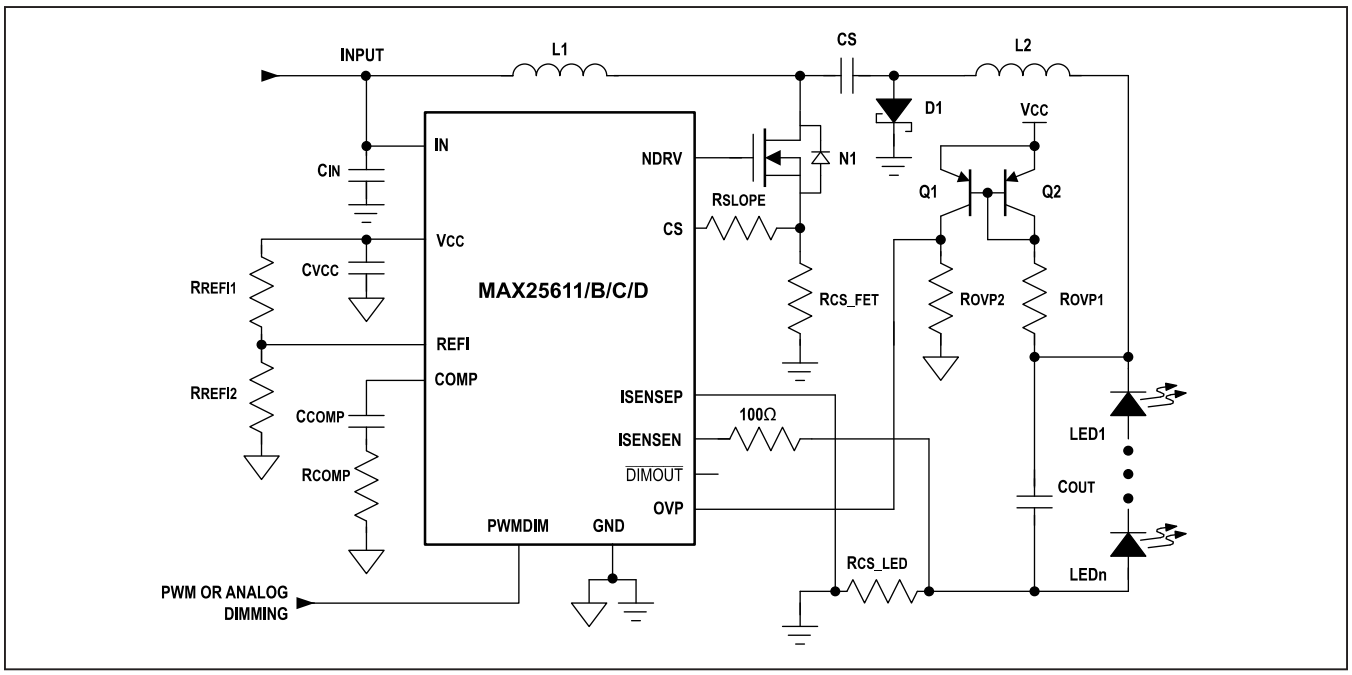


Typical Zeta Application Circuit

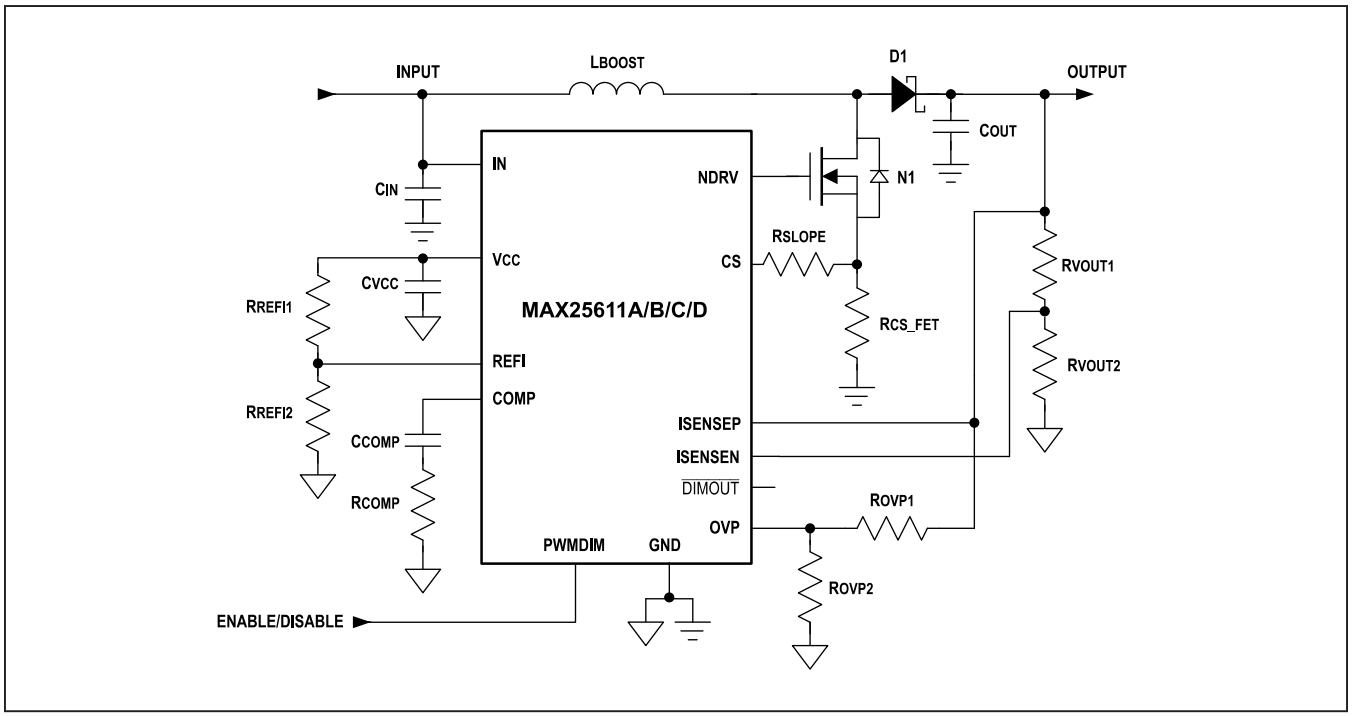


Typical Application Circuits (continued)

Typical Cuk Application Circuit



Typical Voltage Regulator Application Circuit



Ordering Information

PART	PIN-PACKAGE	FEATURE	MAXIMUM V_{IN}
MAX25611AATC/VY+	12 SWTQFN-EP*	350kHz	36
MAX25611AAUD/V+	14 TSSOP	350kHz	36
MAX25611BATC/VY+	12 SWTQFN-EP*	2.2MHz	36
MAX25611BAUD/V+	14 TSSOP	2.2MHz	36
MAX25611CATC/VY+	12 SWTQFN-EP*	350kHz	48
MAX25611CAUD/V+	14 TSSOP	350kHz	48
MAX25611DATC/VY+	12 SWTQFN-EP*	2.2MHz	48
MAX25611DAUD/V+	14 TSSOP	2.2MHz	48

Note: *All parts operate over the -40°C to +125°C automotive temperature range.*
/V Denotes an automotive-qualified part.
Y Denotes side-wettable package.
+ Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	1/19	Updated *Simplified Application Circuit*, *Pin Configuration*, *Pin Description*, *Output Short-Circuit Protection*, Figure 1, *Typical Boost Application Circuit*, *Typical Buck-Boost Application Circuit*, *Typical High-Side Buck Application Circuit*, *Typical SEPIC Application Circuit*, *Typical Zeta Application Circuit*, *Typical Cuk Application Circuit*, *Typical Voltage Regulator Application Circuit*, *Ordering Information*, and added *Functional Diagram*	1, 8, 10, 12, 13, 20–24
2	5/19	Updated title to include MAX25611C and MAX25611D; updated *Absolute Maximum Ratings, Package Information, Electrical Characteristics, Pin Configuration, Pin Description, Detailed Description,* and *Ordering Information*	1–24
3	8/19	Removed future product status from *Ordering Information*	24

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