ADS7869

Analog Motor Control Front-End with Simultaneous Sampling on Seven S/H Capacitors and Three 1MSPS, 12-Bit, 12-Channel ADCs

Data Manual

Literature Number: SBAS253E
May 2003 − Revised July 2006

TEXAS INSTRUMENTS

Contents

List of Illustrations

List of Tables

Analog Motor Control Front-End with Simultaneous Sampling on Seven S/H Capacitors and Three 1MSPS, 12-Bit, 12-Channel ADCs

ADS7869

SBAS253E − MAY 2003 − REVISED JULY 2006

FEATURES

- **Seven Simultaneously-Sampling Sample-and-Hold (S/H) Capacitors**
- **Fully Differential Inputs**
- **Flexible Digital Interface with Four Modes**
  - **One Mode 100% Software-Compatible to VECANA01**
  - **SPI and Two Parallel Modes**
- **Two Up−Down Counter Modules On-Chip**
- **12-Bit System Gain Adjustment for Every Channel**
- **12-Bit Accurate System Offset Adjustment for Every Channel**

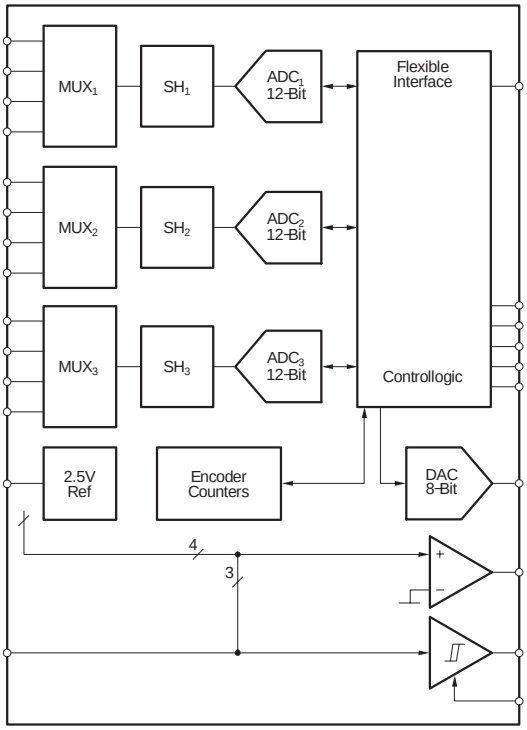
APPLICATIONS

- **Motor Control**

DESCRIPTION

The ADS7869 is a motor control front-end that includes three analog-to-digital converters (ADCs) with a total of seven sample-and-hold capacitors and 12 fully differential input channels. There are four sign comparators connected to four input channels. There are also three additional fully differential inputs; each input is connected to a window comparator and a sign comparator.

In addition, the ADS7869 also offers a very flexible digital interface with a parallel port that can be configured to different standards. Furthermore, a serial peripheral interface (SPI) and a specialized serial interface with three data lines (VECANA01 mode) are provided. This allows the ADS7869 to interface with most digital signal processors (DSPs) or microcontrollers. The chip is specialized for motor-control applications. For the position sensor analysis, two up−down counters are added on the silicon. This feature ensures that the analog input of the encoder is held at the same point of time as the counter value.



1.1 ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7869I	±2	11	TQFP-100	PZT	−40°C to +85°C	ADS7869IPZT	Tray, 90
						ADS7869IPZTR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data manual.

1.2 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS7869I	UNIT
Supply voltage, AV_{DD} to AGND	−0.3 to 6	V
Supply voltage, BV_{DD} to BGND	−0.3 to 6	V
Analog input voltage with respect to AGND	AGND – 0.3 to AV_{DD} + 0.3	V
Reference input voltage with respect to AGND	AGND – 0.3 to AV_{DD} + 0.3	V
Digital input voltage with respect to BGND	BGND – 0.3 to BV_{DD} + 0.3	V
Ground voltage difference AGND to BGND	± 0.3	V
Input current to any pin except supply	−10 to +10	mA
Operating virtual junction temperature range, T_J	−40 to +150	°C
Operating free-air temperature range, T_A	−40 to +85	°C
Storage temperature range, T_{STG}	−65 to +150	°C
Lead temperature 1,6mm (1/16-inch) from case for 10 seconds	+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1.3 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage, AGND to AV_{DD}		4.5	5	5.5	V
Supply Voltage, BGND to BV_{DD}	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Reference Input Voltage		2.475	2.5	2.525	V
Analog Inputs (also see *Fully DIfferential Analog Inputs* section)	+IN – (−IN)	−REF_ADC		+REF_ADC	V
Operating junction temperature range, T_J		−40		+85	°C

1.4 PACKAGE DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	PZT	3.5°C/W	45°C/W	22.222mW/°C	2778mW	1778mW	1444mW
High-K(2)	PZT	3.5°C/W	2.82°C/W	35.461mW/°C	4433mW	2837mW	2305mW

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

1.5 ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

PARAMETER	CONDITION	ADS7869I MIN	ADS7869I TYP(1)	ADS7869I MAX	UNIT
Resolution		12			Bit
Analog Input					
Full-scale Voltage, Differential	See Gain Adjustment	−REF_ADC		+REF_ADC	V
Input Capacitance			10		pF
Input Leakage Current			±1		nA
CMRR	At DC		64		dB
DC Accuracy					
No Missing Codes		11			Bit
INL Integral Linearity Error			±1	±2.5	LSB
DNL Differential Linearity Error			±0.65	±2	LSB
V_{OS} Bipolar Offset Error	Synchronous Channels		2	±6	LSB
V_{OS} Bipolar Offset Error	AX and BX Channels		5	±8	LSB
V_{OS} Bipolar Offset Match	IU, IV, and IW Channels		2.5	6	LSB
V_{OS} Bipolar Offset Match	A1, B1, A2, and B2 Channels		0.5	3	LSB
V_{OS} Bipolar Offset Match	AX and BX Channels		0.5	3	LSB
TCV_{OS} Bipolar Offset Error Drift			1		µV/°C
Gain Error	Max Input Range, Related to REFIN		0.05	1	%
Gain Error	Every Other Input Range		1.5	4	%
Gain Error Drift	Max Input Range, Related to REFIN		3		ppm/°C
PSRR Power-Supply Rejection Ratio	$4.5V < AV_{DD} < 5.5V$		70		dB
Sampling Dynamics					
t_{CONV} Conversion Time per ADC	$16MHz \le f_{CLK} \le 1MHz$	0.75		12	µS
t_{AQ} Acquisition Time		250			ns
Throughput Rate				1000	kSPS
Aperture Delay				20	ns
Aperture Delay Matching			1		ns
Aperture Jitter			50		ps
Clock Frequency		1		16	MHz
AC Accuracy					
Total Harmonic Distortion THD	$V_{IN} = \pm 2.5V_{PP}$ at 10kHz		−78		dB
Signal-to-Noise Distortion SNR	$V_{IN} = \pm 2.5V_{PP}$ at 10kHz		71		dB
Signal-to-Noise + Distortion SINAD	$V_{IN} = \pm 2.5V_{PP}$ at 10kHz		70		dB
Digital Inputs(2)					
Logic Family			CMOS		
V_{IH} High-Level Input Voltage		$0.7 \cdot V_{DD}$		BV_{DD} + 0.3	V
V_{IL} Low-Level Input Voltage		−0.3		$0.3 \cdot V_{DD}$	V
I_{IN} Input Current	BV_{DD} to BGND			±50	nA
C_I Input Capacitance			5		pF
Digital Outputs(2)					
Logic Family			CMOS		
V_{OH} High-Level Output Voltage	BV_{DD} = 4.5V, I_{OH} = −100µA	4.44			V
V_{OL} Low-Level Output Voltage	BV_{DD} = 4.5V, I_{OL} = +100µA			0.5	V
I_{OZ} High-Impedance-State Output Current	$V_I = BV_{DD}$ to BGND			±50	nA
C_O Output Capacitance			5		pF
C_L Load Capacitance				30	pF

(1) All values are at T_A = +25°C.
(2) Applies for 5.0V nominal supply: $4.5V < BV_{DD} < 5.5V$.
(3) Applies for 3.0V nominal supply: $2.7V < BV_{DD} < 3.6V$.

1.5 ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

PARAMETER	CONDITION	ADS7869I			UNIT
		MIN	TYP(1)	MAX	
Digital Inputs(3)					
Logic Family			LVCMOS		
V_{IH} High-Level Input Voltage	BV_{DD} = 3.6V	2		BV_{DD} + 0.3	V
V_{IL} Low-Level Input Voltage	BV_{DD} = 2.7V	−0.3		0.8	V
I_{IN} Input Current	V_I = BV_{DD} to BGND			±50	nA
C_I Input Capacitance			5		pF
Digital Outputs(3)					
Logic Family			LVCMOS		
V_{OH} High-Level Output Voltage	BV_{DD} = 2.7V, I_{OH} = −100µA	BV_{DD} − 0.2			V
V_{OL} Low-Level Output Voltage	BV_{DD} = 2.7V, I_{OL} = +100µA			0.2	V
I_{OZ} High-Impedance-State Output Current	V_I = BV_{DD} to BGND			±50	nA
C_O Output Capacitance			5		pF
C_L Load Capacitance				30	pF
Power Supply					
AV_{DD} Analog Supply Voltage		4.5		5.5	V
BV_{DD} Buffer I/O Supply Voltage		2.7		5.5	V
AI_{DD} Analog Supply Current			45	50	mA
BI_{DD} Buffer I/O Supply Voltage			2		mA
Power Dissipation				250	mW
Reference Output					
V_{REF} Reference Output Voltage	−40°C > t > +85°C	2.475	2.500	2.525	V
V_{REF} Reference Output Voltage	at 25°C	2.480	2.500	2.520	V
dV_{REF}/dT Reference Voltage Drift			±20		ppm/°C
PSRR Power-Supply Rejection Ratio			60		dB
I_{OUT} Output Current	DC Current			1	µA
I_{SC} Short-Circuit Current			1		mA
t_{ON} Turn-On Setting Time			100		µs
Reference Input					
V_{IN} Reference Input Voltage		2.475	2.5	2.525	V
Input Resistance			100		MΩ
Input Capacitance			5		pF
Digital-to-Analog Converter					
Resolution		8			Bits
Output Range	I_{OUT} = 0	0		2.49	V
INL Integral Linearity Error				±1	LSB
DNL Differential Linearity Error				±2	LSB
Offset Error			0.5	1	LSB
Full-Scale Error	FS = Internal Reference Voltage − 1LSB			±1	%
I_{OUT} Output Current				0.5	µA
Output Settling Time	to 0.5LSB, no load capacitance		0.2	1	µs
Position Sensor Sign Comparator					
Input Range	Lower Voltage of Differential Inputs	0		AV_{DD} − 1.8	V
Offset Range			±5	±30	mV
Hysteresis			75	100	mV
Delay Time			25	150	ns

(1) All values are at T_A = +25°C.
(2) Applies for 5.0V nominal supply: 4.5V < BV_{DD} < 5.5V.
(3) Applies for 3.0V nominal supply: 2.7V < BV_{DD} < 3.6V.

1.5 ELECTRICAL CHARACTERISTICS (continued)

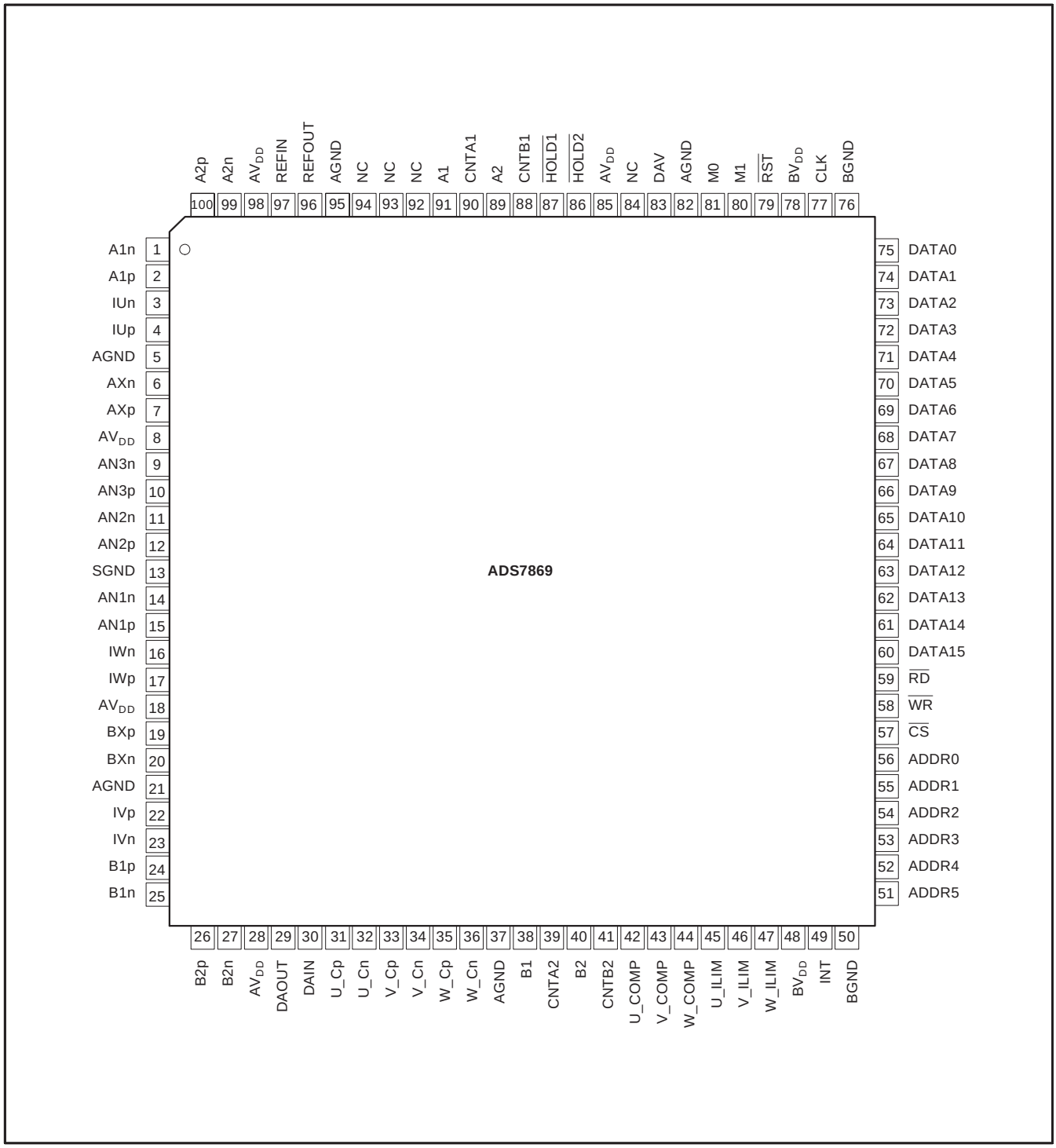
Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

PARAMETER	CONDITION	ADS7869I			UNIT
		MIN	TYP(1)	MAX	
Current Sign Comparator					
Input Range	Lower Voltage of Differential Inputs	0		AV_{DD} − 1.8	V
Offset Range			±2	±20	mV
Hysteresis			10	30	mV
Delay Time			25	150	ns
Window Comparator					
Input Range		−0.3		AV_{DD} + 0.3	V
Offset Range			±10	±30	mV
Hysteresis		60	70	80	mV
Delay Time	f_{CLK} = 16MHz		250	375	ns
Threshold Voltage Input Range	(DAIN pin)	0.5		2.5	V

(1) All values are at T_A = +25°C.
(2) Applies for 5.0V nominal supply: 4.5V < BV_{DD} < 5.5V.
(3) Applies for 3.0V nominal supply: 2.7V < BV_{DD} < 3.6V.

1.6 PINOUT DRAWING

TQFP Package



1.7 PIN FUNCTIONS

TQFP Package

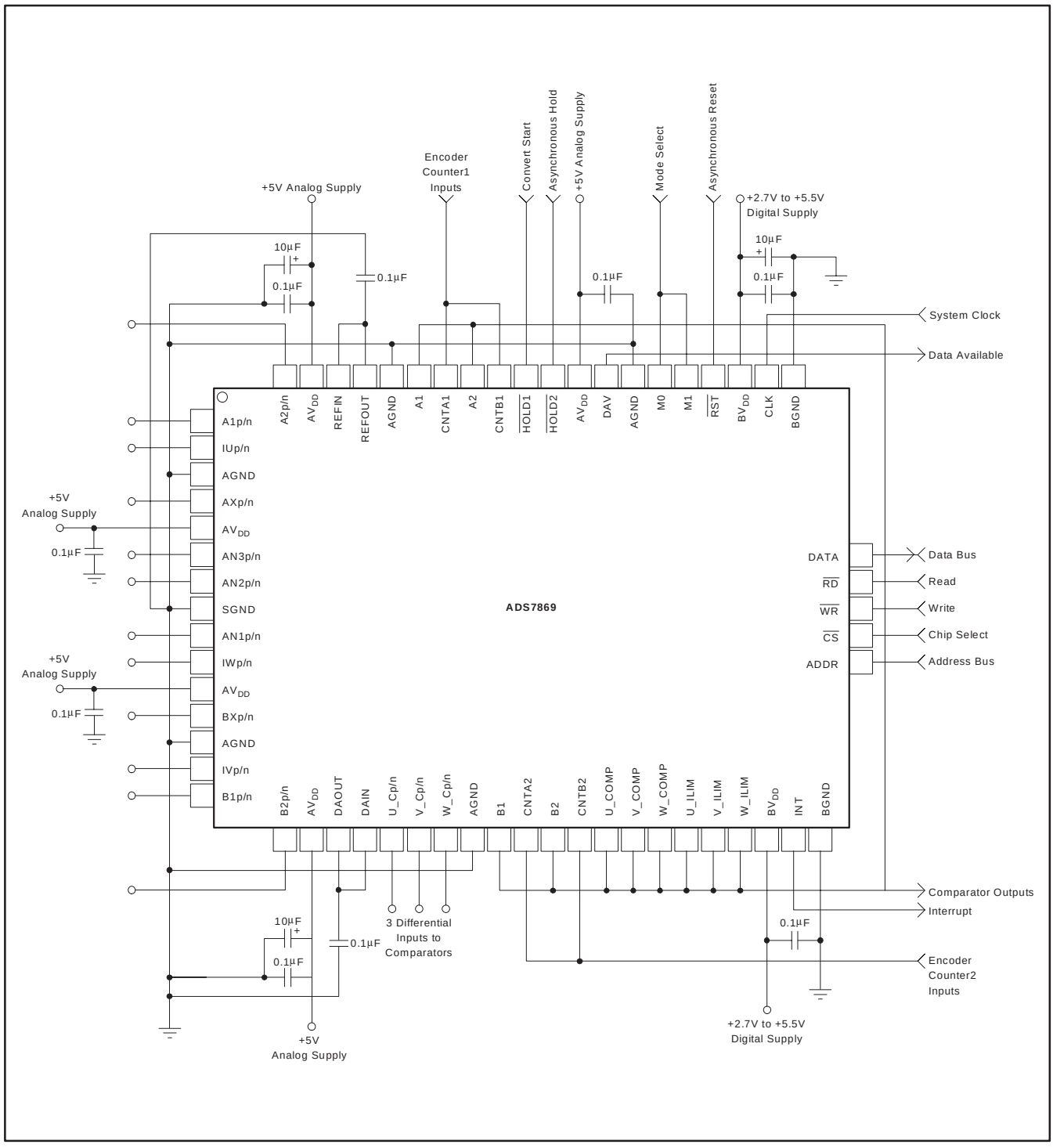
SIGNAL	PIN NUMBER	TYPE	DESCRIPTION
ANALOG SIGNALS			
Analog Input Signals of Position Sensors			
A1p	2	Analog In	Position Sensor 1, Analog Input of SIN, Positive Input
A1n	1	Analog In	Position Sensor 1, Analog Input of SIN, Negative Input
B1p	24	Analog In	Position Sensor 1, Analog Input of COS, Positive Input
B1n	25	Analog In	Position Sensor 1, Analog Input of COS, Negative Input
AXp	7	Analog In	Position Sensor X, Asynchronous Analog Input of SIN, Positive Input
AXn	6	Analog In	Position Sensor X, Asynchronous Analog Input of SIN, Negative Input
A2p	100	Analog In	Position Sensor 2, Analog Input of SIN, Positive Input
A2n	99	Analog In	Position Sensor 2, Analog Input of SIN, Negative Input
B2p	26	Analog In	Position Sensor 2, Analog Input of COS, Positive Input
B2n	27	Analog In	Position Sensor 2, Analog Input of COS, Negative Input
BXp	19	Analog In	Position Sensor X, Asynchronous Analog Input of COS, Positive Input
BXn	20	Analog In	Position Sensor X, Asynchronous Analog Input of COS, Negative Input
Counter Signals of Position Sensors			
A1	91	Digital Out	Sign of SIN Signal, Position Sensor 1
B1	38	Digital Out	Sign of COS Signal, Position Sensor 1
A2	89	Digital Out	Sign of SIN Signal, Position Sensor 2
B2	40	Digital Out	Sign of COS Signal, Position Sensor 2
CNTA1	90	Digital In	Input Signal SIN to 16-bit Up/Down Counter 1
CNTB1	88	Digital In	Input Signal COS to 16-bit Up/Down Counter 1
CNTA2	39	Digital In	Input Signal SIN to 16-bit Up/Down Counter 2
CNTB2	41	Digital In	Input Signal COS to 16-bit Up/Down Counter 2
Analog Input Signals of Phase Currents			
IUp	4	Analog In	Phase U Current, Positive Input
IUn	3	Analog In	Phase U Current, Negative Input
IVp	22	Analog In	Phase V Current, Positive Input
IVn	23	Analog In	Phase V Current, Negative Input
IWp	17	Analog In	Phase W Current, Positive Input
IWn	16	Analog In	Phase W Current, Negative Input

TQFP Package

SIGNAL	PIN NUMBER	TYPE	DESCRIPTION
Comparator Signals of Phase Currents			
DAOUT	29	Analog Out	8-Bit DAC Output for Over-Current Limit Value
DAIN	30	Analog In	Over-Current Limit Value as Input for Window Comparators
U_Cp	31	Analog In	Phase U Current Signal Input for Sign and Window Comparator, Positive Input
U_Cn	32	Analog In	Phase U Current Signal Input for Sign and Window Comparator, Negative Input
V_Cp	33	Analog In	Phase V Current Signal Input for Sign and Window Comparator, Positive Input
V_Cn	34	Analog In	Phase V Current Signal Input for Sign and Window Comparator, Negative Input
W_Cp	35	Analog In	Phase W Current Signal Input for Sign and Window Comparator, Positive Input
W_Cn	36	Analog In	Phase W Current Signal Input for Sign and Window Comparator, Negative Input
U_COMP	42	Digital Out	Sign of Phase U Current
V_COMP	43	Digital Out	Sign of Phase V Current
W_COMP	44	Digital Out	Sign of Phase W Current
U_ILIM	45	Digital Out	Over-current Output of Phase U, Active Low Output
V_ILIM	46	Digital Out	Over-current Output of Phase V, Active Low Output
W_ILIM	47	Digital Out	Over-current Output of Phase W, Active Low Output
Other Analog Signals			
AN(x)p	15, 12, 10	Analog In	Auxiliary Analog Input Channel (x), Positive Input
AN(x)n	14, 11, 9	Analog In	Auxiliary Analog Input Channel (x), Negative Input
REFIN	97	Analog In	Reference Voltage Input Pin
REFOUT	96	Analog Out	Reference Voltage Output Pin
NC	84, 92, 93, 94	—	No connection (should be left open)
DIGITAL INTERFACE SIGNALS			
ADDR(x)	56 – 51	Digital In	Address Decode Input(1)
DATA(xx)	75 – 60	Digital In/Out	Bidirectional 3-state Data Bus(1)
$\overline{CS}$	57	Digital In	Active Low Chip-Select Signal(1)
$\overline{RD}$	59	Digital In	Active Low Read Signal(1)
$\overline{WR}$	58	Digital In	Active Low Write Signal(1)
CLK	77	Digital In	System Clock
INT	49	Digital Out	Active High Interrupt Output
$\overline{RST}$	79	Digital In	Active Low Reset Input
M(x)	81, 80	Digital In	Mode Select Pins(1)
DAV	83	Digital Out	Data Available Signal
$\overline{HOLD1}$	87	Digital In	Active Low Convert Start and Synchronous Hold Signal for Sample-and-Hold Amplifiers
$\overline{HOLD2}$	86	Digital In	Active Low Asynchronous Hold Signal for Sample-and-Hold Amplifiers
POWER SUPPLY			
AV_{DD}	8, 18, 28, 85, 98	Power	Analog Power Supply
BV_{DD}	48, 78	Power	Interface Power Supply
AGND	5, 21, 37, 82, 95		Analog Ground
BGND	50, 76		Interface Ground
SGND	13		Signal Ground

(1) See *Digital* section for detailed information about the different modes.

1.8 BASIC CIRCUIT CONFIGURATION



1.9 TYPICAL APPLICATION CIRCUIT

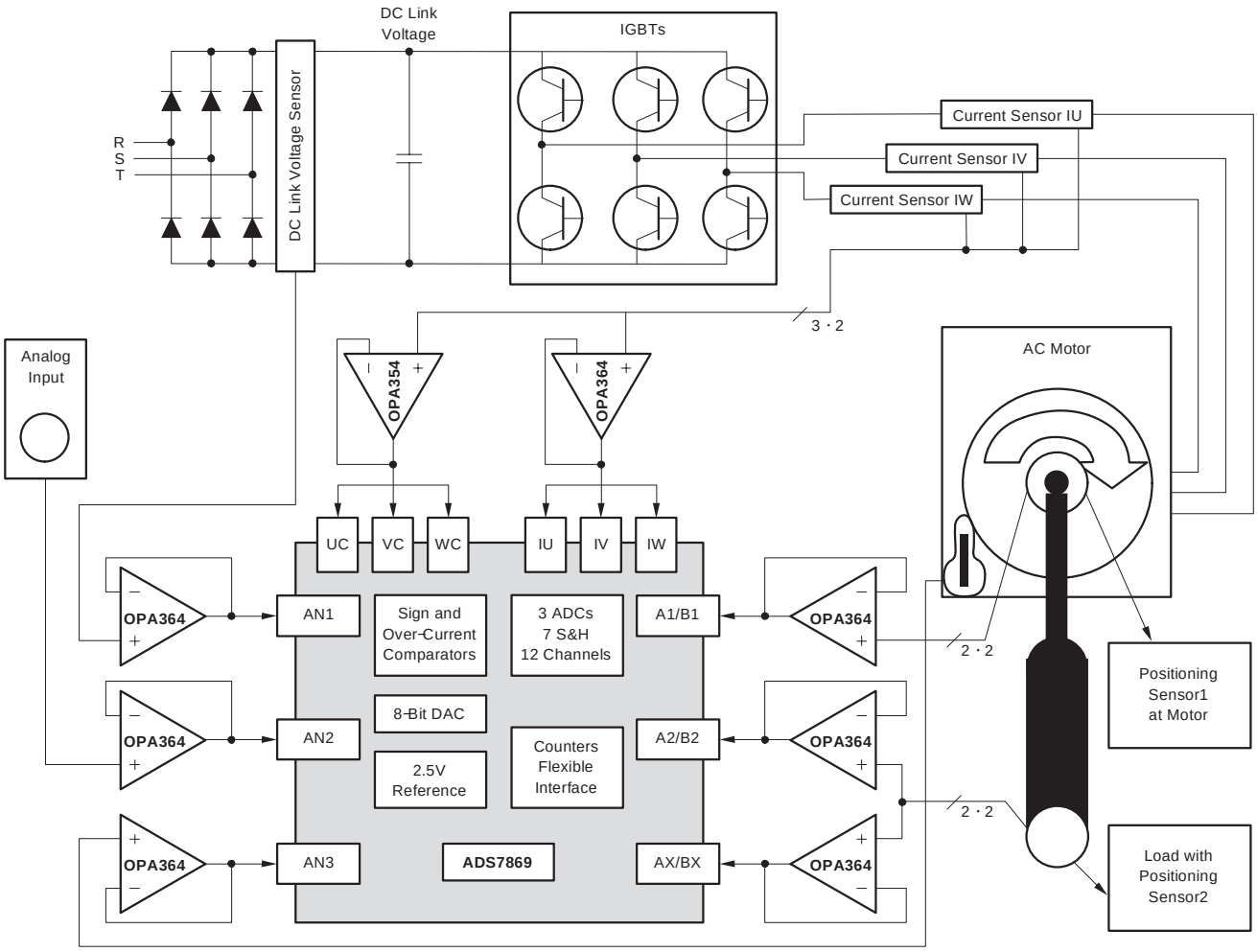


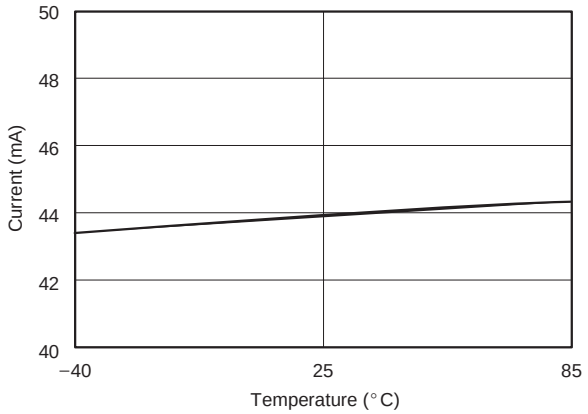
Figure 1−1. Typical Motor Control Application

Figure 1−1 shows an example of a typical motor control circuit. The IU, IV and IW channels measure the currents of the motor. The position (speed) of the motor and load are measured simultaneously by A1, B1 and A2, B2, respectively, using resolver or analog encoder sensors. The asynchronous inputs AX and BX can be used to capture the reference signal of encoders to derive the absolute position. Channel AN1 measures the differential DC link voltage. AN3 measures the temperature of the motor. An auxiliary voltage can be measured with channel AN2. The counter inputs connect to the appropriate comparator outputs (A1 to CNTA1, B1 to CNTB1 and so on). The level input of the window comparators, DAIN, should be connected to the 8-bit DAC output DAOUT.

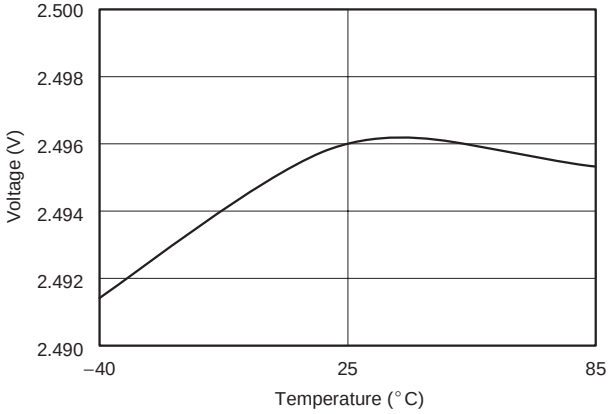
1.10 TYPICAL CHARACTERISTICS

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

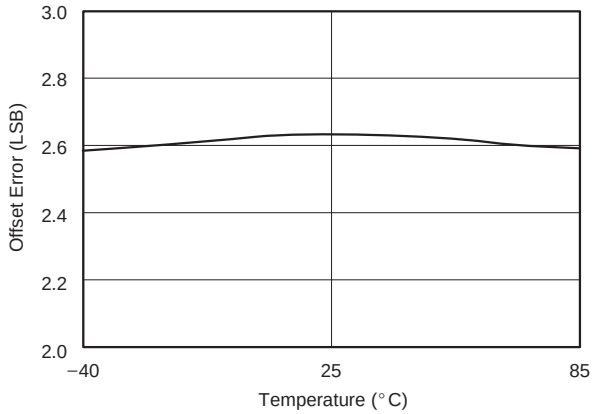
ANALOG SUPPLY CURRENT vs TEMPERATURE



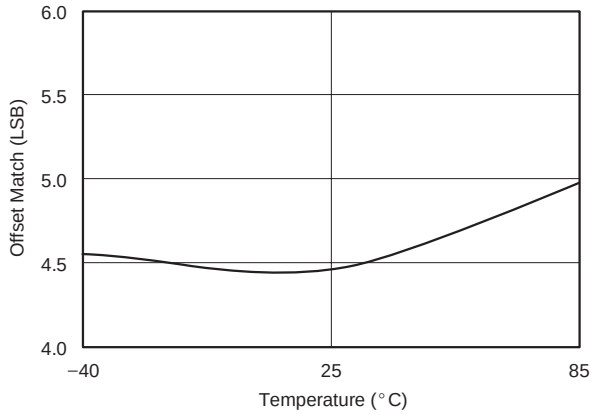
REFERENCE VOLTAGE vs TEMPERATURE



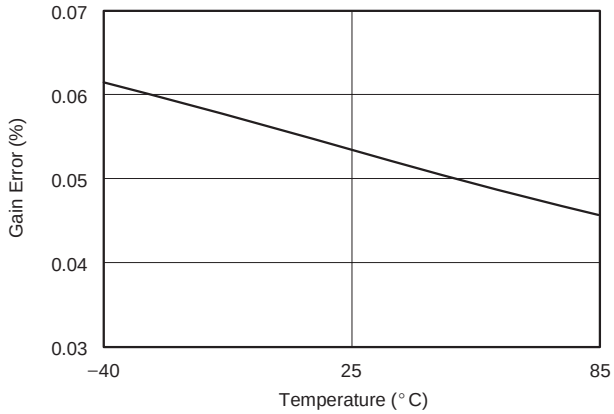
ADC OFFSET ERROR vs TEMPERATURE



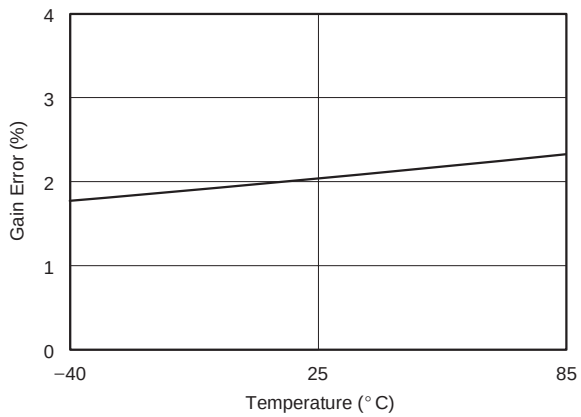
ADC OFFSET MATCH
vs TEMPERATURE FOR ALL CHANNELS



ADC GAIN ERROR AT 1V/V GAIN
vs TEMPERATURE



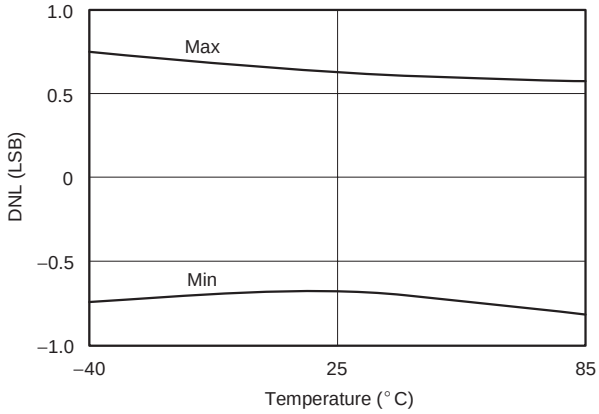
ADC GAIN ERROR AT 5V/V GAIN
vs TEMPERATURE



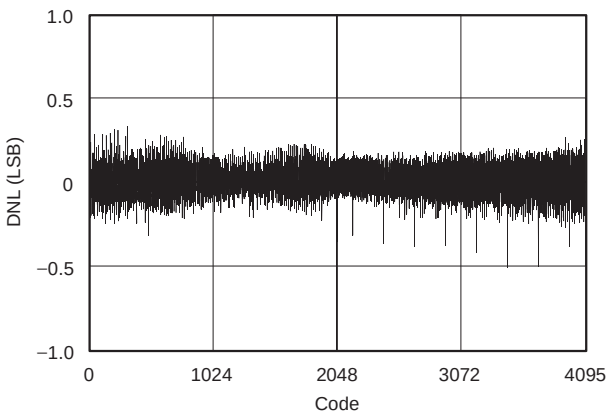
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

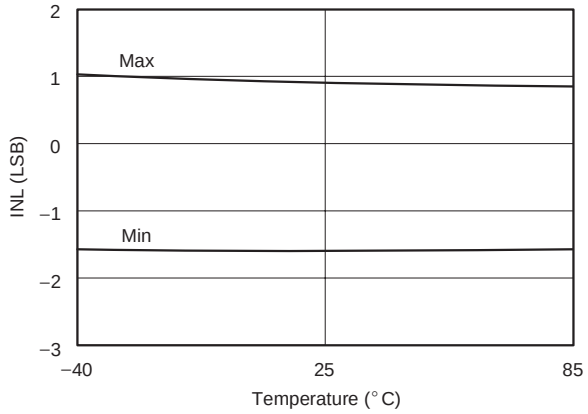
ADC DIFFERENTIAL LINEARITY vs TEMPERATURE



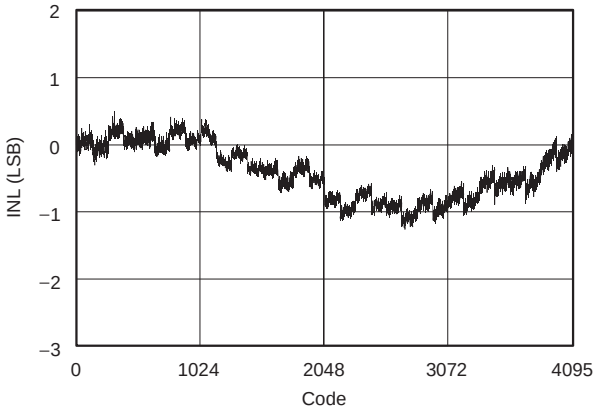
ADC DIFFERENTIAL LINEARITY ERROR vs CODE



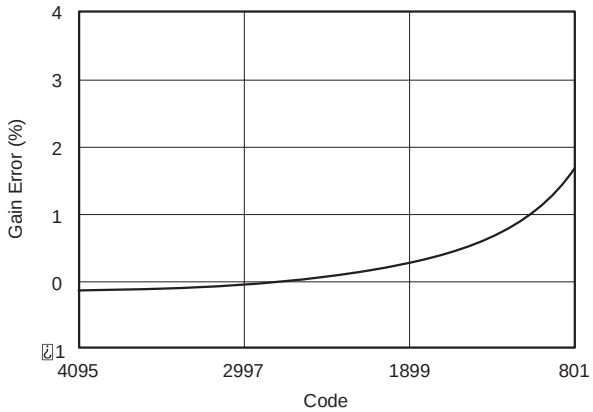
ADC INTEGRAL LINEARITY ERROR vs TEMPERATURE



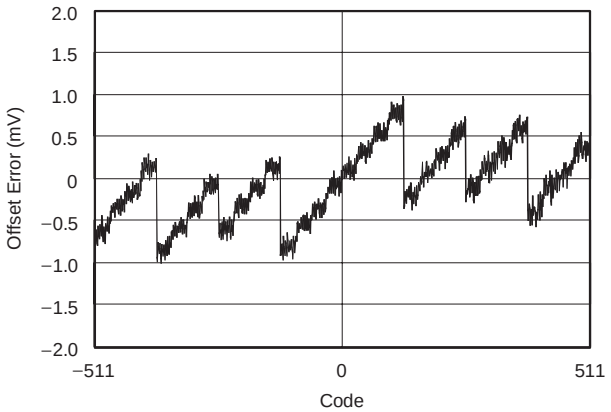
ADC INTEGRAL LINEARITY ERROR vs CODE



GAIN ERROR vs GAIN ADJUSTMENT



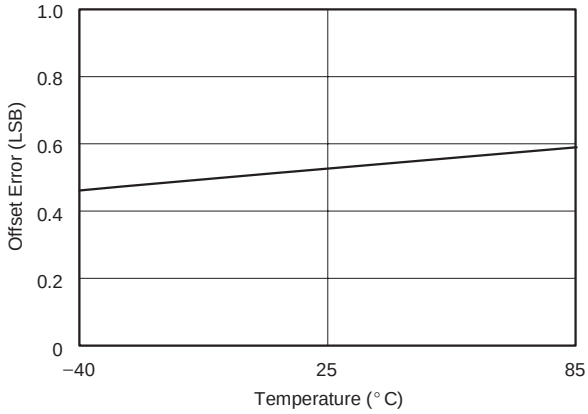
CHANGE IN OFFSET ERROR vs OFFSET ADJUSTMENT



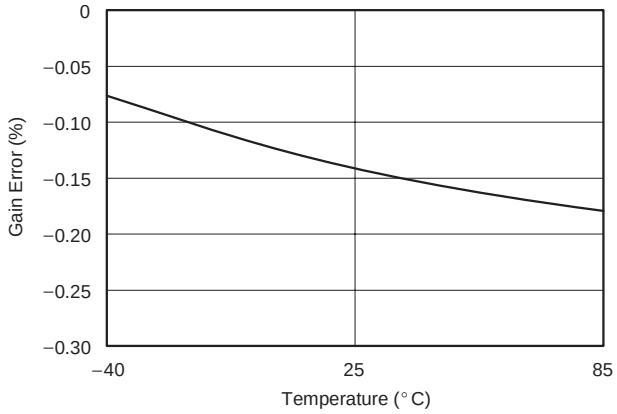
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

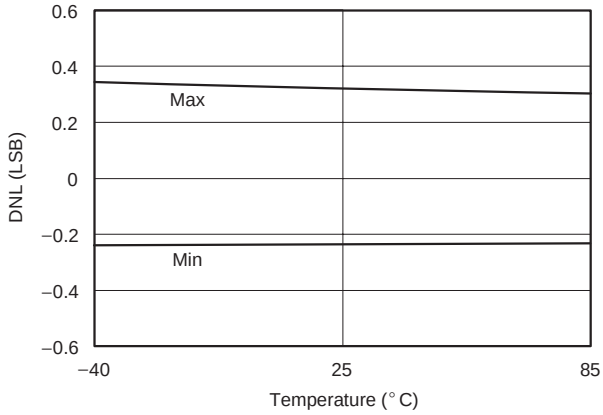
DAC OFFSET ERROR vs TEMPERATURE



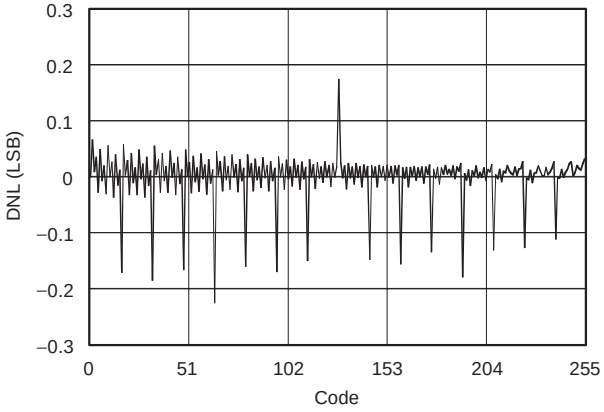
DAC GAIN ERROR vs TEMPERATURE



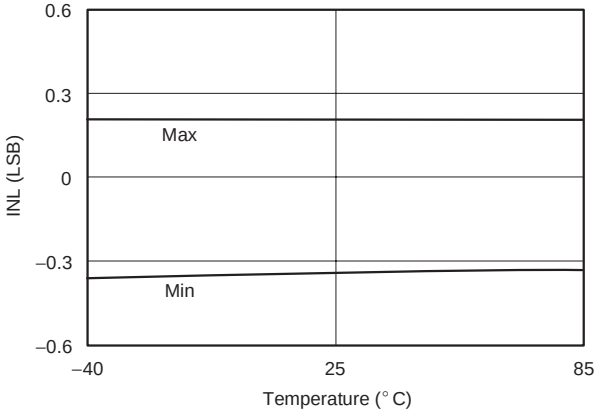
DAC DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



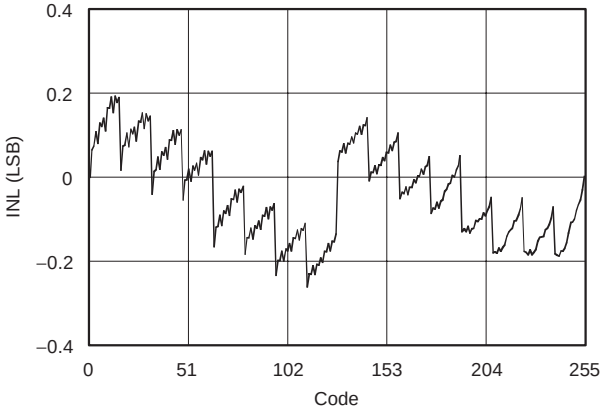
DAC DIFFERENTIAL LINEARITY ERROR vs CODE



DAC INTEGRAL LINEARITY ERROR vs TEMPERATURE



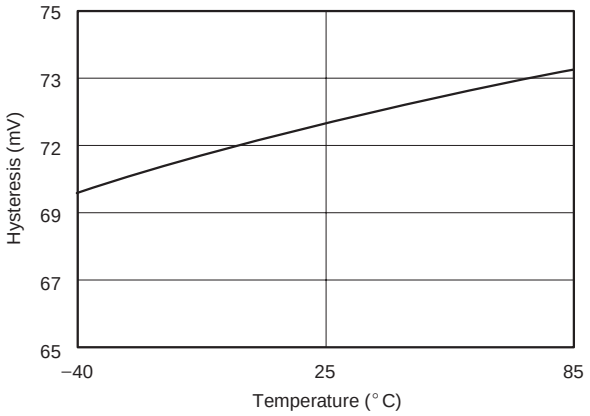
DAC INTEGRAL LINEARITY ERROR vs CODE



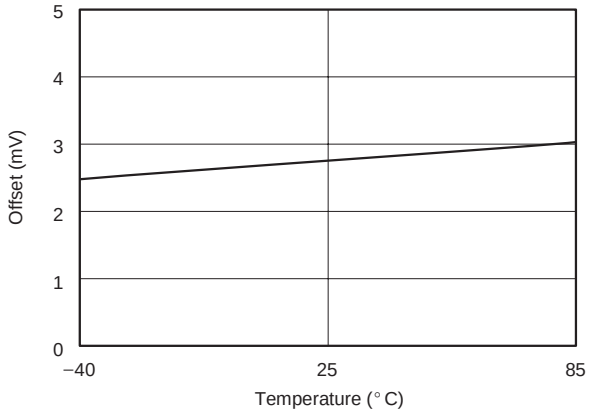
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = internal +2.5V, f_{CLK} = 16MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted.

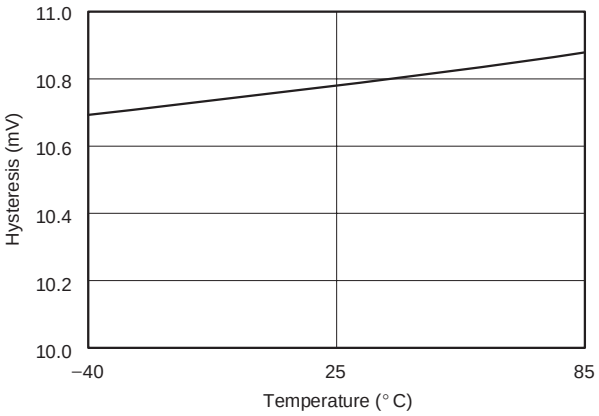
ENCODER COMPARATOR HYSTERESIS vs TEMPERATURE



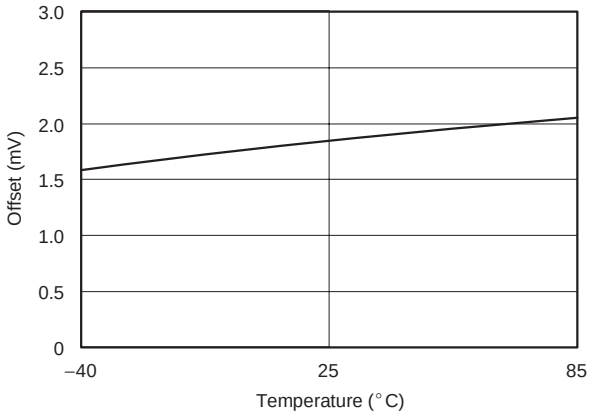
ENCODER COMPARATOR OFFSET vs TEMPERATURE



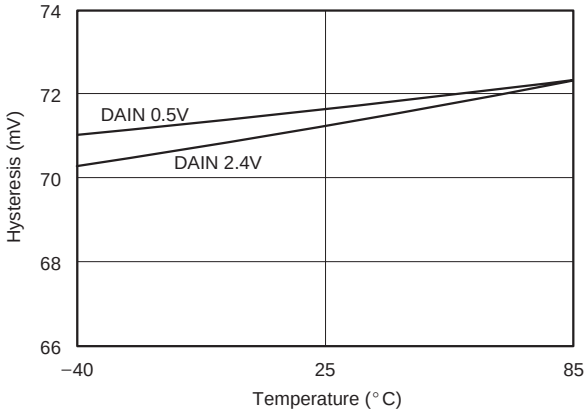
SIGN COMPARATOR HYSTERESIS vs TEMPERATURE



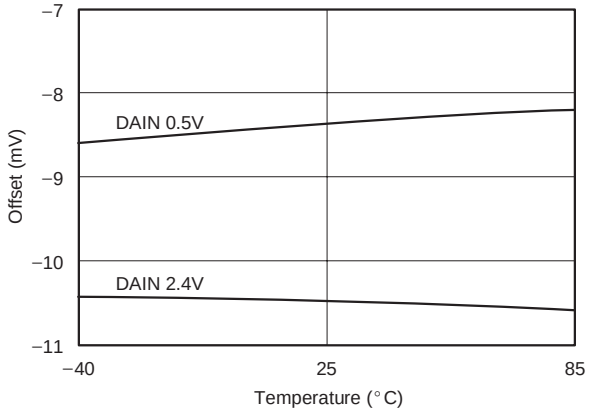
SIGN COMPARATOR OFFSET vs TEMPERATURE



WINDOW COMPARATOR HYSTERESIS vs TEMPERATURE



WINDOW COMPARATOR OFFSET vs TEMPERATURE



1.11 FUNCTIONAL BLOCK DIAGRAM

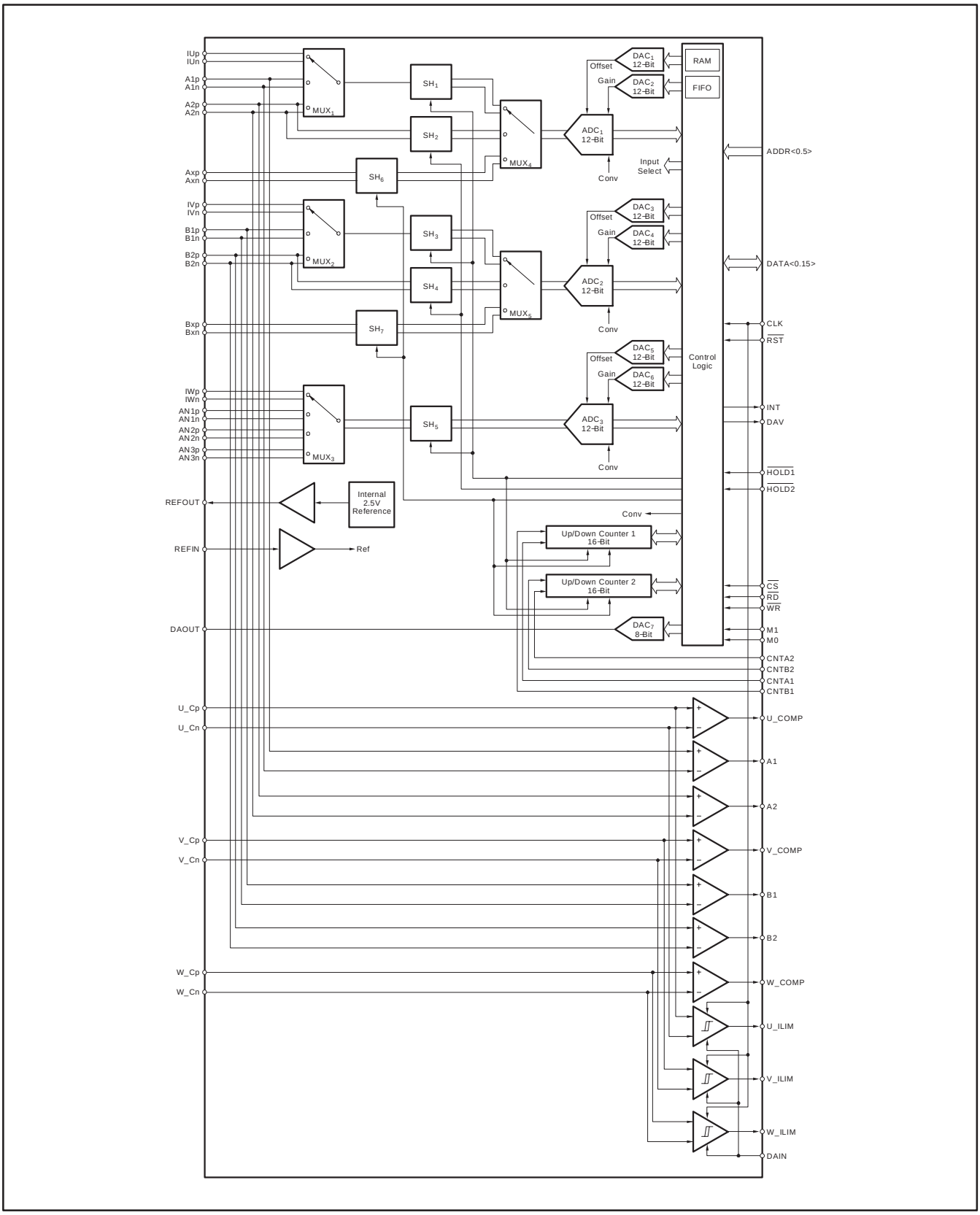


Figure 1−2. Functional Diagram

2 Analog Section

The analog section addresses the Analog-to-Digital Converters, including the gain and offset adjustment. There is also a discussion of the analog inputs, the seven sign comparators, three window comparators, the 8-bit Digital-to-Analog Converter (DAC), the reference voltage, grounding, and the supply voltage.

2.1 Fully Differential Analog Inputs

2.1.1 Analog-to-Digital Converter Inputs

The 12 inputs to the ADCs, as well as the three inputs (U_C, V_C and W_C) to the comparators, are fully differential and provide a good common-mode rejection of 60dB at 50kHz. This is very important to suppress noise in difficult environments.

The seven sample-and-hold circuits from the ADC contain a 5pF capacitor (C_S in Figure 1−3) that is connected via a switch to the analog inputs. Opening the switch holds the data. The switch closes when the conversion is finished. The capacitor is then loaded to an initial voltage that is equal to the reference at the ADC, which is selected with the gain adjustment.

The voltage of the input pin is usually different from the voltage of the sample capacitor when the input switch closes. The sample capacitor needs to be recharged to the 12-bit accuracy, one-half of a least significant bit (LSB), within an acquisition time (t_{AQ}) of at least 200ns.

The minimum −3dB bandwidth of the driving operational amplifier can be calculated to:

$$f_{3db} = \frac{\ln(2) \cdot (n + 1)}{2\pi \cdot t_{AQ}} \quad (1)$$

where *n* is equal to 12, the resolution of the ADC (in the case of the ADS7869). When t_{AQ} = 200ns, the minimum bandwidth of the driving amplifier is 7MHz. The bandwidth can be relaxed if the acquisition time is increased by the application.

The OPA364 from Texas Instruments is recommended; besides the necessary bandwidth, it provides a low offset in a small package at a low price.

The phase margin of the driving operational amplifier is usually reduced by the sampling capacitor of the ADC. A resistor between the capacitor and the amplifier reduces this effect; therefore, an internal 300Ω resistor (R_{SER}) is in series with the switch. The resistance of the closed switch (R_{SW}) is approximately 80Ω. See Figure 1−3.

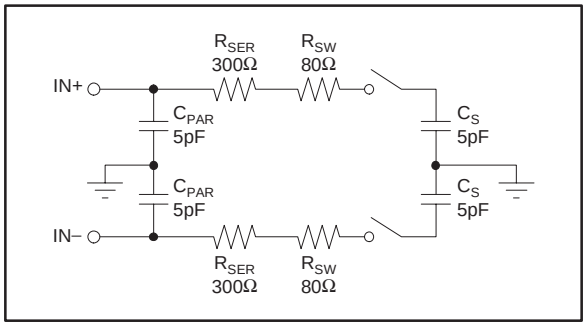


Figure 1−3. Equivalent Input Circuit to the ADCs

The differential input range (positive minus negative input) of the ADC is ±REF_ADC, the reference of the converter, which is selected with the gain adjustment.

It is important that the voltage to all inputs does not exceed more than 0.3V above the analog supply or 0.3V below the ground. There is no DC current flow through the inputs. Current is only necessary when recharging the sample-and-hold capacitors, C_S.

2.1.2 Window Comparator Inputs

A sampling architecture was selected for the window comparators. The sampling time is two clock cycles with a minimum t_{AQ} (see Equation 1) of 125ns. The necessary accuracy is 10mV (see 8-bit DAC section) with a 5V input range. The required bandwidth of the driving amplifier is 8.8MHz (see Equation 1). The OPAx354 from Texas Instruments is recommended.

The input circuit of the window comparator is similar to the ADC inputs. The only difference is that the sampling capacitors are reduced to 2.5pF. (See Figure 1−4.)

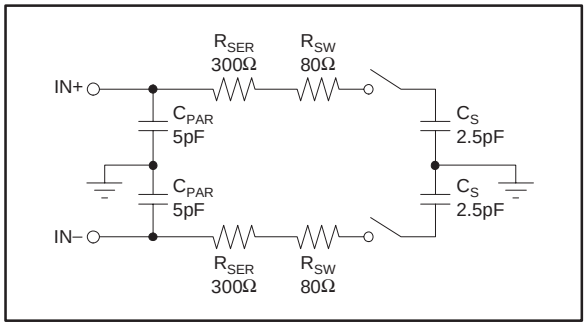


Figure 1−4. Equivalent Input Circuit of the Window Comparators

2.1.3 Sign Comparator Inputs

Four sign comparators are connected to the ADC inputs (A1, B1, A2 and B2); three of the sign comparators are wired to the window comparator inputs (U_C, V_C, and W_C).

The sample capacitors of the ADCs and the window comparators could produce voltage glitches; therefore, it is important to drive the inputs with low impedance.

The lower voltage of the differential input should remain within the range of 0 to AV_{DD}−1.8V.

2.2 Analog-To-Digital Converter

The ADS7869 includes three, SAR-type, 1MSPS, 12-bit ADCs, and three pairs of S/H capacitors, which are each connected to ADC_1 and ADC_2. A single S/H capacitor is connected to ADC_3. Gain and offset adjustments are added to each ADC. (See Figure 1−2 on page 15.)

2.2.1 $\overline{HOLD1}$, $\overline{HOLD2}$

The analog inputs are held when the $\overline{HOLDx}$ signals go low. The charges of the synchronous sample-and-holds (S/H_{1-5}) are frozen on the falling edge of $\overline{HOLD1}$. The setup time of $\overline{HOLD1}$, against the rising edge of the system clock, is typically 25ns. The conversion will automatically start on the next rising edge of the clock. The S/Hs are switched back into the sample mode when the conversion is finished, 12 clock cycles later. This point of time is indicated by DAV. (See Figure 1−10 on page 26.) $\overline{HOLD1}$ must go high at the latest at the 13th falling clock after conversion start.

The asynchronous sample and holds (S/H_{6-7}) are triggered by the active low $\overline{HOLD2}$ signal. The setup time of $\overline{HOLD2}$, against the falling edge of $\overline{HOLD1}$, is 0ns; see Figure 1−10. The conversion of these S/H circuits is initiated when they are selected through the digital interface and the $\overline{HOLD1}$ signal goes low. The inputs are connected back to the S/H capacitor when the $\overline{HOLD2}$ signal goes high. $\overline{HOLD2}$ needs to be low during the whole conversion. It is possible to connect $\overline{HOLD1}$ and $\overline{HOLD2}$ together.

2.2.2 Clock

The ADC uses the external clock CLK, which needs to be in the range of 1MHz to 16MHz. 12 clock cycles are necessary for a conversion, with a minimum of four clock cycles for the acquisition. Therefore, the maximum throughput rate of 1MSPS is achieved with a 16MHz clock and 16 clock cycles per complete conversion cycle. The duty cycle should be 50%; however, the ADS7869 will still function properly with a duty cycle between 30% and 70%.

2.2.3 Reset

A reset condition stops any ongoing conversion and reconnects the synchronous S/Hs to the inputs; see the *Reset* Section.

2.2.4 Gain Adjustment

The output of a 12-bit DAC (REF_ADC) is used as the reference voltage for the ADC. There is one DAC for each ADC. The voltage range is between 0V (code 000_H) and the 2.5V of REFIN (code FFF_H). The ADC operates correctly if the selected voltage is in the range of 0.5V to 2.5V. The output voltage of the DAC sets the differential input range of the ADC, which is ±REF_ADC. The desired input range can be adjusted in 1.22mV steps.

In the VECANA mode, the gain information contained in the digital input word ADIN automatically sets the DAC value. See the *Vecana Interface* section for further information.

In all other modes, there is a register for every input channel inside the digital interface, which stores the gain information for any given channel. When a particular channel is selected by the application, the value of this register is automatically written to the DAC and the DAC output is adjusted to the desired value. The DAC settles to this value within 250ns (equivalent to the minimum acquisition time).

The gain information inside the registers is set to zero when a reset condition occurs. These registers need to be set to the selected value before the ADCs are used.

In VECANA mode, the DAC is initially set to Full-Scale and the differential input range is equal to ±(voltage at the REFIN pin).

CAUTION: An essential offset error occurs when data is held on the sampling capacitors A2 and B2 (or AX and BX) and the gain of the ADC is modified in intermediate conversions before converting the particular channels A2 and B2 (or AX and BX). This offset error is possible under two conditions:

1. Data can be held on the asynchronous sample-and-hold capacitors AX and BX with the $\overline{HOLD2}$ signal. Other channels can be converted before the asynchronous signals AX and BX. The offset error occurs if the gain is changed during these conversions.
2. With the input commands 4−6, channels A1 and B1 are held together with A2 and B2. Channels A1 and B1 will be converted first. During this conversion or further intermediate conversions, the offset error occurs if the gain is modified before the conversion of channels A2 and B2.

2.2.5 Offset Adjustment

The offset can be adjusted, similar to the gain, to a 12-bit level with respect to the actual input voltage range of the ADC. For example, if the input range is ±1V, the offset can be adjusted in increments of 488µV. The maximum adjustment is ±12.5% of the input range.

There is a register inside the digital interface for each input channel. This registers store the offset adjustment value for each channel. When a channel is selected for conversion, the offset is automatically adjusted. The selected channel and the related register information must not be changed during the conversion.

Setting the register to 201_H results in a –12.5% adjustment, 000_H results in no adjustment, and $1FF_H$ results in a +12.5% adjustment. The offset adjustment value 200_H is not allowed.

The offset adjustment cannot be used in VECANA mode. A reset condition will set the offset adjustment to zero.

2.2.6 Transition Noise

The transition noise of the ADS7869 itself is low, as shown in Figure 1−5. Applying a low-noise DC input and initiating 8000 conversions generated this histogram.

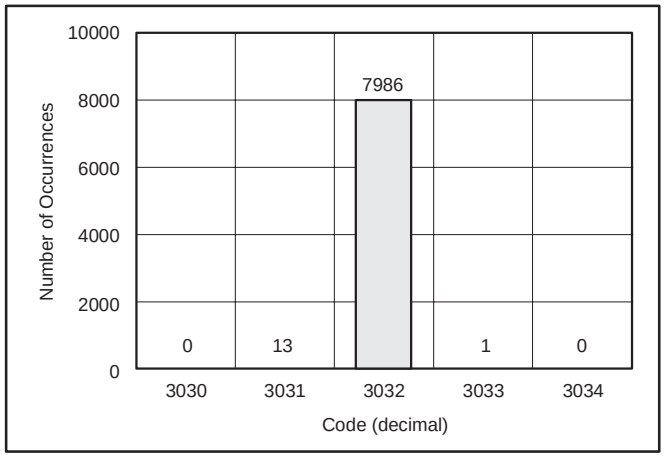


Figure 1−5. Histogram of 8000 Conversions

2.3 Sign Comparators

The ADS7869 includes two sets of sign comparators that differ in their hysteresis. The first set, which is used for the position sensor inputs in motor control applications, is connected to the inputs A1, B1, A2, and B2. The hysteresis of these comparators is typically 75mV. In motor control applications, these comparators are used to measure the signs of the position sensor input signals.

The second set is in parallel to the window comparators at the U_C, V_C, and W_C pins. The hysteresis of these components is typically 10mV. In motor control applications, these comparators are used to measure the sign of the main currents.

The sign comparator switches from 0 to 1 if the differential input voltage is above +1/2 of the hysteresis. If the output is 1, the sign comparator switches back to 0 if the differential input voltage is below −1/2 of the hysteresis. See Figure 1−6.

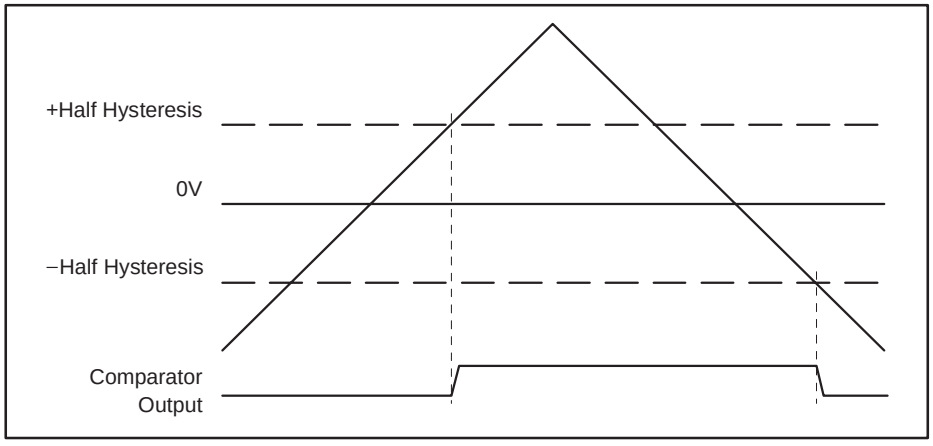


Figure 1−6. Typical Transfer Function of a Sign Comparator

The input range of the comparators is limited. The lower voltage of the differential inputs should always be within the range of 0 to AV_{DD}−1.8V.

On every comparator, the output is delayed to the input voltage. This delay is dependent on the overdrive of the comparator inputs. The overdrive is the input voltage (V_{IN}) minus one-half of the hysteresis.

If the differential input voltage of the position sensor sign comparator is switching from –40mV to +40mV (step function, 2.5mV overdrive), then the delay time of the output is typically 100ns. The delay is reduced to typically 25ns if the comparator is switching between –100mV and +100mV (72.5mV overdrive). For the delay times as a function of step size with different overdrives, see Figure 1−7 and Figure 1−8.

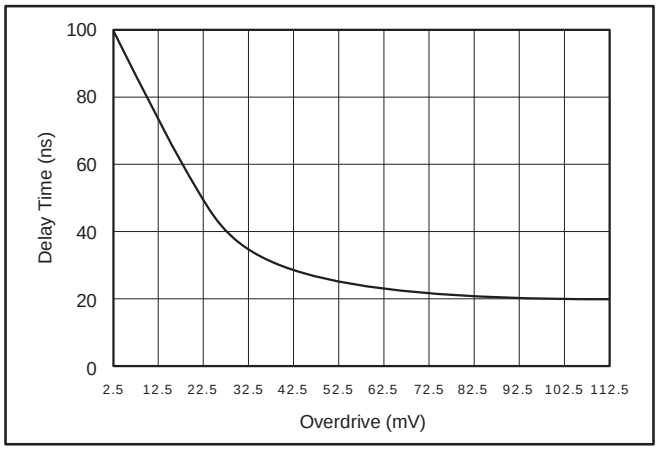


Figure 1−7. Position Sensor Comparator Overdrive

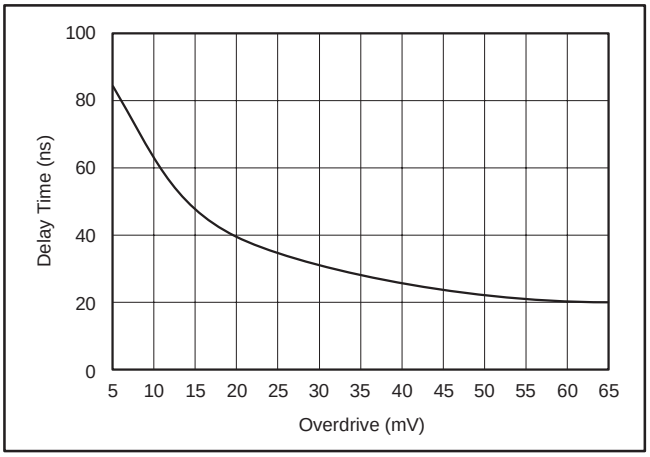


Figure 1−8. Current Sign Comparator Overdrive

2.4 Window Comparators

The window comparators test if the input voltage is within a certain range; this range is ±(voltage applied to DAIN, pin 30). If the differential input voltage remains within this range, then the output of the window comparator is 1. If the voltage is outside this range, then the output is set to 0. The window comparator has a hysteresis that is turned on when the output is 0. The comparator outputs switch back to 1 when the input voltage is within in the range of ±(DAIN −60mV). (See Figure 1−9.) The voltage at DAIN needs to be in a range of 0.5V to 2.5V.

The window comparator has a switched capacitor circuitry, similar to the ADC architecture, but different from other window comparators. This design dramatically increases the accuracy; due to the additional accuracy, a proper front-end of the input signal is required. (See the *Window Comparator Inputs* section.)

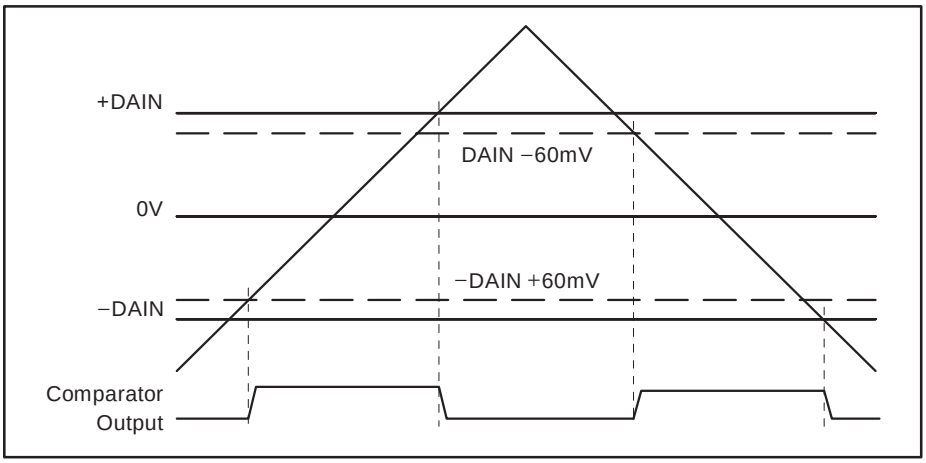


Figure 1−9. Typical Transfer Function of a Window Comparator

Two clock cycles are used to sample the inputs. The next two clock cycles are used to test the lower and the upper voltage limit. Every four clock cycles (or every 250ns with a 16MHz clock) the output of the window comparator is updated. In a worst-case scenario, it takes six clock cycles for the window comparator to detect a current limit. The window comparators need a continuous clock to operate properly.

In motor control applications, the window comparators are used to monitor the main currents for failures.

2.5 8-Bit Digital-to-Analog Converter

A voltage between 0.5V to 2.5V is required at DAIN (pin 30) to set the range of the window comparators; this can be accomplished with the 8-bit DAC. The DAC value is programmed via the digital interface. Input code 00_H corresponds to a DAC output voltage of 0V. The full-scale value (FF_H) is at 2.49V (internal reference minus 1LSB).

The impedance of the output is typically 10kΩ; the output impedance is independent of the output voltage. The DAC output is connected to DAOUT (pin 29). The settling time (t_S) is dependent on the external capacitance (C_e) on this pin, and can be calculated to:

$$t_s = 10k\Omega \cdot C_e \cdot (n + 1) \cdot \ln(2) \quad (2)$$

In this equation, *n* is equal to 8, the resolution of the DAC. The output impedance also limits the output current. This current should not exceed 0.5µA (0.5µA•10kΩ = 5mV).

DAOUT and DAIN can be shorted. A capacitor (typically 0.1µF) can be used to low-pass the DAC output; however, this low-pass configuration is not required.

2.6 Internal Reference

The internal reference, REFOUT (pin 96), provides the 2.5V required for the reference input of the ADCs at REFIN (pin 97). An internal buffer with a high impedance output drives the reference output pin. This internal buffer is optimized to reject glitches at the reference pin. Any capacitor can be connected to the REFOUT pin in able to reduce noise. It is recommended that a 0.1µF capacitor be connected between the REFOUT (pin 96) and the SGND (pin 13). The Signal ground, SGND, is used internally as a negative reference. The reference voltage is considered a differential voltage between this ground and REFOUT.

Normally, the REFOUT and REFIN pins are both shorted. The internal reference provides an excellent temperature drift, typically 20ppm, and an initial accuracy of 2.5V±20mV at 25°C. If this does not provide the required accuracy for an application, then an external reference can be connected to the REFIN pin.

2.7 Grounding

Optimal test results were achieved with a solid ground plane: linearity, offset, and noise performance each showed improvement. During PCB layout, care should be taken that the return currents do not cross any sensitive areas or signals.

Digital signals that interface with the ADS7869 are referenced to the solid ground plane. ESD protection diodes, inside the ADS7869, start conducting if the grounds are separated and the digital inputs go below –0.3V; this includes short glitches. Current will flow through the substrate of the ADS7869 and will disturb the analog performance.

2.8 Supply

The ADS7869 has two separate supplies, BV_{DD} (pins 48 and 78) and AV_{DD} (pins 8, 18, 28, 85 and 98).

BV_{DD} is used as a digital pad supply only, and is in the range of 2.7V to 5.5V. This allows the ADS7869 to interface with all state-of-the-art processors and controllers. BV_{DD} should be filtered in order to limit the noise energy from the external digital circuitry to the ADS7869. The current through BV_{DD} is far below 5mA; depending on the external load, a 10Ω to 100Ω resistor can be placed between the external digital circuitry and the ADS7869. Bypass capacitors (two 0.1µF and one 10µF) should be placed between the two BV_{DD} pins and the ground plane.

AV_{DD} supplies the internal circuitry, and can vary from 4.5 to 5.5V. It is not possible to use a passive filter between the digital board supply of the application and the AV_{DD} pins, because the supply current of the ADS7869 is typically 45mA. In order to generate the analog supply voltage for the ADS7869 and the necessary analog front-end, a linear regulator (7805 family) is recommended. Bypass capacitors of 0.1µF should be placed between all AV_{DD} pins and the ground plane. Bypass capacitors of 10µF should be placed between two AV_{DD} pins and the ground plane.

3 Digital Section

3.1 Introduction

The ADS7869 can interface with a DSP or μC in four different ways. The M1 and M0 pins determine in which mode the ADS7869 will communicate; see Table 1−1. It can be connected as a standard VECANA01 interface, as an SPI, or as two different parallel interfaces.

Table 1−1. Selection of Interface Mode

M1	M0	MODE
0	0	VECANA mode
0	1	SPI mode
1	0	Parallel 1
1	1	Parallel 2

As a function of the selected mode, some pins will have different assignment as shown in Table 1−2.

Table 1−2. Mode vs Pin Functions

Pin No. 80, 81 (M1, M0)	VECANA Mode(1) 00	SPI(1) 01	Parallel 1 10	Parallel 2 11
56	NC	NC	ADDR0 (LSB)	ADDR0 (LSB)
55	NC	NC	ADDR1	ADDR1
54	NC	NC	ADDR2	ADDR2
53	S1	NC	ADDR3	ADDR3
52	S0	NC	ADDR4	ADDR4
51	WINCLK	NC	ADDR5 (MSB)	ADDR5 (MSB)
75	NC	NC	DATA0 (LSB)	DATA0 (LSB)
74	NC	NC	DATA1	DATA1
73	NC	NC	DATA2	DATA2
72	NC	NC	DATA3	DATA3
71	NC	NC	DATA4	DATA4
70	ADOUT1 ADOUT1(3)	NC	DATA5	DATA5
69	ADOUT2 ADOUT2(3)	NC	DATA6	DATA6
68	ADOUT3 ADOUT3(3)	SPISOMI	DATA7	DATA7
67	ADIN ADIN(3)	SPISIMO	DATA8	DATA8
66	NC	SPICLK	DATA9	DATA9
65	NC	NC	DATA10	DATA10
64	NC	NC	DATA11	DATA11
63	NC	NC	DATA12	DATA12
62	NC	NC	DATA13	DATA13
61	NC	NC	DATA14	DATA14
60	NC	NC	DATA15 (MSB)	DATA15 (MSB)
57	NC	SPISTE	CS	CS
59	NC	NC	R/W	RD / – (2)
58	NC	NC	WE	WR / R/W (2)
77	CLK ADCLK(3)	CLK	CLK	CLK
79	RST	RST	RST	RST
49	NC	INT	INT	INT
83	DAV ADBUSY(3)	DAV	DAV	DAV
87	HOLD1 ADCONV(3)	HOLD1	HOLD1	HOLD1
86	HOLD2 NPSH(3)	HOLD2	HOLD2	HOLD2

(1) NC means no connection. The NC pins in VECANA01 and SPI modes should be grounded with a pull-down resistor.
(2) For parallel mode 11 there is one sub-mode for compatibility with the TMS320c54xx DSP family; see *Mode 11 Bus Access (TMS320c54xx DSP family-compatible mode)* section.
(3) Original VECANA01 pin names.

3.2 VECANA Interface

The VECANA01 mode of the ADS7869 interface acts exactly like the original VECANA01 interface. This mode was added to the ADS7869 for backward-compatibility purposes. The VECANA01 interface is a proprietary serial interface with one serial input and three serial outputs.

Sampling and conversion are controlled with the $\overline{\text{HOLD1}}$ and CLK inputs. The ADS7869 is designed to operate with an external clock supplied to the CLK input. This allows the conversion to be synchronous with the system clock, thus reducing transient noise effects. The DAV signal indicates when a conversion is taking place with a low-level pulse. The DAV signal is equivalent to the ADBUSY signal in the VECANA01.

The typical clock frequency for the specified accuracy is 16MHz. This results in a complete conversion cycle, S/H acquisition and analog-to-digital (A/D) conversion of 1µs. It is possible to stop the clock after 14 clock cycles and start it again when the next conversion starts (after $\overline{\text{HOLD1}}$ goes low); see the *WINCLK Selection* section.

When power is applied to the ADS7869, one conversion cycle is required for initialization before valid digital data is transmitted on the second cycle. The first conversion after power is applied is performed with indeterminate configuration values in the Input Setup Register. The second conversion uses those values to perform proper conversions and to output valid digital data from each of the ADCs.

The setup word received by the ADS7869 is used for the next conversion cycle while the ADCs are converting and transmitting their serial digital data for one conversion cycle. The 13-bit word is supplied to ADIN (pin 67), and is stored in the buffered Input Setup Register.

Configuration parameters are:

- DAC output voltage;
- Programmable gain/input voltage range;
- Input multiplexer; and
- sample-and-hold selection.

The DAC Input portion of the ADIN word (bits DAC [7...0]) determines the value of the DAC output voltage; see Table 1−5. The 8-bit DAC has 256 possible output steps from 0V to +2.490V. The value of 1LSB is 9.76mV (see Table 1−3 for input/output relationships).

Table 1−3 to Table 1−6 show information regarding these parameters.

Table 1−3. DAC Input/Output Relationships

DAC Input Code		Analog Output
00_H	$0000\ 0000_B$	0V
01_H	$0000\ 0001_B$	+0.010V
...	...	...
...	...	...
FF_H	$1111\ 1111_B$	+2.490V

Table 1−4. VECANA Gain Select Information

Gain Select Bits	Gain Setting	Input Voltage Range
0_H	5.0V/V	±0.5V
1_H	2.5V/V	±1.0V
2_H	1.25V/V	±2.0V
3_H	1.0V/V	±2.5V

The Gain Select portion (bits GAIN [1..0]) determines the programmable gain of the ADIN word; see Table 1−5. The gain for all three ADCs is set by one gain input parameter. The gain values and allowable full-scale inputs are shown in Table 1−4.

The gain setting and input voltage range for the channels AN1, AN2, and AN3 at ADC3 are always 1.0V/V with respect to ±2.5V.

Table 1−5. 13-bit VECANA ADIN Word Format

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	GAIN1	GAIN0	IN2	IN1	IN0

3.2.1 Input Channel Selection

Table 1−6 shows the relationships between the value of the input select bits and the input channels that are converted.

Table 1−6. Controls for Input Multiplexers and Sample Holds

INPUT SELECT, BITS 2−0		ANALOG SIGNAL CONNECTED TO ADC_X					
HEX CODE	BINARY CODE	ADC_1		ADC_2		ADC_3	
0_H	000	—	—	—	—	AN3	SH_5
1_H	001	AX	SH_6	BX	SH_7	AN3	SH_5
2_H	010	A2	SH_1	B2	SH_3	AN2	SH_5
3_H	011	A2	SH_2	B2	SH_4	AN2	SH_5
4_H	100	A1	SH_1	B1	SH_3	AN1	SH_5
5_H	101	A1	SH_1	B1	SH_3	AN1	SH_5
6_H	110	A1	SH_1	B1	SH_3	AN1	SH_5
7_H	111	IU	SH_1	IV	SH_3	IW	SH_5

Input Select = 0_H

The synchronous sample-and-hold, SH_5, samples AN3 (only), then ADC3 converts it on the signal $\overline{HOLD1}$.

Input Select = 1_H

AX is sampled by the asynchronous sample-and-hold, SH_6, with the signal $\overline{HOLD2}$; ADC1 converts it on the signal $\overline{HOLD1}$. BX is sampled by the asynchronous sample-and-hold, SH_7, with the signal $\overline{HOLD2}$; ADC2 converts it on the signal $\overline{HOLD1}$. AN3 is sampled by the synchronous sample-and-hold, SH_5, then ADC3 converts it on the signal $\overline{HOLD1}$.

The signal $\overline{HOLD2}$ must be low during the entire conversion. If $\overline{HOLD2}$ is high before a conversion starts, ADC_1 and ADC_2 will not convert.

Input Select = 2_H

A2 is sampled by the synchronous sample-and-hold, SH_1; ADC_1 converts it on the signal $\overline{HOLD1}$. B2 is sampled by the synchronous sample-and-hold, SH_3; ADC_2 converts it on the signal $\overline{HOLD1}$. AN2 is sampled by the synchronous sample-and-hold, SH_5; ADC_3 converts it on the signal $\overline{HOLD1}$.

Input Select = 3_H

A2 is converted by ADC_1 on the signal $\overline{HOLD1}$. A2 is sampled on SH_2 in a preceding conversion with Input Select 4_H, 5_H, or 6_H. B2 is converted by ADC_2 on the signal $\overline{HOLD1}$. B2 is sampled on SH_4 in a preceding conversion with Input Select 4_H, 5_H, or 6_H. AN2 is sampled by the synchronous sample-and-hold, SH_5; ADC_3 converts it on the signal $\overline{HOLD1}$.

Input Select = 4_H, 5_H and 6_H

A1 is sampled by the synchronous sample-and-hold, SH_1; ADC_1 converts it on the signal $\overline{HOLD1}$. B1 is sampled by the synchronous sample-and-hold, SH_3; ADC_2 converts it on the signal $\overline{HOLD1}$. AN1 is sampled by the synchronous sample-and-hold, SH_5; ADC_3 converts it on the signal $\overline{HOLD1}$. A2 is sampled by the synchronous sample-and-hold, SH_2, on the signal $\overline{HOLD1}$. B2 is sampled by the synchronous sample-and-hold, SH_4, on the signal $\overline{HOLD1}$.

Input Select = 7_H

IU is sampled by the synchronous sample-and-hold, SH_1; ADC_1 converts it on the signal $\overline{HOLD1}$. IV is sampled by the synchronous sample-and-hold, SH_3; ADC_2 converts it on the signal $\overline{HOLD1}$. IW is sampled by the synchronous sample-and-hold, SH_5; ADC_3 converts it on the signal $\overline{HOLD1}$.

3.2.2 VECANA Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
ADCLK Period	t_{C1}	62.5		ns
ADCLK HIGH or LOW Time	t_{W1}	20		ns
HOLD1 Signal Setup Time	t_{SU1}	25		ns
HOLD1 Signal Hold Time	t_{H1}	20	$15 + 12.5t_{C1}$	ns
$\overline{HOLD2}$ Signal Setup Time	t_{SU2}	0		ns
$\overline{HOLD2}$ Signal Hold Time	t_{H2}	0		ns
Delay Time from ADCLK Rising to DAV Falling Edge	t_{D1}		15	ns
Output Data Delay Time	t_{D2}		10	ns
Input Data Setup Time	t_{SU3}	10		ns
Input Data Hold Time	t_{H3}	10		ns
Delay Time from ADCLK Rising to DAV Rising Edge	t_{D3}		15	ns
Sampling Time	t_{SAMPLE}	4		t_{C1}

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

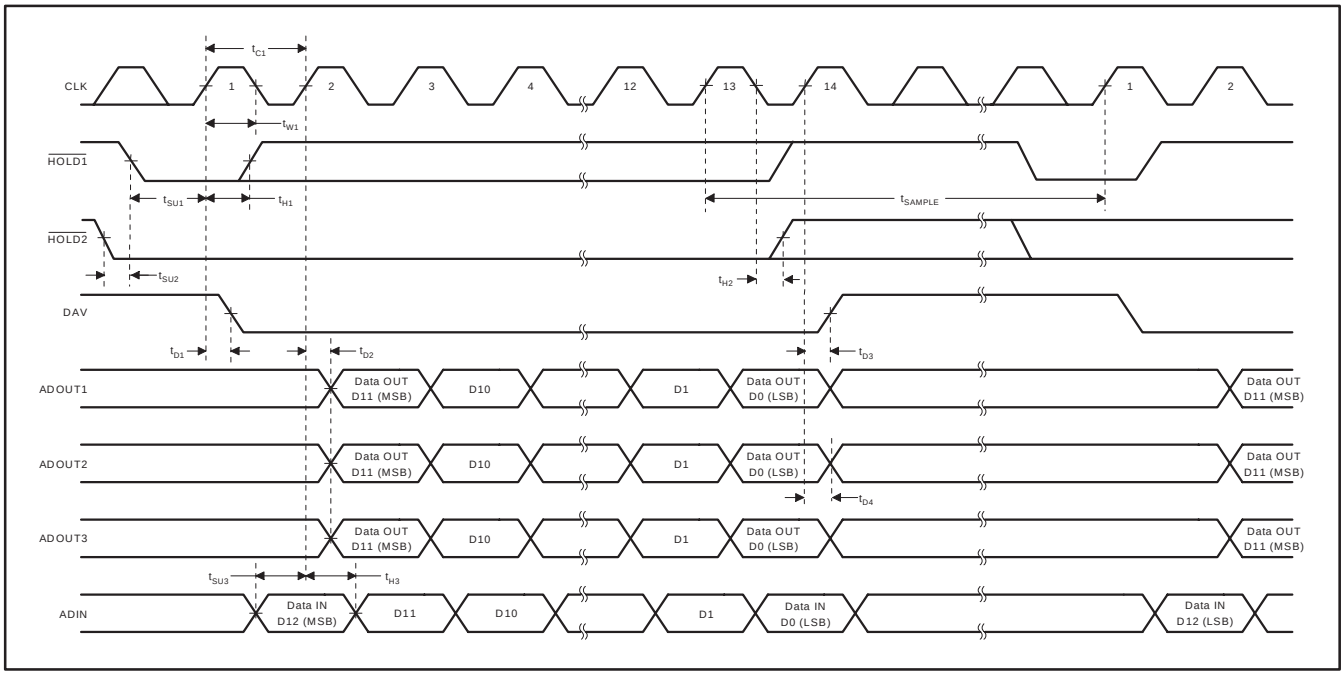


Figure 1−10. VECANA Access

3.2.3 WINCLK Selection

It is possible to apply a separate clock for the window comparators at the WINCLK (pin 51) in VECANA01 mode. By using the pins S0 (pin 52) and S1 (pin 53) as decoder inputs, the window comparators can be supplied with the system clock, an external clock (supplied by the WINCLK), and two divided external clocks; see Table 1−7.

Table 1−7. Window Comparator Clock

S1	S0	Clock to Window Comparators
0	0	Synchronous system clock
0	1	External WINCLK clock
1	0	External WINCLK clock / 2
1	1	External WINCLK clock / 4

The system clock, provided by CLK (pin 77), drives the window comparators in the other modes (SPI and parallel modes).

The window comparator clock, WINCLK, must be synchronous with the system clock, provided by CLK (pin 77). The window comparators can be supplied with a 6MHz clock when the system runs with a 15MHz clock.

In order to provide the window comparators with a maximum of 1µs detection time, a minimum clock of 6MHz must be supplied. See the *Window Comparator* section. It is necessary to operate the window comparators with a continuous clock.

3.3 Serial Peripheral Interface (SPI)

The SPI runs fully asynchronous to the rest of the system. The four signals of the SPI are SPICLK, SPISIMO, SPISOMI and $\overline{\text{SPISTE}}$. The maximum speed of the SPI is 25MHz. When the select signal $\overline{\text{SPISTE}}$ is HIGH, the entire SPI, except the address and the data registers, is in reset state. The SPI clock SPICLK and the serial data input SPISIMO are disabled when $\overline{\text{SPISTE}}$ is HIGH. The incoming data is strobed by the SPI on the falling edge of the SPICLK. Outgoing data is put on the output SPISOMI on the rising edge of the SPICLK (see Figure 1−11). For a transmission of one 16-bit data word, 24 bits are required. The first incoming bit to the ADS7869 determines if the whole transmission is a read or a write operation. A ‘1’ means a read and a ‘0’ means a write operation. There are seven address bits, but only the six LSBs are used. Then the 16 data bits are transmitted or received (see Table 1−8).

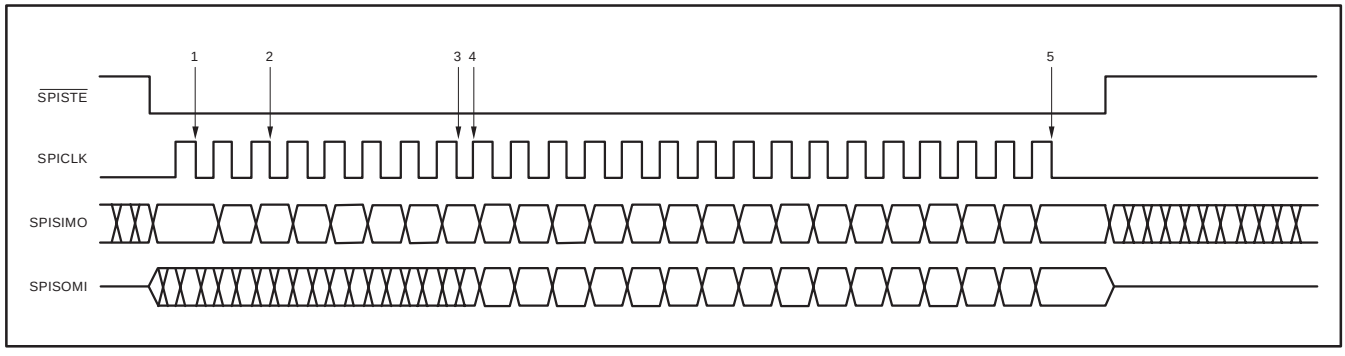


Figure 1−11. One SPI Transfer Cycle

Table 1−8. SPI Write 24-bit Word Format

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
R/W	X	Address						Data															

One 16-bit transfer is accomplished, as follows:

1. On the first falling edge of SPICLK, the read/write bit is strobed.
2. On the third falling edge of SPICLK, the MSB of the address (bit 5) is strobed.
3. On the eighth falling edge of SPICLK, the LSB of the address (bit 0) is strobed and the corresponding data of the register map is read.
4. On the ninth rising edge, the data read from the register map is latched into a shift register and shifted one position each rising edge of the SPICLK. This data is always sent out, even when a write operation is performed.
5. On the 24th falling edge of SPICLK, the last data bit is shifted in from SPISIMO and a write pulse is generated to write the data into the register map, if a write operation was performed.

During continuous read or write (see Figure 1−12), the address is decrementing after each read or write; see the indicating arrows. When the address is set to 00_H, in the beginning, the FIFO can be read out fast. The data is written into the register map on the 16th SPICLK of a data word. If the $\overline{\text{SPISTE}}$ is inactive before the 16th SPICLK in a data word, the data is not written into the register map; therefore, the data is lost.

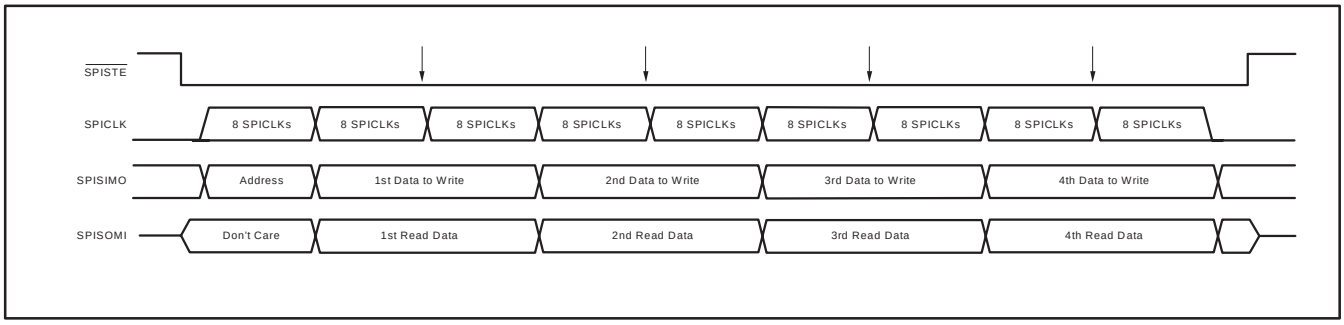


Figure 1−12. Continuous SPI Transfer Cycle

3.3.1 SPI Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
SPICLK Period	t_{C1}	40		ns
SPICLK HIGH or LOW Time	t_{W1}	10		ns
Delay Time from SPISTE Falling to SPICLK Rising Edge	t_{D1}	15		ns
Delay Time from SPISTE Falling to SPISOMI not Tristate	t_{D2}		15	ns
Data Setup Time	t_{SU1}	10		ns
Input Data Hold Time	t_{H1}	10		ns
Output Data Delay Time	t_{D3}		10	ns
Enable Lag Time	t_{D4}	15		ns
SPISOMI Disable Time	t_{D5}		15	ns
Sequential Transfer Delay	t_{W2}	30		ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

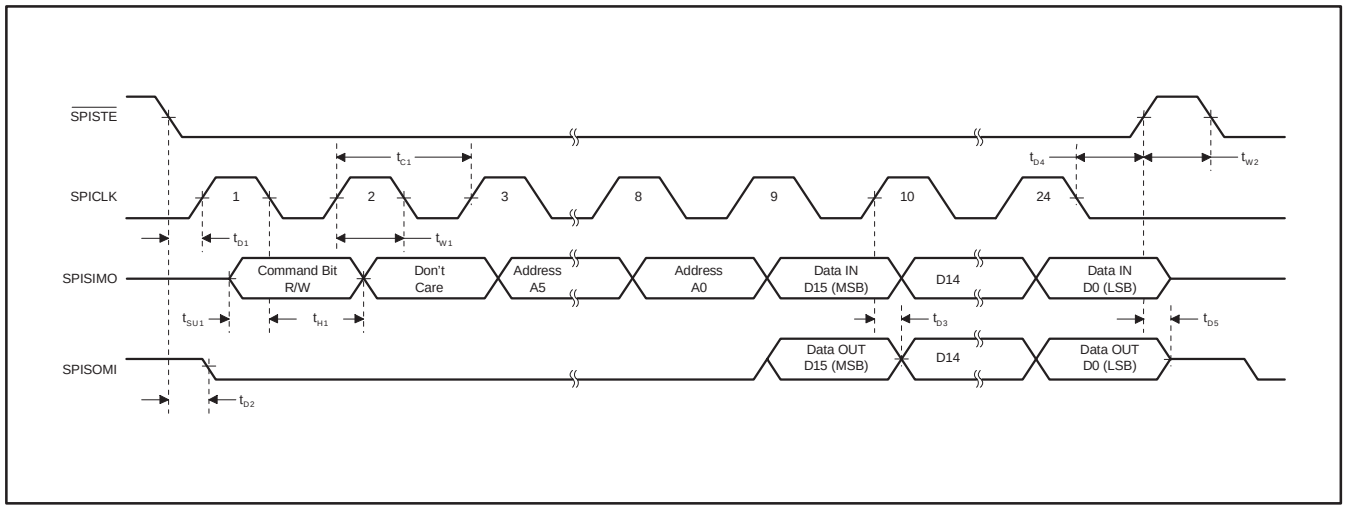


Figure 1−13. SPI Access

3.4 Parallel Interface

The Parallel Interface has the following major capabilities:

1. Data words:
   - Data path with a width of 16 bits is supported.
2. Bus handshaking:
   - Separate $\overline{RD}$ and $\overline{WR}$ style control signals.
   - Separate R/$\overline{W}$ and $\overline{WE}$ style control signals.
3. Mapping
   - The ADS7869 appears as a memory-mapped peripheral. See Table 1−10 on page 37 and Table 1−11 on page 38.
   - Internal registers are directly mapped into consecutive locations in the external bus address space.

3.4.1 Parallel Read and Write Control

Reading from and writing to the ADS7869 is controlled by the chip select input ($\overline{CS}$, pin 57), the write input ($\overline{WR}$, pin 58) and the read input ($\overline{RD}$, pin 59). There is a control bit for mode 11, which can be reset to activate a special compatibility mode. (See *Mode 11 Bus Access [DSP-compatible mode]* section.) The read and write pins can be configured as a combined Read/Write and Write enable depending on the needs of the host processor. The mode pins M0 and M1 determine the method by which the ADS7869 is accessed by the host (see Table 1−9).

Table 1−9. Host Parallel Port Operation

[M1, M0]	PIN NAME	PIN NO.	FUNCTION	OPERATION
‚10‘	R/$\overline{W}$	59	Read/Write Signal	0: Data can be written to ADS7869; see $\overline{WE}$ 1: Data from ADS7869 is written to the Data Bus
	$\overline{WE}$	58	Write Enable	0: Data Bus is read by ADS7869 at rising edge 1: ADS7869 Write function is disabled
‚11‘ standard	$\overline{RD}$	59	Read Signal	0: Data from ADS7869 is written to the Data Bus 1: ADS7869 Read function is disabled
	$\overline{WR}$	58	Write Signal	0: Data Bus is read by ADS7869 at rising edge 1: ADS7869 Write function is disabled
‚11‘ TMS	—	59	—	Signal is ignored by ADS7869
	R/$\overline{W}$	58	Read/Write Signal	0: Data Bus is read by ADS7869 at rising edge of $\overline{CS}$ 1: Data from ADS7869 is written to the Data Bus

3.4.2 Mode 10 Bus Access

When M1 = 1 and M0 = 0 (mode 10), the host port uses the $\overline{RD}$ (pin 59) as a read/write signal (R/$\overline{W}$) and the $\overline{WR}$ (pin 58) as a write-enable signal $\overline{WE}$. The current cycle is only processed when the chip select input $\overline{CS}$ (pin 57) of the ADS7869 is active low.

R/$\overline{W}$ determines the direction of the transfer during a bus cycle; see Figure 1−14. When R/$\overline{W}$ is high, data is placed on the databus by ADS7869, according to the address, as long as $\overline{CS}$ is low.

For a write cycle, a low-level signal (on $\overline{WE}$) indicates to the ADS7869 that the data on the bus is valid. With the rising edge of $\overline{WE}$ the data is latched into the ADS7869. When the host sets $\overline{CS}$ to low, a valid access to the ADS7869 is detected (see Figure 1−15).

3.4.2.1 Read Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Delay time from $\overline{CS}$ LOW to output data not in tri-state mode(2)	t_{D1}		8	ns
Access time from address valid to output data valid	t_{A1}		10	ns
Delay time from address not valid to output data not valid(3)	t_{D2}	0	8	ns
Delay time from CS HIGH to output data in tri-state mode(4)	t_{D3}		8	ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) Refer to $\overline{CS}$ signal or R/$\overline{W}$ signal whichever occurs last.
(3) One or more read cycles can be performed in one $\overline{CS}$ cycle.
(4) Refer to $\overline{CS}$ signal or R/$\overline{W}$ signal whichever occurs first.

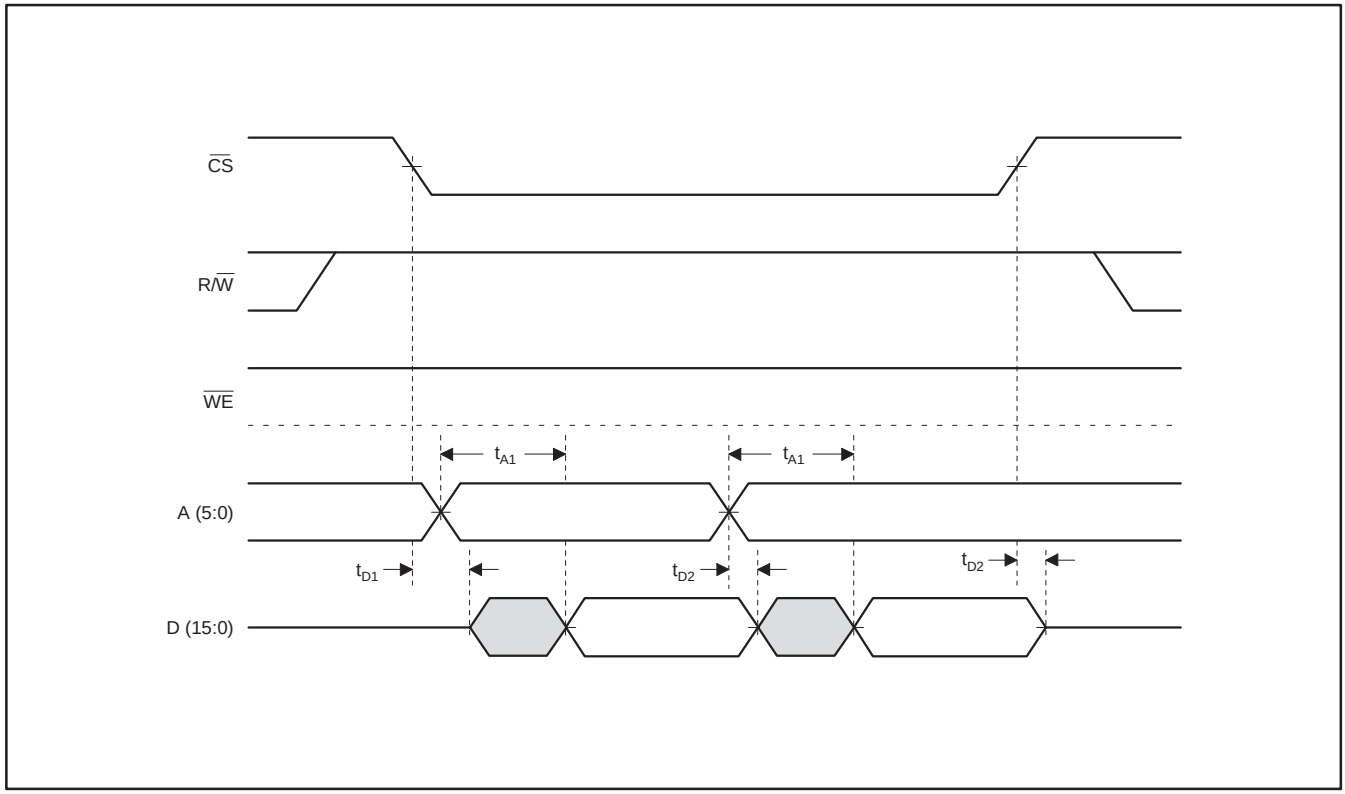


Figure 1−14. Mode 10 Read Access

3.4.2.2 Write Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Delay time from R/W LOW to CS LOW	t_{D1}	0		ns
Access time from $\overline{CS}$ LOW to $\overline{WE}$ HIGH	t_{A1}	25		ns
Width time for $\overline{WE}$ LOW	t_{W1}	20		ns
Width time for $\overline{WE}$ HIGH(2)	t_{W2}	10		ns
Setup time, address valid before rising edge of $\overline{WE}$	t_{SU1}	10		ns
Hold time, address valid after rising edge of $\overline{WE}$	t_{H1}	5		ns
Setup time, data valid before rising edge of $\overline{WE}$	t_{SU2}	10		ns
Hold time, data valid after rising edge of $\overline{WE}$	t_{H2}	5		ns
Delay time from $\overline{WE}$ HIGH to $\overline{CS}$ HIGH	t_{D2}	10		ns
Delay time from $\overline{CS}$ HIGH to R/$\overline{W}$ HIGH	t_{D3}	0		ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) One or more write cycles can be performed in one $\overline{CS}$ cycle.

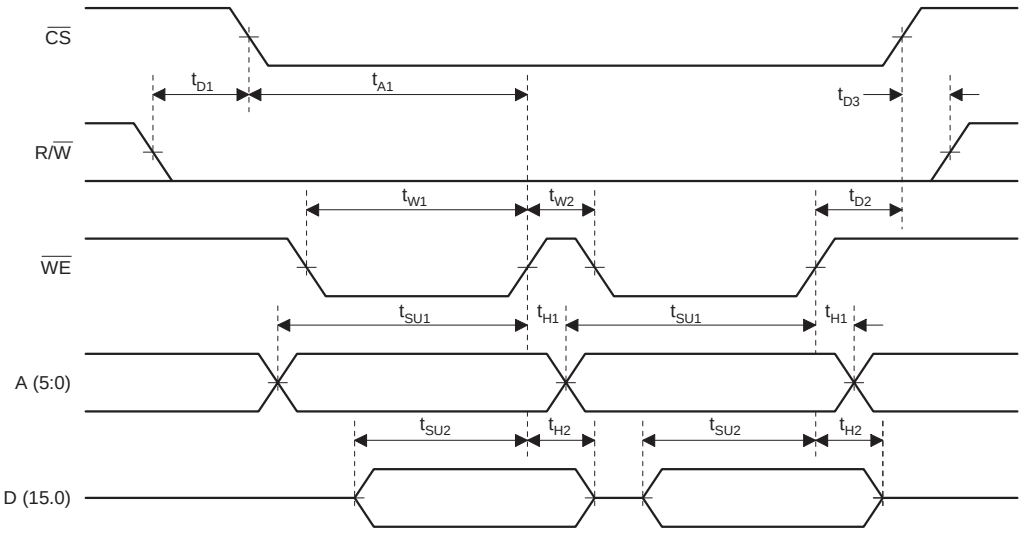


Figure 1−15. Mode 10 Write Access

3.4.3 Mode 11 Bus Access (Standard Mode)

When M1 = 1 and M0 = 1 (mode 11), the host port uses $\overline{WR}$ (pin 58) and $\overline{RD}$ (pin 59) for independent write and read access to the ADS7869. The current cycle is processed only when the $\overline{CS}$ (pin 57) input of the ADS7869 is an active low. Bit 0 of the PARALLEL register (Address 27_H) must have a reset value of 1 to use the standard mode.

In Mode 11 operation, $\overline{RD}$ indicates to the ADS7869 that the host processor has requested a data transfer (see Figure 1−16). The ADS7869 outputs data to the host. The address can be changed within a $\overline{CS}$ low cycle, and more than one data can be read.

To configure the registers in the ADS7869, the host issues a $\overline{WR}$ signal to indicate that valid data is available on the bus. With the rising edge of the $\overline{WR}$ the data is latched into the ADS7869; see Figure 1−17. The address for the ADS7869 must be valid before the write operation takes place. The $\overline{CS}$ signal can stay low between two consecutive writes.

3.4.3.1 Read Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Delay time from CS LOW to output data not in tri-state mode(2)	t_{D1}		8	ns
Access time from address valid to output data valid	t_{A1}		10	ns
Delay time from address not valid to output data not valid(3)	t_{D2}	0	8	ns
Delay time from CS HIGH to output data in tri-state mode(4)	t_{D3}		8	ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) Refer to $\overline{CS}$ signal or $\overline{RD}$ signal whichever occurs last.
(3) One or more read cycles can be performed in one $\overline{CS}$ cycle.
(4) Refer to $\overline{CS}$ signal or $\overline{RD}$ signal whichever occurs first.

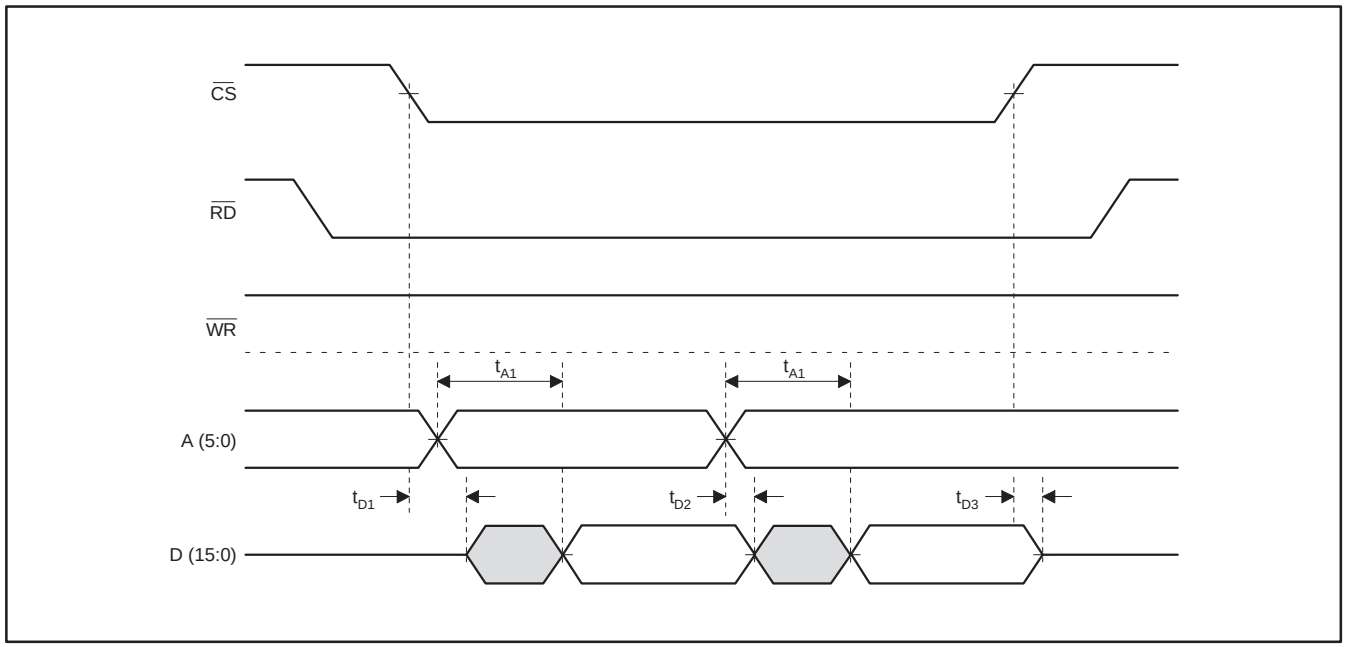


Figure 1−16. Mode 11 Read Access (Standard Mode)

3.4.3.2 Write Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Access time from CS LOW to WR HIGH	t_{A1}	15		ns
Width time for WR LOW	t_{W1}	10		ns
Width time for WR HIGH(2)	t_{W2}	10		ns
Setup time, address valid before rising edge of WR	t_{SU1}	10		ns
Hold time, address valid after rising edge of WR	t_{H1}	5		ns
Setup time, data valid before rising edge of WR	t_{SU2}	10		ns
Hold time, data valid after rising edge of WR	t_{H2}	5		ns
Delay time from WR HIGH to CS HIGH	t_{D1}	10		ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) One or more write cycles can be performed in one CS cycle.

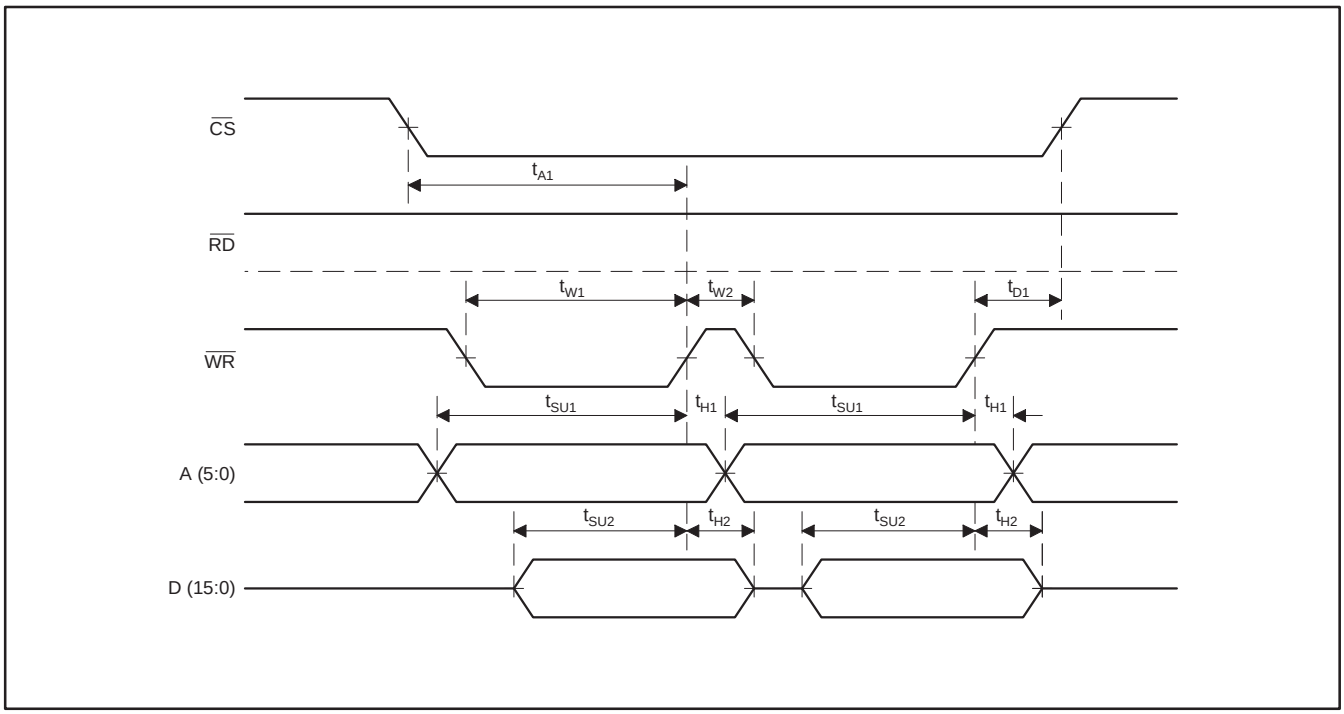


Figure 1−17. Mode 11 Write Access (Standard Mode)

3.4.4 Mode 11 Bus Access (TMS320c54xx DSP Family-Compatible Mode)

In the TMS320c54xx DSP family-compatible mode (M1 = 1 and M0 = 1), the host port uses $\overline{CS}$ (pin 57) together with $\overline{WR}$ (pin 57) as an R/$\overline{W}$ for independent read and write access to the ADS7869. Bit 0 of the PARALLEL register (address 27_H) must have a value of 0 to use this compatible mode.

In this mode, $\overline{CS}$, together with the R/$\overline{W}$ (which remains high), indicates to the ADS7869 that the host processor has requested a read data transfer (see Figure 1−18). The ADS7869 will output data to the host as long as the $\overline{CS}$ is an active low.

To configure the registers, in the ADS7869 the host puts the R/$\overline{W}$ signal to low to indicate that valid data is available on the bus. With the rising edge of the $\overline{CS}$, the data is latched into the ADS7869 (see Figure 1−19). The address for the ADS7869 must be valid before the $\overline{CS}$ is set to low.

Before using this mode, the register bit 0 at address 27_H must be reset. The reset can be performed with a TMS320C54xx DSP write operation with the original mode 11, because the write access is similar to the write access of mode 11. (See *Mode 11 Bus Access [standard mode]* section.) This mode can perform read operations, after bit 0 is reset, as mentioned above.

3.4.4.1 Read Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Delay time from $\overline{CS}$ LOW to output data not in tri-state mode	t_{D1}		8	ns
Access time from address valid to output data valid	t_{A1}		10	ns
Delay time from address not valid to output data not valid(2)	t_{D2}	0	8	ns
Delay time from CS HIGH to output data in tri-state mode	t_{D3}		8	ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) One or more read cycles can be performed in one $\overline{CS}$ cycle.

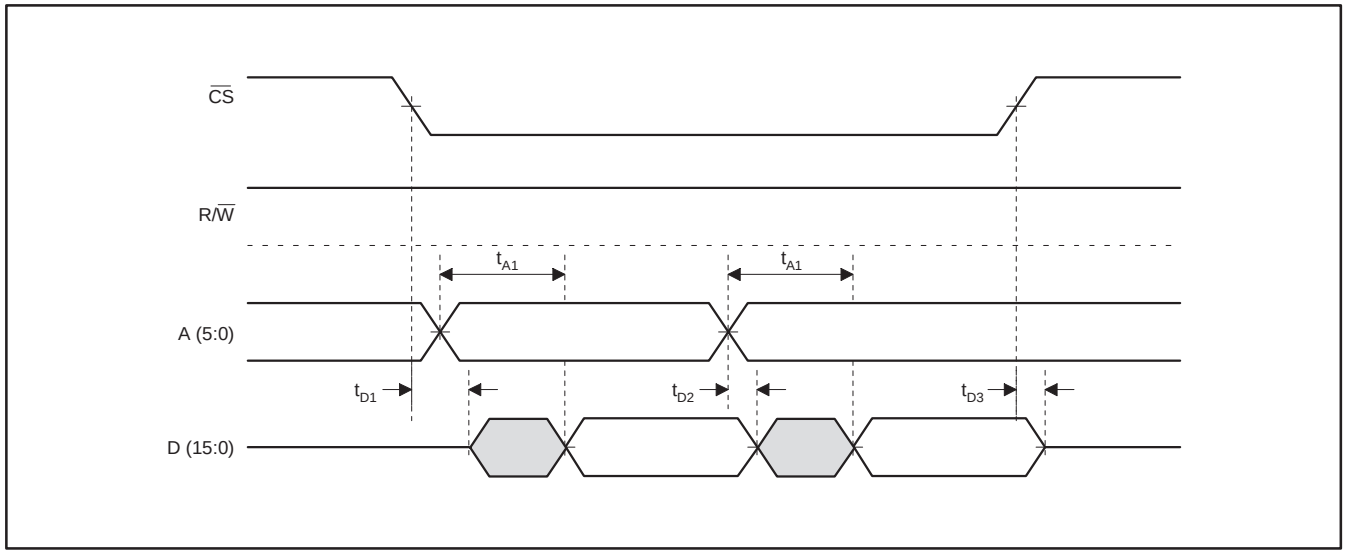


Figure 1−18. Mode 11 Read Access (TMS320c54xx mode)

3.4.4.2 Write Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Setup time from R/W LOW to CS LOW	t_{SU1}	0		ns
Hold time from $\overline{CS}$ HIGH to R/$\overline{W}$ HIGH	t_{H1}	5		ns
Setup time from address valid to CS LOW	t_{SU2}	10		ns
Hold time from $\overline{CS}$ HIGH to address not valid	t_{H2}	5		ns
Setup time from data valid to CS HIGH	t_{SU3}	10		ns
Hold time from $\overline{CS}$ HIGH to data not valid	t_{H3}	5		ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

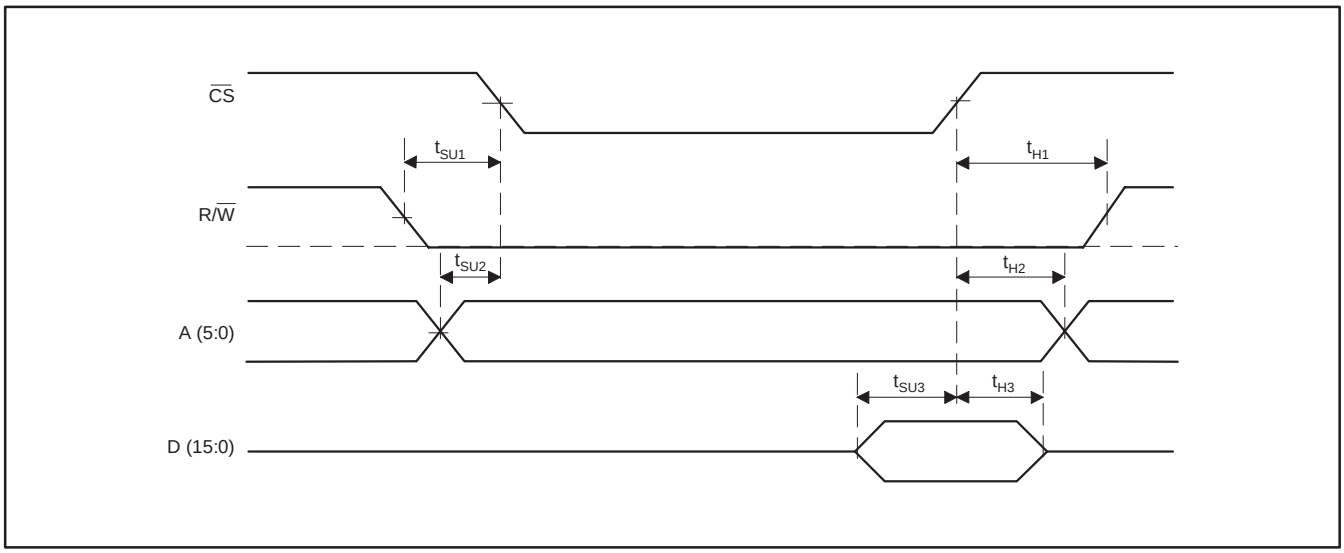


Figure 1−19. Mode 11 Write Access (TMS320c54xx mode)

3.5 Register Map

Table 1−10. Register Map Write 16-bit Data

ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00_H	Unwriteable (don't care)															
01_H	x	x	x	x	x	x	Channel IU, write 10-bit offset DAC-value									
02_H	x	x	x	x	x	x	Channel A1, write 10-bit offset DAC-value									
03_H	x	x	x	x	x	x	Channel A2, write 10-bit offset DAC-value									
04_H	x	x	x	x	x	x	Channel IV, write 10-bit offset DAC-value									
05_H	x	x	x	x	x	x	Channel B1, write 10-bit offset DAC-value									
06_H	x	x	x	x	x	x	Channel B2, write 10-bit offset DAC-value									
07_H	x	x	x	x	x	x	Channel IW, write 10-bit offset DAC-value									
08_H	x	x	x	x	x	x	Channel AN1, write 10-bit offset DAC-value									
09_H	x	x	x	x	x	x	Channel AN2, write 10-bit offset DAC-value									
$0A_H$	x	x	x	x	x	x	Channel AN3, write 10-bit offset DAC-value									
$0B_H$	x	x	x	x	x	x	Channel AX, write 10-bit offset DAC-value									
$0C_H$	x	x	x	x	x	x	Channel BX, write 10-bit offset DAC-value									
$0D_H$	x	x	x	x	Channel IU, write 12-bit gain DAC-value											
$0E_H$	x	x	x	x	Channel A1, write 12-bit gain DAC-value											
$0F_H$	x	x	x	x	Channel A2, write 12-bit gain DAC-value											
10_H	x	x	x	x	Channel IV, write 12-bit gain DAC-value											
11_H	x	x	x	x	Channel B1, write 12-bit gain DAC-value											
12_H	x	x	x	x	Channel B2, write 12-bit gain DAC-value											
13_H	x	x	x	x	Channel IW, write 12-bit gain DAC-value											
14_H	x	x	x	x	Channel AN1, write 12-bit gain DAC-value											
15_H	x	x	x	x	Channel AN2, write 12-bit gain DAC-value											
16_H	x	x	x	x	Channel AN3, write 12-bit gain DAC-value											
17_H	x	x	x	x	Channel AX, write 12-bit gain DAC-value											
18_H	x	x	x	x	Channel BX, write 12-bit gain DAC-value											
19_H	x	x	x	x	x	x	x	x	Over current, write 8-bit window DAC-value							
$1A_H$	x	x	x	x	x	x	x	x	x	x	x	DAV	x	INPUT		
$1B_H$	x	x	x	x	x	x	x	x	x	x	x	x	Write 4-bit counter control			
$1C_H$	Unwriteable (don't care)															
$1D_H$	Counter 1, write 16-bit value in EDGECOUNT1 counter															
$1E_H$	Unwriteable (don't care)															
$1F_H$	Unwriteable (don't care)															
20_H	Unwriteable (don't care)															
21_H	Counter 2, write 16-bit value in EDGECOUNT2 counter															
22_H	Unwriteable (don't care)															
23_H	Unwriteable (don't care)															
24_H	write 16-bit value in FIFO_TEST register															
25_H	write 16-bit value in COMP_TEST register															
26_H	Counter interrupt enables				x	x	x	x	x	x	x	x	x	x	FIFO interrupt enables	
27_H	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	PARALLEL
28_H	write 16-bit value in RESET register															
29_H−$3F_H$	Unwriteable (don't care)															

NOTE: 'x' means unwriteable (don't care)

Table 1−11. Register Map Read 16-bit Data

ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00_H	FIFO data															
01_H	Channel IU, read 10-bit offset DAC-value (1)															
02_H	Channel A1, read 10-bit offset DAC-value (1)															
03_H	Channel A2, read 10-bit offset DAC-value (1)															
04_H	Channel IV, read 10-bit offset DAC-value (1)															
05_H	Channel B1, read 10-bit offset DAC-value (1)															
06_H	Channel B2, read 10-bit offset DAC-value (1)															
07_H	Channel IW, read 10-bit offset DAC-value (1)															
08_H	Channel AN1, read 10-bit offset DAC-value (1)															
09_H	Channel AN2, read 10-bit offset DAC-value (1)															
$0A_H$	Channel AN3, read 10-bit offset DAC-value (1)															
$0B_H$	Channel AX, read 10−bit offset DAC−value (1)															
$0C_H$	Channel BX, read 10-bit offset DAC-value (1)															
$0D_H$	0	0	0	0	Channel IU, read 12-bit gain DAC-value											
$0E_H$	0	0	0	0	Channel A1, read 12-bit gain DAC-value											
$0F_H$	0	0	0	0	Channel A2, read 12-bit gain DAC-value											
10_H	0	0	0	0	Channel IV, read 12-bit gain DAC-value											
11_H	0	0	0	0	Channel B1, read 12-bit gain DAC-value											
12_H	0	0	0	0	Channel B2, read 12-bit gain DAC-value											
13_H	0	0	0	0	Channel IW, read 12-bit gain DAC-value											
14_H	0	0	0	0	Channel AN1, read 12-bit gain DAC-value											
15_H	0	0	0	0	Channel AN2, read 12-bit gain DAC-value											
16_H	0	0	0	0	Channel AN3, read 12-bit gain DAC-value											
17_H	0	0	0	0	Channel AX, read 12-bit gain DAC-value											
18_H	0	0	0	0	Channel BX, read 12-bit gain DAC-value											
19_H	(3)	(3)	(3)	(3)	(3)	(3)	(3)	(3)	Over current, read 8-bit window DAC-value							
$1A_H$	0	0	0	0	0	0	0	0	0	0	0	DAV	0	INPUT		
$1B_H$	Read counter control and status register															
$1C_H$	Counter 1, read 16-bit value in ASEDGCNT1 register															
$1D_H$	Counter 1, read 16-bit value in SYEDGCNT1 register															
$1E_H$	Counter 1, read 16-bit value in SYEDGPRD1 register															
$1F_H$	Counter 1, read 16-bit value in SYEDGTIME1 register															
20_H	Counter 2, read 16-bit value in ASEDGCNT2 register															
21_H	Counter 2, read 16-bit value in SYEDGCNT2 register															
22_H	Counter 2, read 16-bit value in SYEDGPRD2 register															
23_H	Counter 2, read 16-bit value in SYEDGTIME2 register															
24_H	Read 16-bit value in FIFO_TEST register															
25_H (2)	Read 6 MSB of COMP register						B2	B1	A2	A1	UC	VC	WC	UI	VI	WI
26_H	Read INTERRUPT register															
27_H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PARALLEL
28_H	Read 0000_H															
29_H−$3F_H$	Unused (read 0000_H)															

(1) MSB is copied to upper bits to achieve 16-bit two's complement values.
(2) The lower 10 bits are the comparator outputs.
(3) The MSB of the 8-bit DAC is copied in the upper 8 bits.

3.6 Register Descriptions

The following table shows the symbols that are used in this section. The last number in the symbol represents the reset value.

R	Readable Bit
W	Writeable Bit
U	Unused
0/1	Value After Reset

The clock has to be running when the registers in the register map are accessed.

3.6.1 FIFO Data Register (00_H)

The FIFO Data Register is at address 00_H in the register map. The output word of the FIFO is in16-bit format. The resolution of the ADCs is 12 bits. Output data from each of the ADCs is in binary two's complement format. The four MSBs are used for channel identification. The format of the output word is shown in Table 1−12.

There are three words stored in the FIFO for each conversion. There must be three read accesses to this register to get all three conversion values out of the FIFO.

Table 1−12. FIFO Output Word Format

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0
CA3	CA2	CA1	CA0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

	CA3−0: INPUT CHANNEL ADDRESS BITS
Bit 15−12:	0000 = Data from IU input 0001 = Data from A1 input 0010 = Data from A2 input 0011 = Data from IV input 0100 = Data from B1 input 0101 = Data from B2 input 0110 = Data from IW input 0111 = Data from AN1 input 1000 = Data from AN2 input 1001 = Data from AN3 input 1010 = Data from AX input 1011 = Data from BX input 1100 = Unused 1101 = Unused 1110 = Unused 1111 = Unused
Bit 11−0:	**DATA11−0**: The output from the ADCs

In test mode, the upper four bits are copied from Bit 11 of the written data; see the *FIFO Test Register (24_H)* section.

3.6.2 Offset Registers (01_H to $0C_H$)

The Offset Registers are stored at the addresses 01_H to $0C_H$. The Offset Registers are 10 bits wide and represented in the two's complement format. The sign bit is copied in bit locations 15 to 10. This copy is only performed by a read access (that is, bits 15 to 10 must not be correctly set, in order to achieve the copy of the sign bit). The data format is shown in Table 1−13. The valid offset adjustment values are from –511 (201_H) to +511 ($1FF_H$). The value –512 (200_H) is not allowed.

Table 1−13. Offset Registers

R0	R0	R0	R0	R0	R0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
D9	D9	D9	D9	D9	D9	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−9:	**D9:** The MSB of the offset
Bit 8−0:	**D9−0:** The 10 bits of the offset value

3.6.3 Gain Registers ($0D_H$ to 18_H)

The Gain Registers are stored at the addresses $0D_H$ to 18_H. The Gain Registers are 12 bits wide. The gain value is stored in a straight binary format. The data format is shown in Table 1−14.

Table 1−14. Gain Registers

R0	R0	R0	R0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−12:	Always read as '0'; don't care at write
Bit 11−0:	**D11−0:** The 12 bits of the gain value

3.6.4 WINDAC Register (19_H)

The WINDAC Register is located in address 19_H. The WINDAC Register sets the output of the 8-bit DAC used by the window comparators. The word is in 8-bit straight binary format. The output voltage is a function of the register value and the internal reference voltage. (See Table 1−3.) The format of the data word is shown in Table 1−15.

Table 1−15. WINDAC Register

R0	R0	R0	R0	R0	R0	R0	R0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
D7	D7	D7	D7	D7	D7	D7	D7	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−8:	**D7**: MSB from DAC input data
Bit 7−0:	**D7−0**: The 8 bits input to Digital-to-Analog Converter

3.6.5 Control Register ($1A_H$)

The Control Register is located in address $1A_H$. The control register contains the input selection and the DAV pin control. (See the *FIFO* section for additional information.) The format of the Control Register is shown in Table 1−16. For more about the input selection, see the *Vecana Interface* section.

Table 1−16. Control Registers

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	RW0	R0	RW0	RW0	RW0
0	0	0	0	0	0	0	0	0	0	0	DAV	0	I2	I1	I0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−5, 3:	**Unused** (read as ‘0’); don’t care at write
Bit 4:	**DAV:** The 8 bits input to Digital-to-Analog Converter 1 = DAV signal active HIGH 0 = DAV signal active LOW
Bit 2−0:	**I2−0:** Input channel selection bits 000 = AN3 for ADC_3 001 = AX for ADC_1, BX for ADC_2, and AN3 for ADC3 010 = A2 via SH_1 for ADC_1, B2 via SH_3 for ADC_2 and AN2 for ADC_3 011 = A2 via SH_2 for ADC_1, B2 via SH_4 for ADC_2 and AN2 for ADC_3 100, 101, 110 = A1 for ADC_1, B1 for ADC_2 and AN1 for ADC_3 111 = IU for ADC_1, IV for ADC_2 and IW for ADC_3

3.6.6 Counter Control/Status Register ($1B_H$)

The Counter Control/Status Register is located in address 1_{BH}. The counter control/status register CCTRLSTAT is a combined control register for the filtered input of the counters and a status register for the over- or under-flow status of the counters and the filtered input signals strobed by $\overline{\text{HOLD1}}$. See the *Digital Counters* section for more information on this topic.

When the filter bits FxxE are set, the appropriate input is synchronized with the system clock and a digital filter processes the input signal. If the bit is reset, the signals are just synchronized.

The overflow states EOx/TOx are set when the appropriate counter has reached the value $FFFF_H$. This indicates when the time, between two edges of the input signals, is greater than 4ms at 16MHz. Only the time counter keeps its value until a counter reset is performed. See the *Reset Register* section for additional information.

The filtered values of the counter inputs CNTA2, CNTA1, CNTB2 and CNTB1 are sampled with the synchronous signal $\overline{\text{HOLD1}}$ and are stored in the appropriate bits FB1, FA1, FB2 and FA2. The format of the Counter Control/Status Register is described in Table 1−17.

Table 1−17. Counter Control/Status Register

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	RW1	RW1	RW1	RW1
FA1	FB1	FA2	FB2	0	0	0	0	EO2	TO2	EO1	TO1	FA2E	FB2E	FA1E	FB1E
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15:	**FA1:** Synchronously strobed FILTA1 signal
Bit 14:	**FB1:** Synchronously strobed FILTB1 signal
Bit 13:	**FA2:** Synchronously strobed FILTA2 signal
Bit 12:	**FB2:** Synchronously strobed FILTB2 signal
Bit 7:	**EO2**: EDGECNT2, over- or under-flow state 1 = when EDGECNT1 reached $FFFF_H$ 0 = when EDGECNT1 is other than $FFFF_H$
Bit 6:	**TO2**: TIMECOUNT2, over- or under-flow state 1 = when TIMECOUNT1 reached $FFFF_H$ 0 = when TIMECOUNT1 is other than $FFFF_H$
Bit 5:	**EO1**: EDGECNT1, over- or under-flow state 1 = when EDGECNT0 reached $FFFF_H$ 0 = when EDGECNT0 is other than $FFFF_H$
Bit 4:	**TO1**: TIMECOUNT1, over- or under-flow state 1 = when TIMECOUNT0 reached $FFFF_H$ 0 = when TIMECOUNT0 is other than $FFFF_H$
Bit 3:	**FA2E**: Enable of digital filter input CNTA2 1 = Input signal of CNTA2 will be filtered 0 = Input signal of CNTA2 will not be filtered
Bit 2:	**FB2E**: Enable of digital filter input CNTB2 1 = Input signal of CNTB2 will be filtered 0 = Input signal of CNTB2 will not be filtered
Bit 1:	**FA1E**: Enable of digital filter input CNTA1 1 = Input signal of CNTA1 will be filtered 0 = Input signal of CNTA1 will not be filtered
Bit 0:	**FB1E**: Enable of digital filter input CNTB1 1 = Input signal of CNTB1 will be filtered 0 = Input signal of CNTB1 will not be filtered

3.6.7 Edge Count Register ($1C_H$, $1D_H$, 20_H and 21_H)

There are four shadow registers for the two edge counters. The registers SYEDGCNT1 and SYEDGCNT2, synchronous edge count 1 (in address $1D_H$), and synchronous edge count 2 (in address 21_H), latch the values, from the edge counters, when the synchronous hold signal $\overline{\text{HOLD1}}$ is set to low.

Registers ASEDGCNT1, ASEDGCNT2, asynchronous edge count 1 (in address $1C_H$), and asynchronous edge count 2 (in address 20_H), latch the values from the edge counters when the asynchronous hold signal $\overline{\text{HOLD2}}$ is set to low.

An initial value is given to the edge counter 1, EDGECNT1, by writing into the register SYEDGCNT1. An initial value is given to the edge counter 2, EDGECNT2, by writing into the register SYEDGCNT2; see Table 1−18.

Table 1−18. Synchronous Latched Edge Count Register

RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	R−	R−
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−2:	**D15−2**: The 14 MSBs of the synchronous latched edge counters
Bit 1−0:	**D1−0**: The 2 LSBs of the synchronous latched edge counters. The value is adjusted to the value of the CNTAx and CNTBx by a write access to these registers or a reset condition.

CNTAx	CNTBx	EDGECNTx bit 1	EDGECNTx bit 0	Position of the Angle
0	0	0	0	1st Quadrant
1	0	0	1	2nd Quadrant
1	1	1	0	3rd Quadrant
0	1	1	1	4th Quadrant

The data can only be read from the asynchronous latched registers ASEDGCNT1 and ASEDGCNT2; see Table 1−19.

Table 1−19. Asynchronous Latched Edge Count Register

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−0:	**D15−0**: The 16 bits of the asynchronous latched edge counters

3.6.8 Edge Period Register ($1E_H$ and 22_H)

There are two read-only shadow registers for the two edge-period registers. The registers SYEDGPRD1 and SYEDGPRD2, synchronous edge period 1 (in address $1E_H$) and synchronous edge period 2 (in address 22_H), latch the values from the edge period registers when the synchronous hold signal $\overline{\text{HOLD1}}$ is set to low. The Edge Period Register is described in Table 1−20.

Table 1−20. Edge Period Register

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−0:	**D15−0**: The 16 bits of the synchronous latched edge period registers

3.6.9 Edge Time Period Register ($1F_H$ and 23_H)

There are two read-only shadow registers for the two edge time counters. The registers SYEDGTIME1 and SYEDGTIME2, synchronous edge time 1 (in address $1F_H$) and synchronous edge time 2 (in address 23_H), latch the values from the edge time counters when the synchronous hold signal $\overline{\text{HOLD1}}$ is set to low. The Edge Time Register is described in Table 1−21.

Table 1−21. Edge Time Period Register

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−0:	**D15−0**: The 16 bits of the synchronous latched edge time counters

3.6.10 FIFO Test Register (24_H)

The purpose of the FIFO Test Register, in address 24_H, is to test the FIFO during production test; the FIFO is filled with a defined pattern via this register. The internal FIFO structure can be verified by reading the patterns of the FIFO data register. When the FIFO test is enabled, the multiplexers are switched and lead the data (of the FIFO test register) into the FIFO, instead of the normal ADC data; to simulate the three ADCs, the data is latched into the FIFO three times. To distinguish between the channels, the first data is unchanged to simulate ADC_1, the second data is inverted to simulate ADC_2, and the six LSBs of the third data are inverted to simulate ADC_3. While the FIFO test is enabled, a total of three data words will be stored in the FIFO, with one write instruction. In order to fill the entire FIFO register with test data, 10 writes must be performed. The test data is written into the FIFO only when the four enable bits have the value A_H. **This register should not be used in normal operation.** The format of the output word is shown in Table 1−22.

Table 1−22. FIFO Test Register

RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0	RW0
E3	E2	E1	E0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−12:	**E3−0:** Input channel address bits 0000 = Disable FIFO test ... 1001 = Disable FIFO test 1010 = Enable FIFO test write procedure 1011 = Disable FIFO test ... 1111 = Disable FIFO test
Bit 11−0:	**DATA11−0:** The input data that will be written into the FIFO registers

In FIFO test mode the four channel bits are copied from Bit 11 of the written data.

3.6.11 Comparator Test Register (25_H)

The purpose of the Comparator Test Register, in address 25_H, is to apply a defined pattern to the comparator output pins. This feature is for testing algorithms in the DSP or testing the hardware controlled by the comparator outputs. To enable the comparator test, the enable part of the register must contain the value $0C_H$. **This register should not be used in normal operation.** By reading the Comparator Test register, the comparator outputs are sent back in order to allow the host to read the actual comparator outputs in one cycle. The format of the output word is shown in Table 1−23.

Table 1−23. Comparator Test Register

RW0	RW0	RW0	RW0	RW0	RW0	RW−	RW−	RW−	RW−	RW−	RW−	RW−	RW−	RW−	RW−
E5	E4	E3	E2	E1	E0	A1/B2	B1	A2	B2/A1	UC	VC	WC	UI	VI	WI
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−10:	**E5−0:** Input channel address bits 000000 = Disable COMPARATOR_TEST ... 001011 = Disable COMPARATOR_TEST 001100 = Enable COMPARATOR_TEST write procedure 001101 = Disable COMPARATOR_TEST ... 111111 = Disable COMPARATOR_TEST
Bit 9:	**A1**: Control bit of position sensor, sign comparator A1 output 1 = Comparator output A1, set HIGH 0 = Comparator output A1, set LOW By reading this bit, comparator output B2 is read
Bit 8:	**B1**: Control bit of position sensor, sign comparator B1 output 1 = Comparator output B1, set HIGH 0 = Comparator output B1, set LOW
Bit 7:	**A2**: Control bit of position sensor, sign comparator A2 output 1 = Comparator output A2, set HIGH 0 = Comparator output A2, set LOW
Bit 6:	**B2**: Control bit of position sensor, sign comparator B2 output 1 = Comparator output B2, set HIGH 0 = Comparator output B2, set LOW By reading this bit, comparator output A1 is read
Bit 5:	**UC**: Control bit phase U current sign comparator 1 = Comparator output U_COMP, set HIGH 0 = Comparator output U_COMP, set LOW
Bit 4:	**VC**: Control bit phase V current sign comparator 1 = Comparator output V_COMP, set HIGH 0 = Comparator output V_COMP, set LOW
Bit 3:	**WC**: Control bit phase W current sign comparator 1 = Comparator output W_COMP, set HIGH 0 = Comparator output W_COMP, set HIGH
Bit 2:	**UI**: Control bit phase U current window comparator 1 = Comparator output U_ILIM, set HIGH 0 = Comparator output U_ILIM, set LOW
Bit 1:	**VI**: Control bit phase V current window comparator 1 = Comparator output V_ILIM, set HIGH 0 = Comparator output V_ILIM, set LOW
Bit 0:	**WI**: Control bit phase W current window comparator 1 = Comparator output W_ILIM, set HIGH 0 = Comparator output W_ILIM, set LOW

3.6.12 Interrupt Register (26_H)

The Interrupt Register, in address 26_H, contains the interrupt source and interrupt control bits. The bits xOxF are set when a particular counter had an over- or under-flow. The bits remain set until the Interrupt Register is read; this is independent of whether the counter over- or under-flow states remain or not. The counter over- or under-flow interrupt is enabled when the appropriate xOxE bits are set.

The FFF bit, FIFO full flag, will be set when the FIFO is (or was) full and remains set until the Interrupt Register is read, independent of whether the FIFO is full or not. The FF bit, FIFO full, indicates whether the FIFO is full or not. The FFF bit is cleared when the Interrupt Register is read. The FIFO full interrupt is enabled when the bit FFE (or FIFO full enable) is set.

The FEF bit, FIFO empty flag, will be set when the FIFO is (or was) empty and remains set until the Interrupt Register is read, independent of whether the FIFO is empty or not. The FE bit, FIFO empty, indicates if the FIFO is empty or not. The bit FEF is cleared when the Interrupt Register is read. The FIFO empty interrupt is enabled when the FEE bit , FIFO empty enable, is set. For more information about the Interrupt pin, see the *Interrupt* section. Table 1−24 describes the Interrupt Register.

Table 1−24. Interrupt Register

RW0	RW0	RW0	RW0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	RW0	RW0
EO2E	TO2E	EO1E	TO1E	EO2F	TO2F	EO1F	TO1F	0	0	FF	FE	FFF	FEF	FFE	FEE
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15:	**EO2E**: Edge counter 2, EDGECNT2, over- or under-flow interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable
Bit 14:	**TO2E**: Time counter 2, TIMECOUNT2, over- or under-flow interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable
Bit 13:	**EO1E**: Edge counter 1, EDGECNT1, over- or under-flow interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable
Bit 12:	**TO1E**: Time counter 1, TIMECOUNT1, over- or under-flow interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable
Bit 11:	**EO2F**: Edge counter 2, EDGECNT2, over- or under-flow flag 1 = EDGECNT2 over- or under-flow occurred 0 = EDGECNT2 over- or under-flow did not occur
Bit 10:	**TO2F**: Time counter 2, TIMECOUNT2, over- or under-flow flag 1 = TIMECOUNT2 over- or under-flow occurred 0 = TIMECOUNT2 over- or under-flow did not occur
Bit 9:	**EO1F**: Edge counter 1, EDGECNT1, over- or under-flow flag 1 = EDGECNT1 over- or under-flow occurred 0 = EDGECNT1 over- or under-flow did not occur
Bit 8:	**TO1F**: Time counter 1, TIMECOUNT1, over- or under-flow flag 1 = TIMECOUNT1 over- or under-flow occurred 0 = TIMECOUNT1 over- or under-flow did not occur
Bit 7−6:	**Unused** (read as ‘0’)

Interrupt Register, continued

Bit 5:	**FF**: FIFO full state 1 = FIFO is full 0 = FIFO is not full
Bit 4:	**FE**: FIFO empty state 1 = FIFO is empty 0 = FIFO is not empty
Bit 3:	**FFF**: FIFO full flag 1 = FIFO is or was full 0 = FIFO is not or was not full
Bit 2:	**FEF**: FIFO empty flag 1 = FIFO is or was empty 0 = FIFO is not or was not empty
Bit 1	**FFE**: FIFO full interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable
Bit 0:	**FEE**: FIFO empty interrupt enable bit 1 = Interrupt enable 0 = Interrupt disable

3.6.13 Parallel Register (27_H)

The Parallel Register, in address 27_H, controls the parallel interface mode 11; see the *Mode 11 Bus Access* sections. The Parallel Register has no effect on modes 00, 01, and 10. There is only one bit present in the Parallel Register, the M bit. The format of the Parallel Register is shown in Table 1−25.

Table 1−25. Parallel Register

R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	RW1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	M
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−1:	**Unused** (read as ‘0’)
Bit 0:	**M**: Set up the type of the parallel interface 1 = Parallel interface, mode 11 (default) 0 = TMS320c54xx DSP family-compatible parallel interface

3.6.14 Reset Register (28_H)

The Reset Register, in address 28_H, can either reset the ADS7869 entirely, or simply reset the counters. Writing an AA_H pattern to the C_X bits will reset both counter 1 and counter 2, and all registers related to the counters. Writing an AA_H pattern to the S_X bits forces the ADS7869 into a reset state; both the digital and the analog sections are reset. The Reset Register is a write-only register. If the Reset Register is read, the data 0000_H will be received. The format of the input word is shown in Table 1−26. To reset the complete ADS7869, the pattern $AAAA_H$ should be written to the Reset Register.

Once the Reset Register activates a system reset, the register must not be rewritten to in order to deactivate the reset condition. Writing another pattern to the C_X bits (other than AA_H) deactivates a reset condition of the counters or a reset condition of the device.

For more information about reset conditions, see the *Reset* section.

Table 1−26. Reset Register

W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0
S7	S6	S5	S4	S3	S2	S1	S0	C7	C6	C5	C4	C3	C2	C1	C0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit 15−8:	**S7−0:** Reset control of entire ADS7869 (both digital and analog sections) 00000000 = No effect on ADS7869 ... 10101001 = No effect on ADS7869 10101010 = Reset entire ADS7869 10101011 = No effect on ADS7869 ... 11111111 = No effect on ADS7869
Bit 7−0:	**C7−0**: Reset control of both counters and related registers of ADS7869 00000000 = No effect on ADS7869 ... 10101001 = No effect on ADS7869 10101010 = Reset both counters in ADS7869 10101011 = No effect on ADS7869 ... 11111111 = No effect on ADS7869

3.7 FIFO

The FIFO of the ADS7869 is organized as a 32-word ring buffer with 16 bits per word, shown in Figure 1−20.

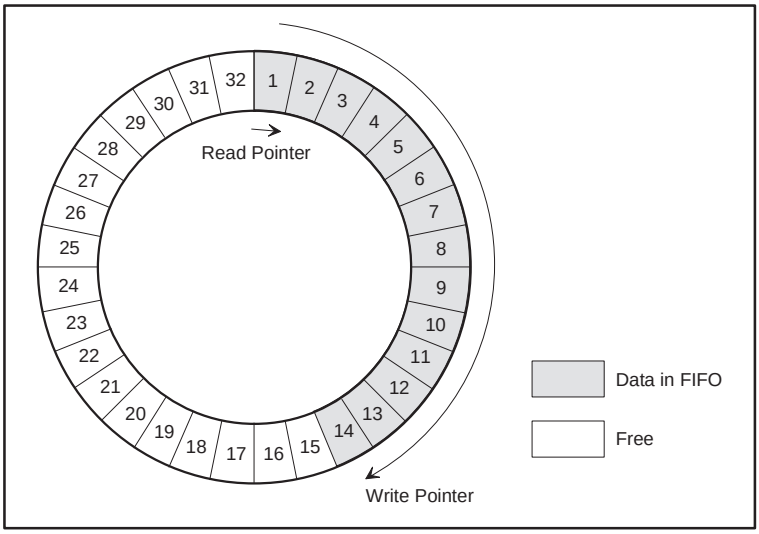


Figure 1−20. FIFO Structure

The converted data of the ADS7869 is automatically written into the FIFO. To control the writing and reading process, a write pointer and a read pointer are used. The read pointer always shows the location that contains the last read data. The write pointer indicates the location that contains the last written sample. The converted values are written in a predefined sequence to the circular buffer, beginning with ADC_1 and ending with ADC_3. The channel number is stored with the ADC data. The data of the FIFO is read through the FIFO register at address 00_H; its format is presented in Table 1−27. The table shows that the channel information for the converted channel data, is continually maintained. The address 00_H in the register map shows only the data to which the read pointer is directed.

The FIFO generates the DAV signal; see Figure 1−22 on page 51. In VECANA mode, this signal is low; it indicates that the ADS7869 is converting data (see Figure 1−10 on page 26). In the other modes, the DAV indicates that data in the FIFO is available. The DAV signal can be configured as either a positive or negative signal; see the *Control Register* section.

Table 1−27. FIFO 16-bit Data Read Format

ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00_H	0	0	0	0	ADC_1 value, channel IU, included offset and gain compensation											
00_H	0	0	0	1	ADC_1 value, channel A1, included offset and gain compensation											
00_H	0	0	1	0	ADC_1 value, channel A2, included offset and gain compensation											
00_H	0	0	1	1	ADC_2 value, channel IV, included offset and gain compensation											
00_H	0	1	0	0	ADC_2 value, channel B1, included offset and gain compensation											
00_H	0	1	0	1	ADC_2 value, channel B2, included offset and gain compensation											
00_H	0	1	1	0	ADC_3 value, channel IW, included offset and gain compensation											
00_H	0	1	1	1	ADC_3 value, channel AN1, included offset and gain compensation											
00_H	1	0	0	0	ADC_3 value, channel AN2, included offset and gain compensation											
00_H	1	0	0	1	ADC_3 value, channel AN3, included offset and gain compensation											
00_H	1	0	1	0	ADC_1 value, channel AX, included offset and gain compensation											
00_H	1	0	1	1	ADC_2 value, channel BX, included offset and gain compensation											
00_H	1	1	0	0	Not existing											
00_H	1	1	0	1	Not existing											
00_H	1	1	1	0	Not existing											
00_H	1	1	1	1	Not existing											

The DAV signal becomes active when the write pointer is ahead of the read pointer. The DAV signal becomes inactive again when the read pointer equals the write pointer (that is, when the FIFO is empty).

When the ADCs are writing data into the FIFO, and the write pointer is more than 32 steps ahead of the read pointer, a FF (FIFO Full) state will be set. FF is cleared when the first FIFO read operation is performed. To synchronize the pointers after an FF state, the FIFO should be read out until a FE (FIFO Empty) occurs.

If a read is attempted, while the read and write pointers are equal, the read pointer will not increase; the same data (the data with the same channel number) is read again. When this occurs, an FE state is set. The FE state is cleared when new data is written into the FIFO. The read pointer will not go beyond the write pointer. Both FF and FE go into the Interrupt section. The functional block diagram of the FIFO is shown in Figure 1−21.

The purpose of the test data is to verify the FIFO structure for the development of an application. This is described in the *FIFO Test Register* section. **This register should not be used in normal operation.**

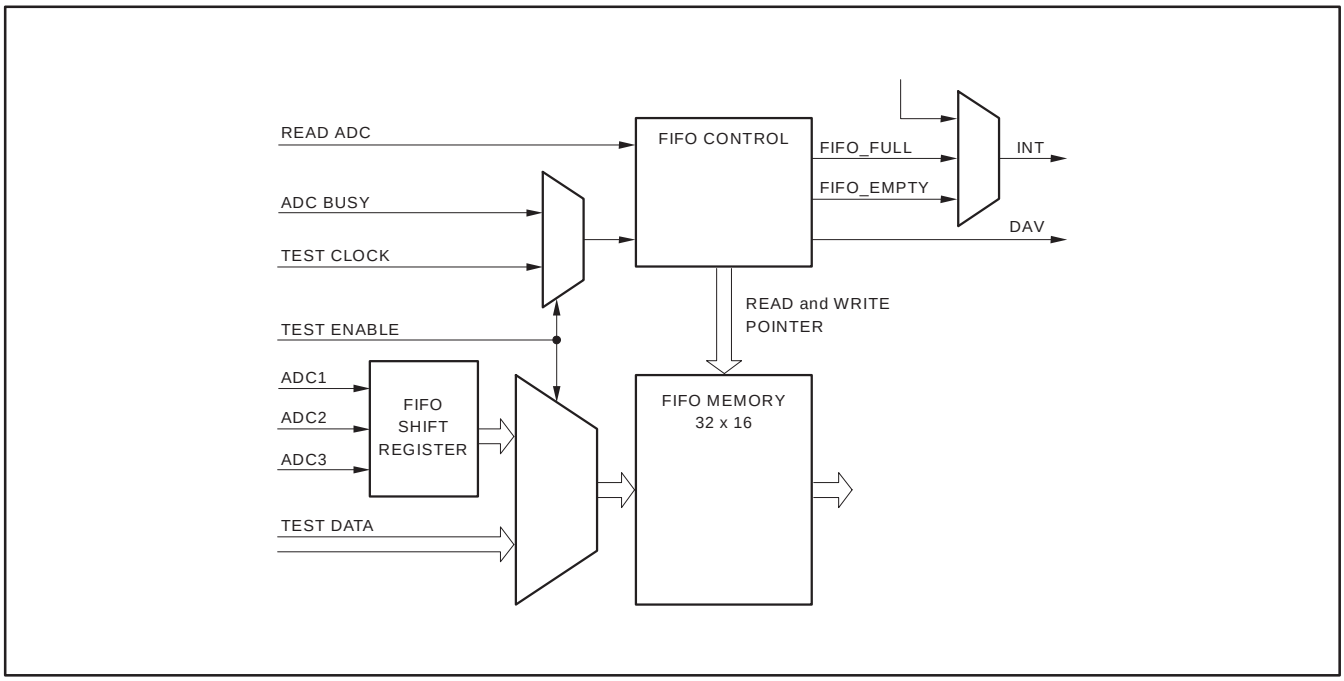


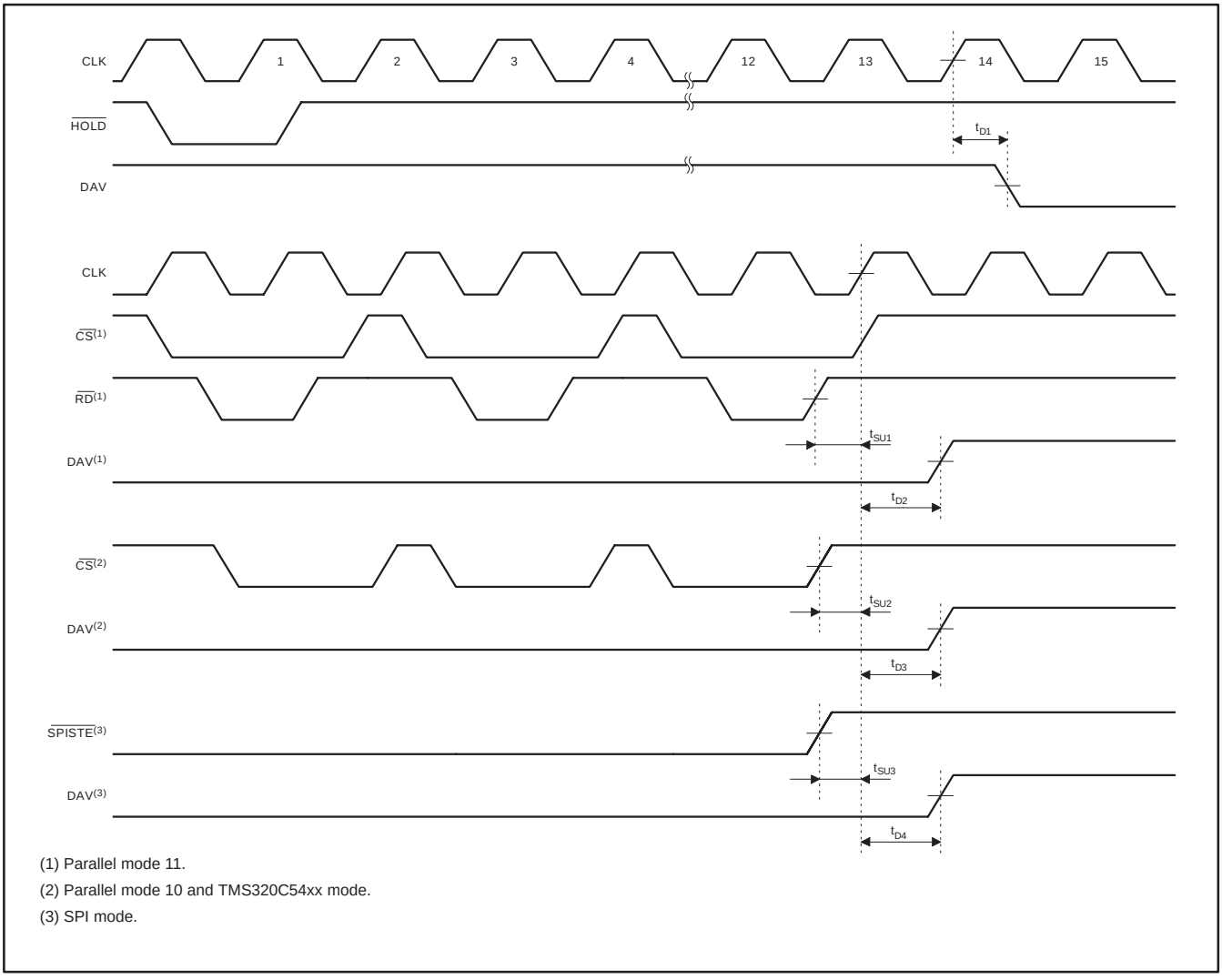
Figure 1−21. FIFO Block Diagram

3.7.1 DAV Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Delay time from 14th rising CLK to falling DAV(2)	t_{D1}		50	ns
Setup time from $\overline{RD}$ HIGH to next rising CLK	t_{SU1}	8		ns
Delay time from rising CLK to rising DAV(2)(3)	t_{D2}		50	ns
Setup time from $\overline{CS}$ HIGH to next rising CLK	t_{SU2}	8		ns
Delay time from rising CLK to rising DAV(2)(3)	t_{D3}		50	ns
Setup time from $\overline{SPISTE}$ HIGH to next rising CLK	t_{SU3}	8		ns
Delay time from rising CLK to rising DAV(2)(3)	t_{D4}		50	ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) With the DAV bit in the Control register (14_H), the DAV signal can have opposite polarity.
(3) Only applicable when the last data is read from the FIFO



(1) Parallel mode 11.
(2) Parallel mode 10 and TMS320C54xx mode.
(3) SPI mode.

Figure 1−22. Timing of the DAV Signal

3.8 Digital Counter Modules

The interface of the ADS7869 for the analog position sensors has the following features:

- Up to 16MHz operation frequency
- Error-safe state machine for fully four-quadrant decoding
- High noise immunity:
  - Differential signal inputs
  - Analog input comparators with hysteresis
  - Schmitt trigger digital inputs
- Digital Noise Filter
- 16-bit binary Up/Down counters with over- and under-flow detection
- Synchronous to the system clock
- Asynchronous and synchronous latching of the counter values at the same time as the ADC values are sampled and held
- Five shadow registers

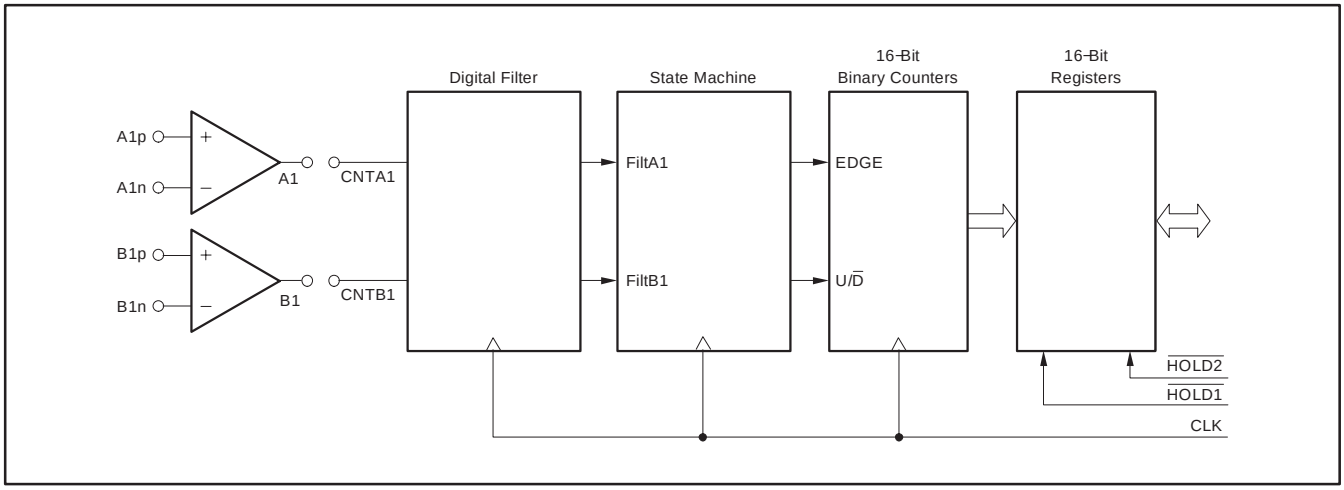


Figure 1−23. Block Diagram of a Counter Module

3.8.1 Operation

Analog position sensors have two signals on the output, sine and cosine. Both signals are differential and positioned at 90 electrical degrees to each other. The sign comparators, with typically 75mV hysteresis, process the position sensor output differential signal. This dramatically reduces the common-mode noise, which is present in motor control applications. The digital output signal from the comparator is connected to the counter input. Extra noise suppression is obtained with Schmitt trigger inputs. The digital signals are carried through a programmable digital filter. The filtered, glitch-free signals are processed by a state machine, which increments or decrements the counters. The counter values are then latched into corresponding registers by the synchronous or asynchronous hold signals $\overline{\text{HOLD1}}$ and $\overline{\text{HOLD2}}$.

There is a counter module implemented for each pair of position sensor signals (A1, B1 and A2, B2). These counters can count upwards or downwards, depending on the direction of the position sensor signal (that is, the phase difference of the signals A1 and B1, respectively, or A2 and B2). These counter values are stored in shadow registers when the ADC channels are sampled and held. The four position sensor channels and the counter values are all sampled at the same time on the $\overline{\text{HOLD1}}$ or $\overline{\text{HOLD2}}$ signal.

With a 16MHz system clock, the maximum data rate that the counters will operate at is 2MHz.

3.8.2 Digital Noise Filter

A digital noise filter rejects noise on the incoming quadrature signal. The digital noise filter rejects large, short duration, noise spikes; false counts, triggered by noise or spikes, are also significantly suppressed. See Figure 1−24.

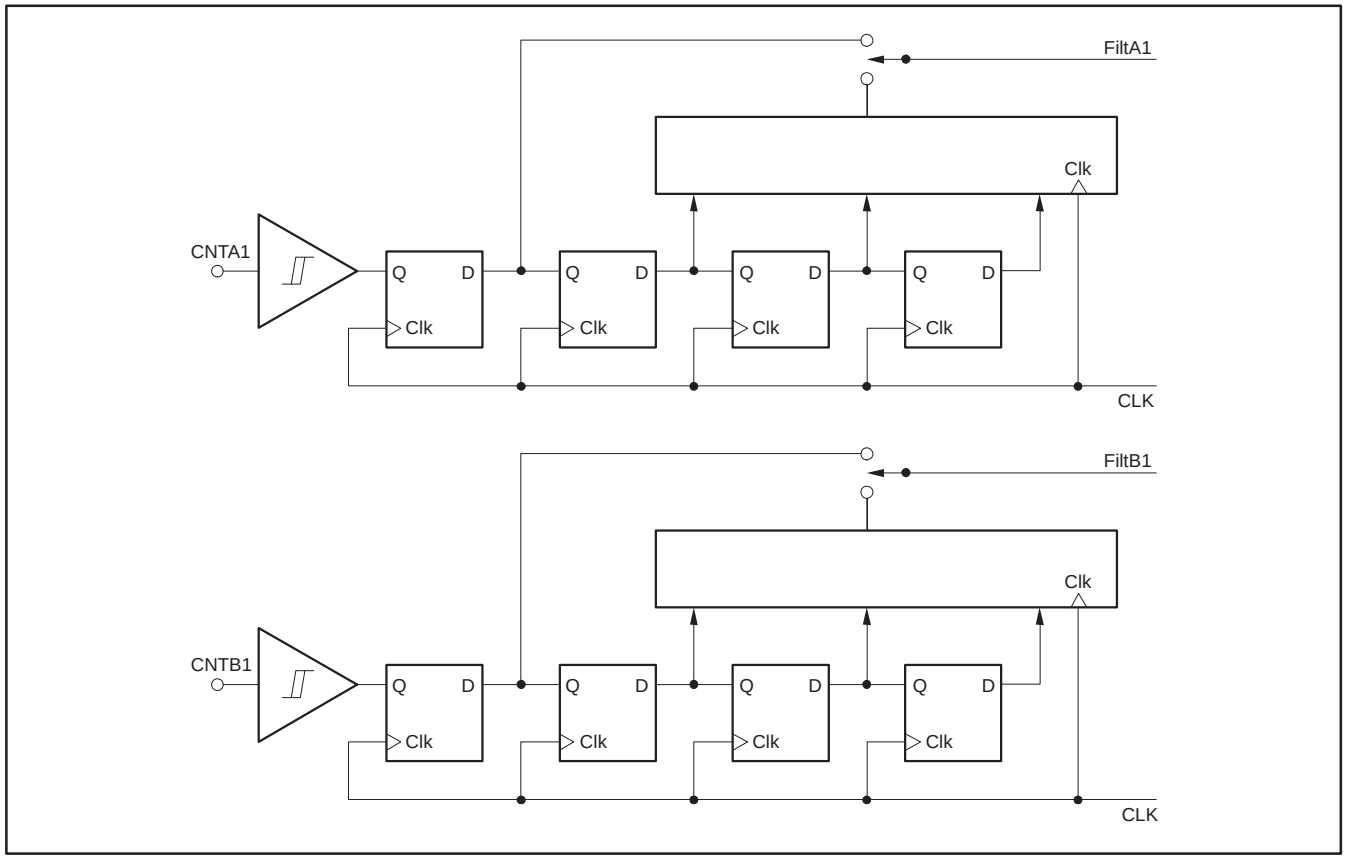


Figure 1−24. Digital Noise Filter Block Diagram

The input signals, Cnt_{XY}, are sampled on the rising clock edge. Before the signals are passed to the state machine, the signals must be stable for a minimum of three consecutive rising clock edges. Pulses shorter than two clock periods are rejected; glitches between rising clock edges are also ignored. See Figure 1−25.

3.8.2.1 Filtered Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLK Period	t_{C1}	62.5		ns
Counter input signal, CNTA1 or CNTB1, Period	t_{C2}	8		t_{C1}
Counter input signal, CNTA1 or CNTB1, HIGH or LOW time	t_{W2}	4		t_{C1}
Delay between CNTA1 or CNTB1 signal, any combination	t_{D1}	2		t_{C1}
Filtered noise spike on CNTA1 or CNTB1 input HIGH or LOW Time	t_{W3}		2	t_{C1}

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

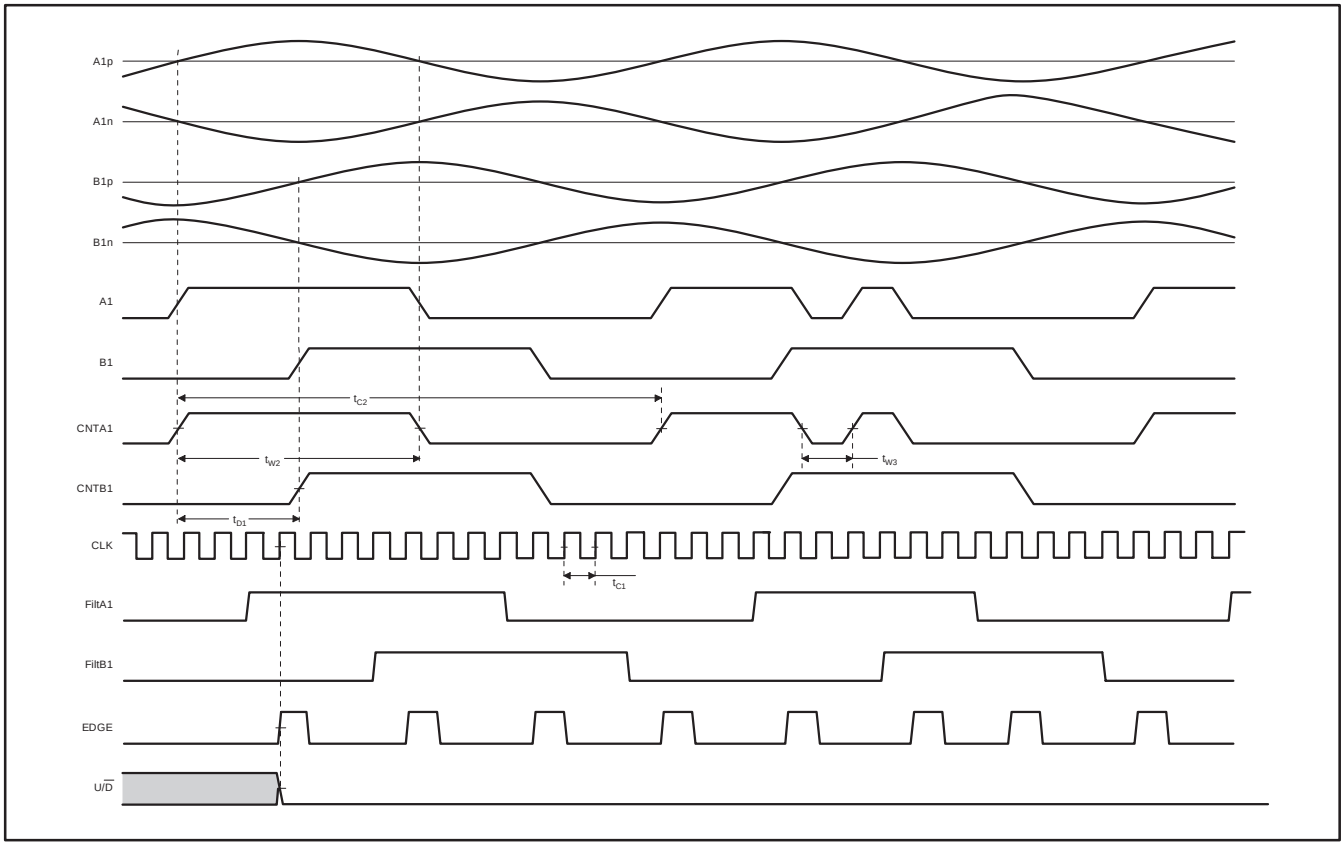


Figure 1−25. Timing Diagram of the Counter Signals with the Digital Noise Filter Enabled

3.8.2.2 Unfiltered Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLK Period	t_{C1}	62.5		ns
Counter input signal, CNTA1 or CNTB1, Period	t_{C2}	8		t_{C1}
Counter input signal, CNTA1 or CNTB1, HIGH or LOW time	t_{W2}	4		t_{C1}
Delay between CNTA1 or CNTB1 signal, any combination	t_{D1}	2		t_{C1}

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

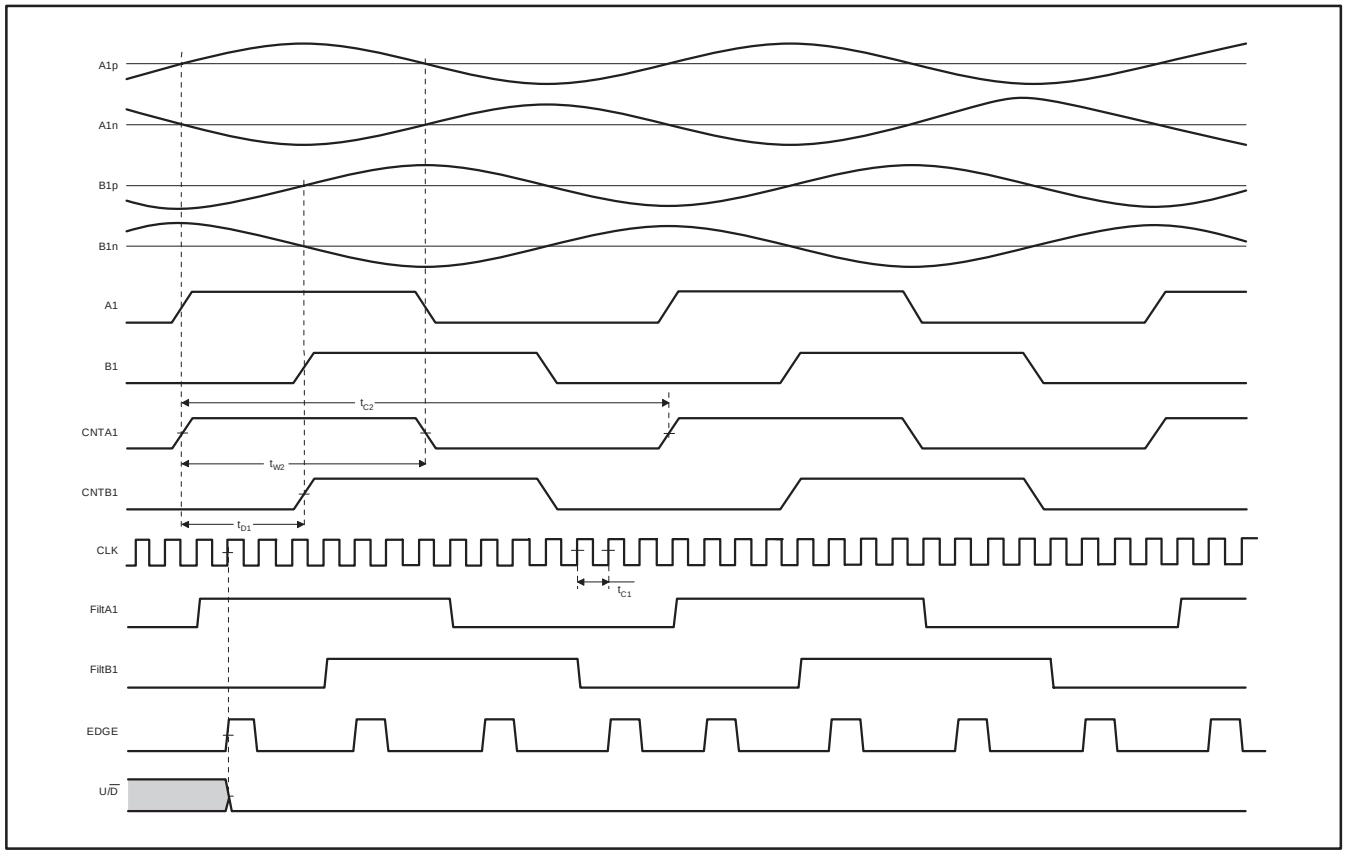


Figure 1−26. Timing Diagram of the Counter Signals with the Digital Noise Filter Disabled

3.8.3 Binary Counters and Registers

The complete up/down counter includes two 16-bit counters and five 16-bit shadow registers. The first counter is a 16-bit up/down counter, which counts upwards or downwards on the EDGE input signal as a function of the U/$\overline{D}$ signal. This is the coarse angle counter, and it is called EDGECNT. For the fine angle computation, the second 16-bit counter, TIMECOUNT, is implemented. This counter increments with the system clock and resets when the EDGE signal occurs. The TIMECOUNT counter cannot be decremented. The system is shown in Figure 1−27 and the timing is shown in Figure 1−28. The U/$\overline{D}$ signal is high, counting upwards, when B1 runs before A1. The U/$\overline{D}$ signal is low, counting downwards, when A1 runs before B1. The EDGE signal is set by every filtered edge of A1 and B1.

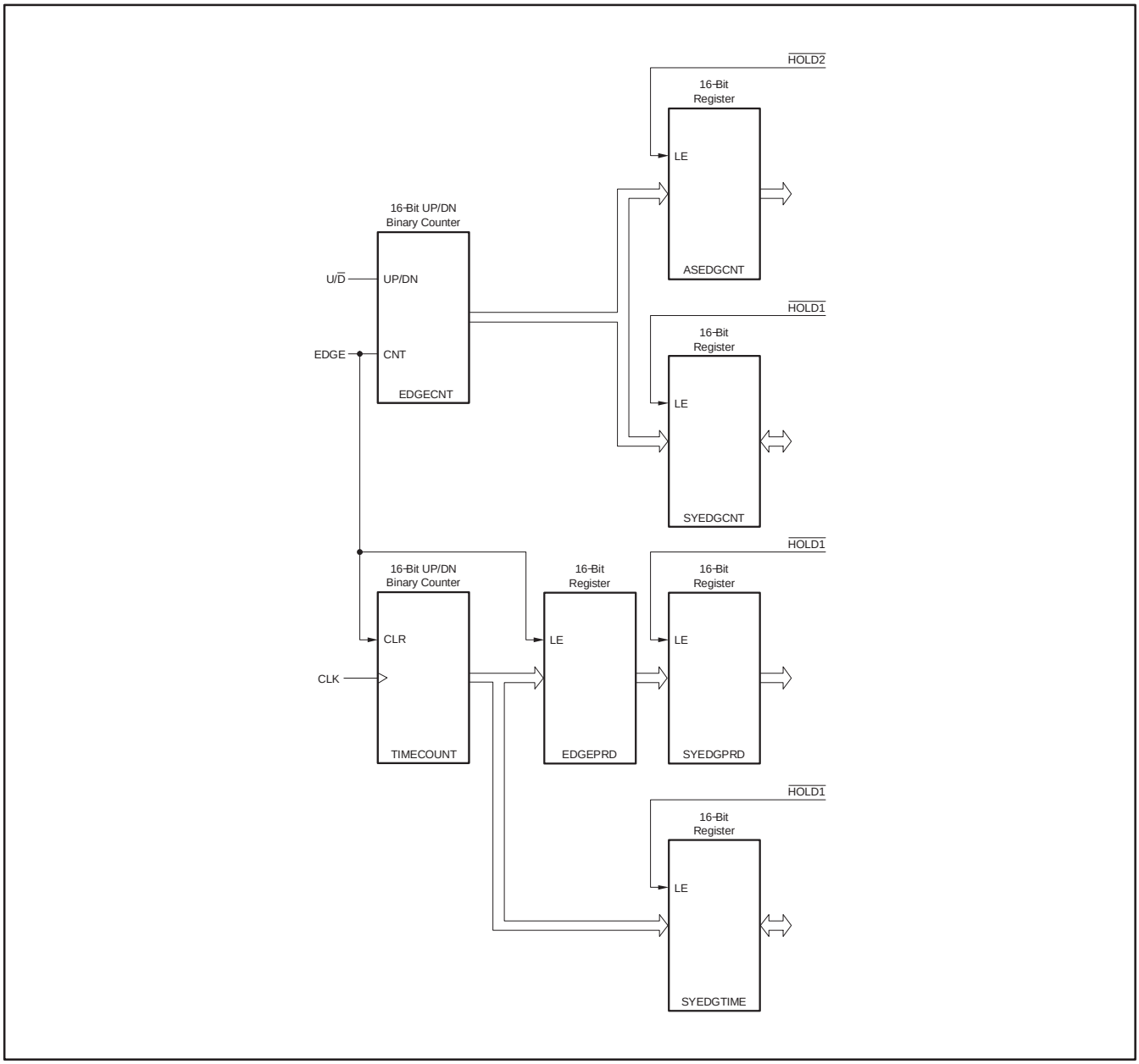


Figure 1−27. Detail Counter Block Diagram

When EDGECNT cause an over- or under-flow, the corresponding bit in the Interrupt Register is set. The counter continues to increment or decrement in value. When the EDGE signal rises, the TIMECOUNT value is latched into the shadow register EDGEPRD. The value of EDGEPRD is the number of system clocks between two valid edges of the input signals from the comparators. This value is reciprocally proportional to the angular speed of the position sensor. The value in the EDGEPRD register is latched in the SYEDGPRD Register on the synchronous hold signal, $\overline{\text{HOLD1}}$.

The EDGECNT and TIMECOUNT counter values are stored into the shadow registers (SYEDGCNT and SYEDGPRD) with the synchronous hold signal, $\overline{\text{HOLD1}}$, which samples the analog inputs. The value of the SYEDGTIME Register represents the time between the last EDGE signal and the synchronous hold signal $\overline{\text{HOLD1}}$. The EDGECNT counter value is stored into a shadow register ASEDGCNT on the asynchronous sample signal $\overline{\text{HOLD2}}$.

The shadow registers SYEDGCNT, ASEDGCNT, SYEDGPRD and SYEDGTIME can be read through the register map. The counter EDGECNT can be written through the address of the SYEDGCNT Register in the register map. The 14 MSBs of the written data are stored in the EDGECNT register. The two LSBs are determined from the inputs FiltA1 and FiltB1; see the *Edge Count Register* section. This is to prevent inconsistency between the EDGECNT counters and the ADC data of the position sensor input signals.

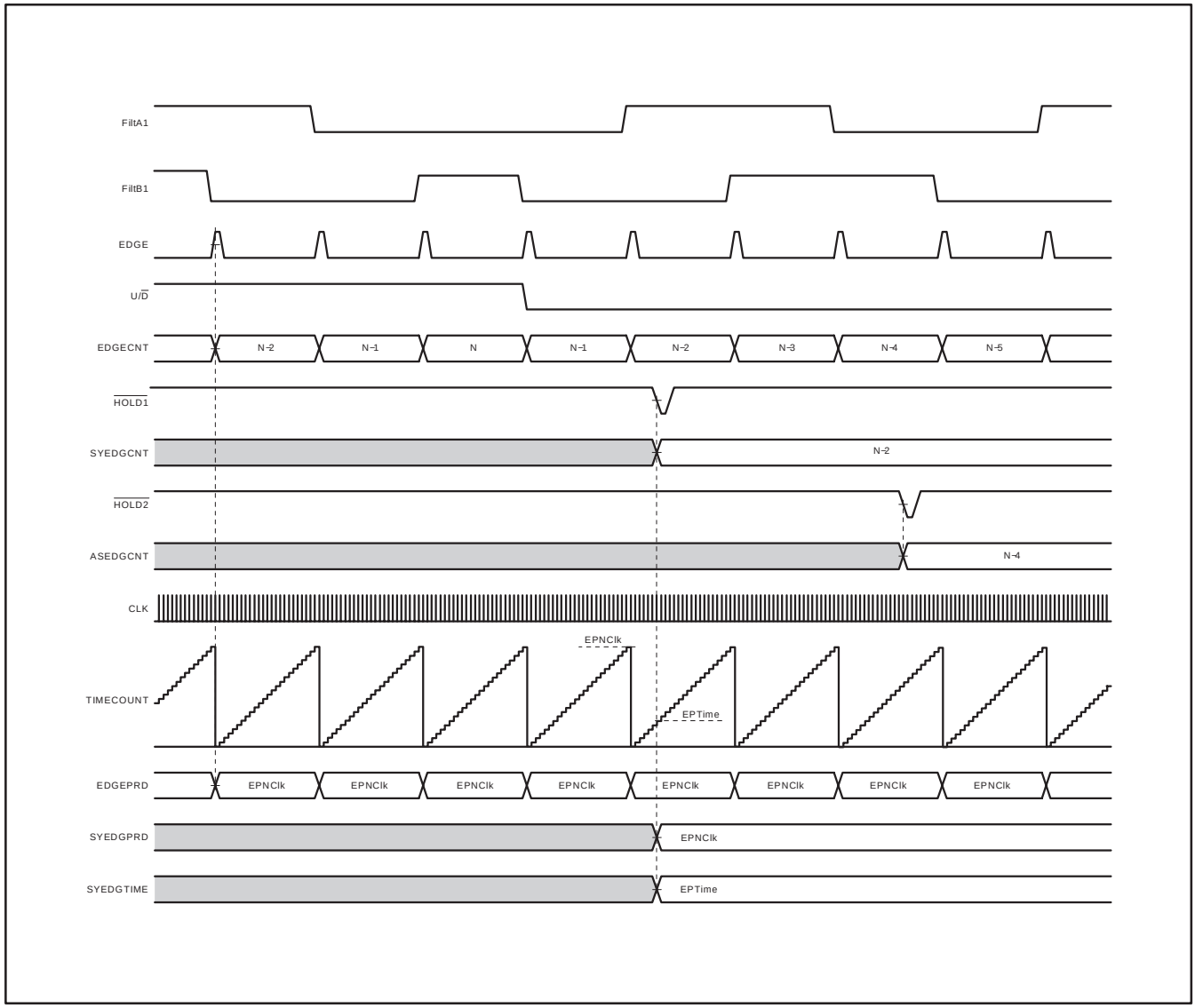


Figure 1−28. Detail Counter Timing Diagram

3.9 Interrupt

The interrupt can have several sources:

- FIFO full status
- FIFO empty status
- Two TIMECOUNT over- or under-flows
- Two EDGECOUNT over- or under-flows

These six sources are combined into one interrupt signal. The interrupt signal is active high; when the interrupt pin INT is high, one of the six sources is also high.

To reset an interrupt, the Interrupt Register must be read (see *Interrupt Register* section), in order to allow the host to determine which source, or sources, caused the interrupt.

3.10 Reset

The ADS7869 can be forced into a reset state in three different ways:

- Power-on.
- Pulling the $\overline{RST}$ pin (reset pin 79) low.
- Writing to the Reset Register.

In addition, the digital counters can be reset via the Reset Register, without resetting the entire ADS7869.

In a reset state, the analog inputs are sampled, the registers (in the register map) are forced into their reset values, and the FIFO and the counters are cleared. One rising clock pulse during a reset condition is necessary to reset the synchronous counters.

It takes one clock cycle for the ADS7869 to begin the normal operation after the last reset condition is cleared. (See Figure 1−29.)

3.10.1 Reset Timing Characteristics(1)

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V − 5V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Setup time from RST LOW to rising CLK	t_{SU1}	10		ns
Hold time from rising CLK to RST HIGH	t_{H1}	5		ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

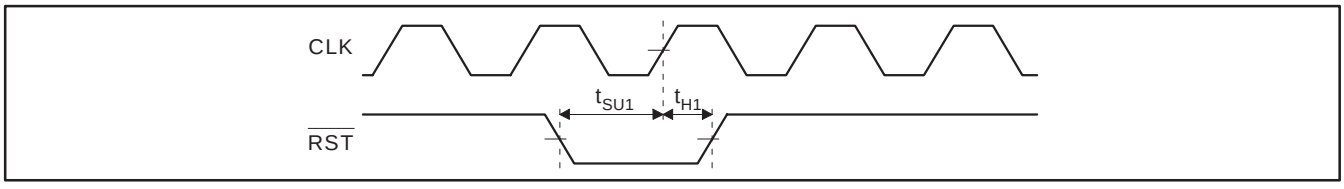


Figure 1−29. Timing Diagram of the Reset Signal $\overline{RST}$

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
7/06	E	2	Ordering Information	Changed ordering number and transport media.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7869IPZT	ACTIVE	TQFP	PZT	100	90	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS7869I	Samples
ADS7869IPZTR	ACTIVE	TQFP	PZT	100	1000	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS7869I	Samples
ADS7869IPZTRG4	ACTIVE	TQFP	PZT	100	1000	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS7869I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

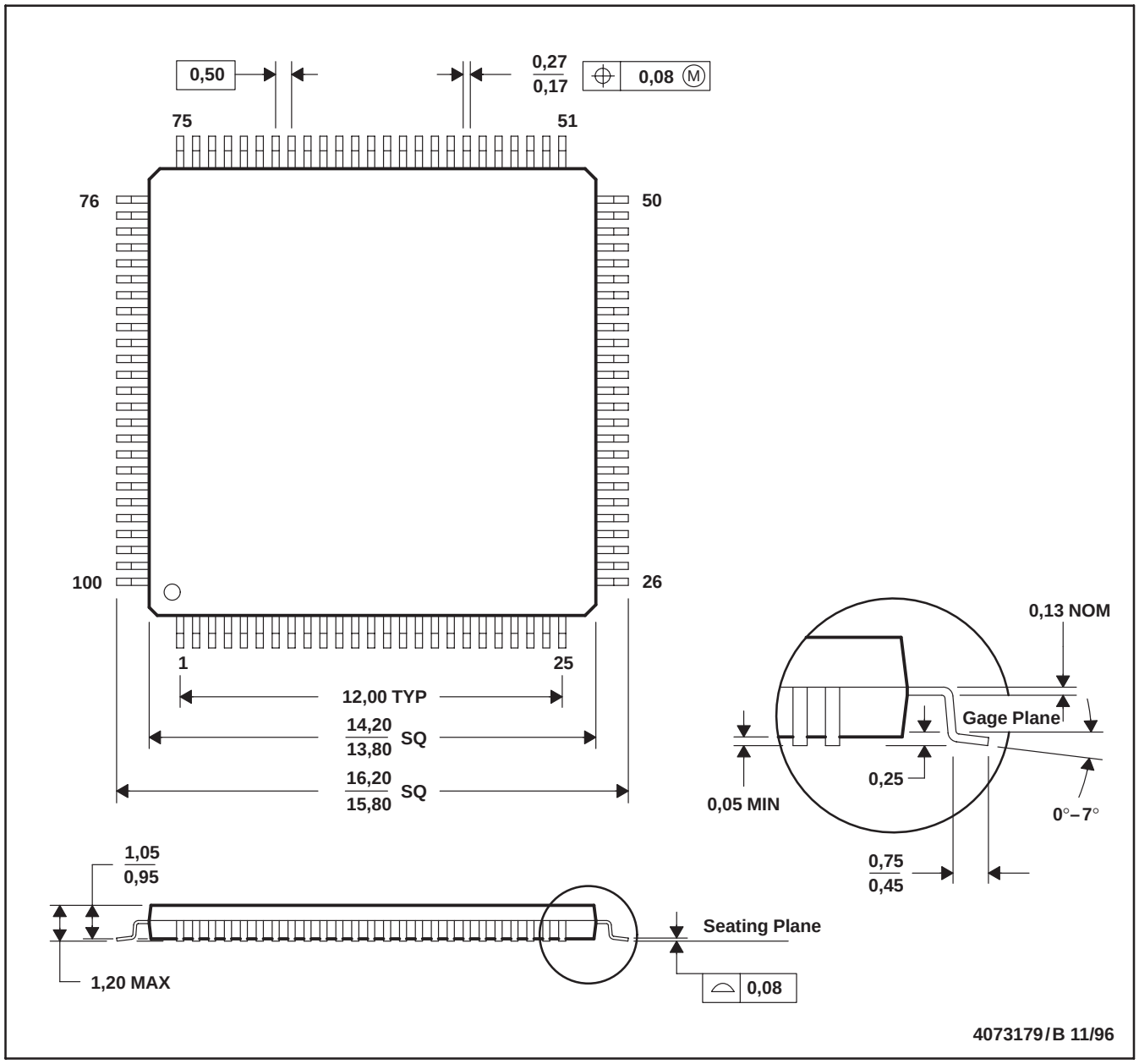
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MTQF012B – OCTOBER 1994 – REVISED DECEMBER 1996

PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265