IXYS
INTEGRATED CIRCUITS DIVISION

IX4340NE
Automotive Grade 5-Ampere, Dual Low-Side MOSFET Driver

Features

- AEC-Q100 qualified
- Two independent drivers, each capable of sourcing and sinking 5A
- 5V to 20V supply voltage range
- AEC-Q100 Grade 1 -40°C to +125°C operating temperature range
- AEC-Q100 Classification 3A ±4kV ESD rating (Human Body Model)
- Thermally enhanced 8-pin SOIC package
- CMOS and TTL compatible inputs
- Independent enable for each driver
- Under voltage lockout circuitry
- Fast propagation delays (16ns typical)
- Fast rise and fall times (7ns typical)

Applications

- On-board chargers
- DC-DC converters
- Electric vehicle charging stations
- Motor controllers
- Power inverters

Description

The IX4340NE is an automotive grade, AEC-Q100 qualified dual, high current, low side gate driver. Each of the two outputs is capable of sourcing and sinking 5A of peak current, and has a maximum voltage rating of 20V. The two outputs can be paralleled for higher current applications. Fast propagation delay times (16ns typical) and fast rise and fall times (7ns) make the IX4340NE well suited for high frequency applications.

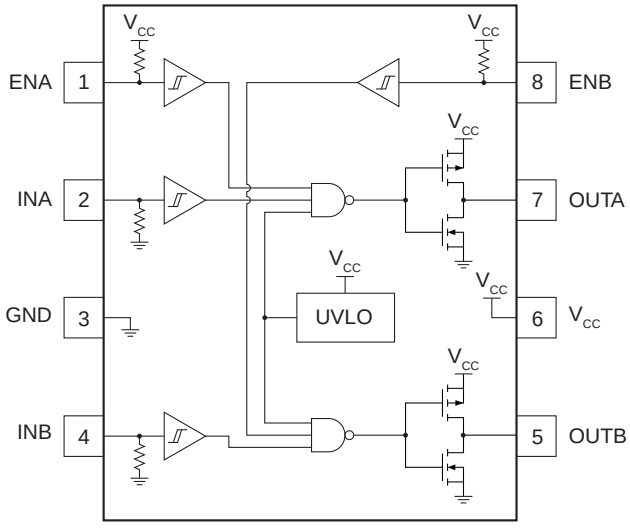
The inputs are TTL and CMOS logic compatible, and there is an independent Enable function for each output. Under voltage lockout circuitry (UVLO) prevents the high side source driver from conducting until there is sufficient supply voltage. The outputs are held low if the logic inputs are floating.

The IX4340NE is available in a thermally enhanced 8-pin SOIC package.

Ordering Information

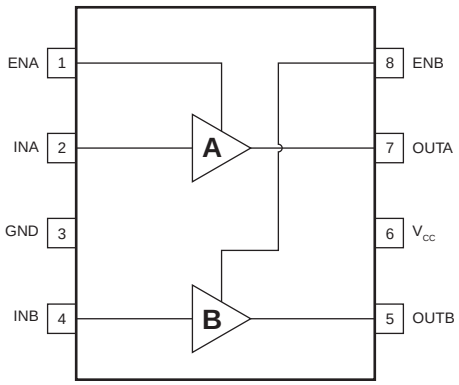
Part Number	Description
IX4340NE	8-Pin SOIC w/ Exposed Thermal Pad (100/Tube)
IX4340NETR	8-Pin SOIC w/ Exposed Thermal Pad (4000/Reel)

IX4340NE Functional Block Diagram



1 Specifications

1.1 Pin Configuration



1.2 Logic Table

IXx	ENx	V_{CC}	OUTx
1	1	V_{CC}>$UVLO_{ON}$	1
0	1	V_{CC}>$UVLO_{ON}$	0
x	0	V_{CC}>$UVLO_{ON}$	0
x	x	V_{CC}<$UVLO_{ON}$	0

1.3 Pin Definitions

Pin #	Name	Description
1	ENA	Enable input for Channel A. A logic high (or floating) enables Channel A (the state of OUTA is determined by INA). A logic low disables OUTA (OUTA held low regardless of INA).
2	INA	Channel A logic input. Internally pulled to GND.
3	GND	Ground. Common ground reference for the device.
4	INB	Channel B logic input. Internally pulled to GND.
5	OUTB	Channel B output, capable of sourcing and sinking 5A
6	V_{CC}	Supply Voltage.
7	OUTA	Channel A output, capable of sourcing and sinking 5A
8	ENB	Enable input for Channel B. A logic high (or floating) enables Channel B (the state of OUTB is determined by INB). A logic low disables OUTB (OUTB held low regardless of INB).
The thermal pad on the bottom of the thermally enhanced IX4340NE may be connected to GND or left floating; it must not be connected to any other net. The thermal pad is not intended to carry current.		

1.4 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	20	V
Input Voltage	V_{IN}	-0.3	20	V
Output Current	I_{OUT}	-	±5	A
ESD Rating (Human Body Model)	V_{ESD}	-4000	+4000	V
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

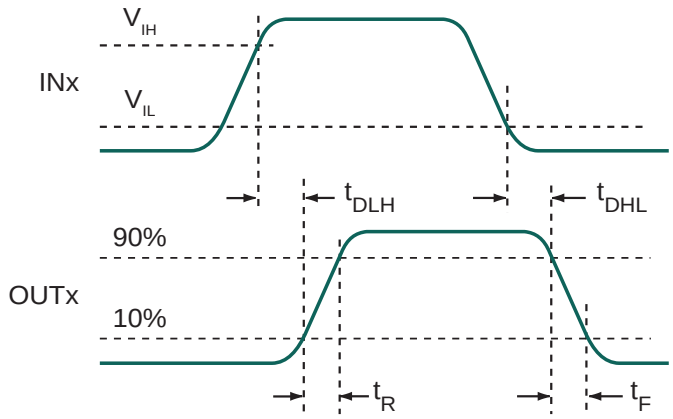
Absolute maximum electrical ratings are at T_A=25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.5 Electrical Characteristics

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Supply						
Supply Current	OUTA and OUTB Open	I_{CC}	-	1.4	2.5	mA
Under Voltage Lockout (UVLO)						
UVLO Rising Threshold	V_{CC} Rising	$UVLO_{ON}$	3.5	3.85	4.2	V
UVLO Falling Threshold	V_{CC} Falling	$UVLO_{OFF}$	3.1	3.3	3.5	
UVLO Threshold Hysteresis	-	$UVLO_{HYS}$	0.2	0.5	0.8	
Logic Inputs (INA, INB, ENA, ENB)						
Input Low Voltage	-	V_{IL}	-	-	0.8	V
Input High Voltage	-	V_{IH}	2.5	-	-	
Output Drivers (OUTA, OUTB)						
Output Pull-Up Resistance	I_{OUT} = -100mA, T_J = 25°C	R_{OH}	-	1	1.5	Ω
	I_{OUT} = -100mA		-	1.3	1.8	
Output Pull-Down Resistance	I_{OUT} = 100mA, T_J = 25°C	R_{OL}	-	0.6	1.1	
	I_{OUT} = 100mA		-	0.8	1.4	
Rise Time	C_{LOAD} = 1.8nF	t_R	-	7	15	ns
Fall Time	C_{LOAD} = 1.8nF	t_F	-	7	15	
Propagation Delay, Low to High	C_{LOAD} = 1.8nF	t_{DLH}	5	16	30	
Propagation Delay, High to Low	C_{LOAD} = 1.8nF	t_{DHL}	5	16	30	
Propagation Delay Matching	-	t_M	-5	-	5	



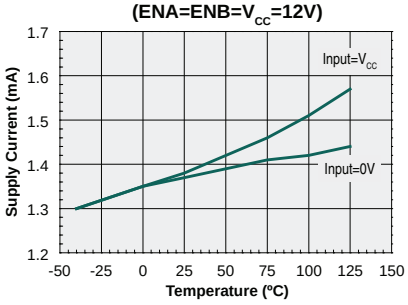
1.6 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Impedance, Junction-to-Ambient	θ_{JA}	85	°C/W
Thermal Impedance, Junction-to-Case	θ_{JC}	10	

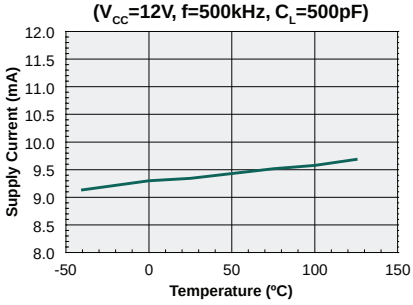
2 Performance Data

Unless otherwise noted, data presented in these graphs is typical of device operation at T_A=25ºC.

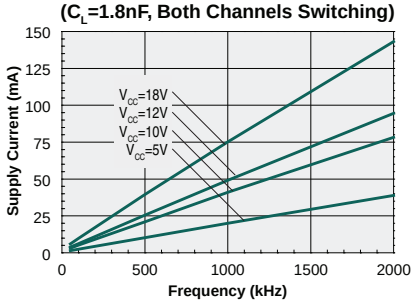
Supply Current vs. Temperature Outputs in DC ON/OFF Condition (ENA=ENB=V_{CC}=12V)



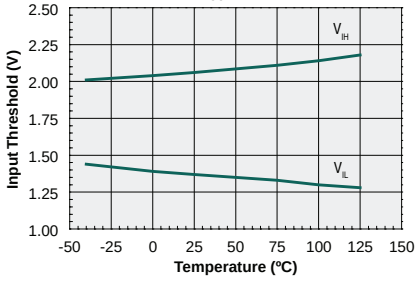
Operating Supply Current vs. Temperature (Outputs Switching) (V_{CC}=12V, f=500kHz, C_L=500pF)



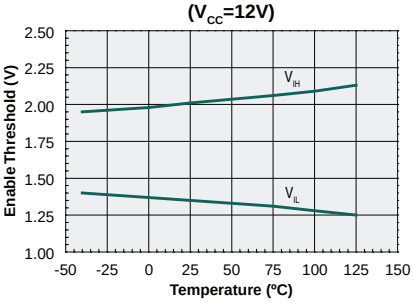
Operating Supply Current vs. Frequency (C_L=1.8nF, Both Channels Switching)



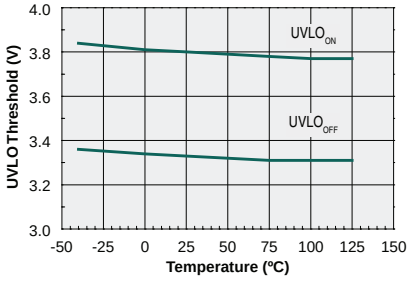
Input Threshold vs. Temperature (V_{CC}= 12V)



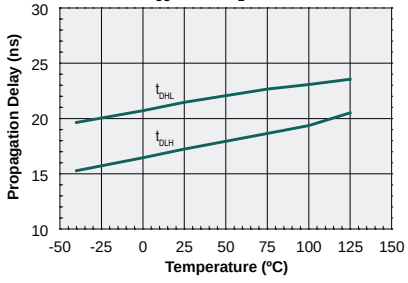
Enable Threshold vs. Temperature (V_{CC}=12V)



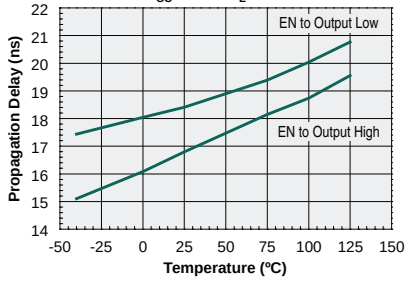
UVLO Threshold vs. Temperature



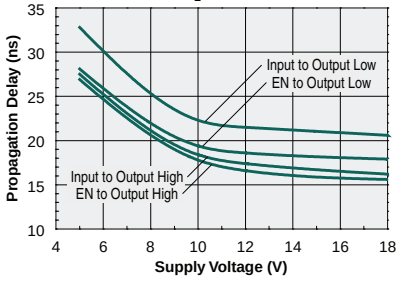
Input To Output Propagation Delay vs. Temperature (V_{CC}=12V, C_L=1.8 nF)



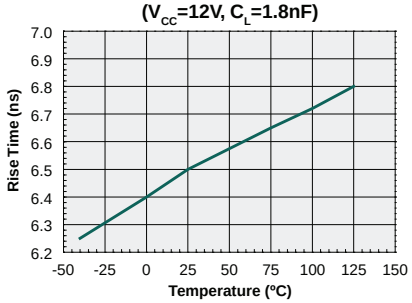
Enable to Output Propagation Delay vs. Temperature (V_{CC}=12V, C_L=1.8nF)



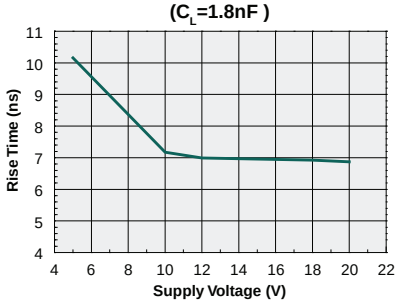
Propagation Delay vs. Supply Voltage (C_L=1.8nF)



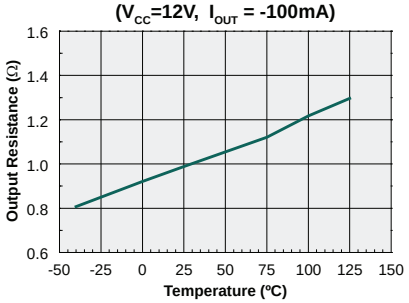
Rise Time vs. Temperature (V_{CC}=12V, C_L=1.8nF)



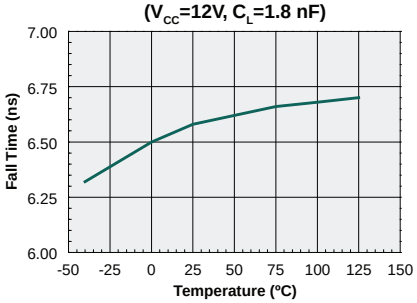
Rise Time vs. Supply Voltage (C_L=1.8nF)



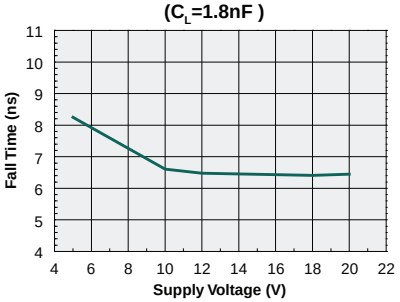
Output Pull-Up Resistance vs. Temperature (V_{CC}=12V, I_{OUT} = -100mA)



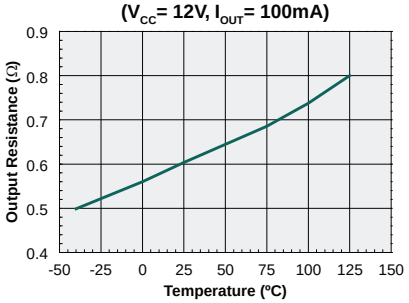
Fall Time vs. Temperature (V_{CC}=12V, C_L=1.8 nF)



Fall Time vs. Supply Voltage (C_L=1.8nF)



Output Pull-Down Resistance vs. Temperature (V_{CC}= 12V, I_{OUT}= 100mA)



3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4340NE	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

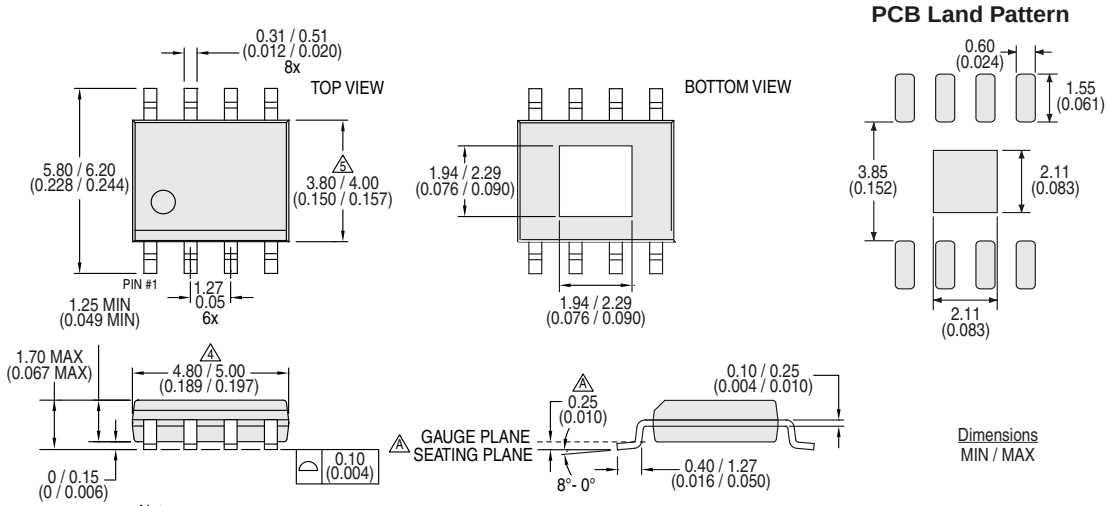
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX4340NE	260°C	30 seconds	3

3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

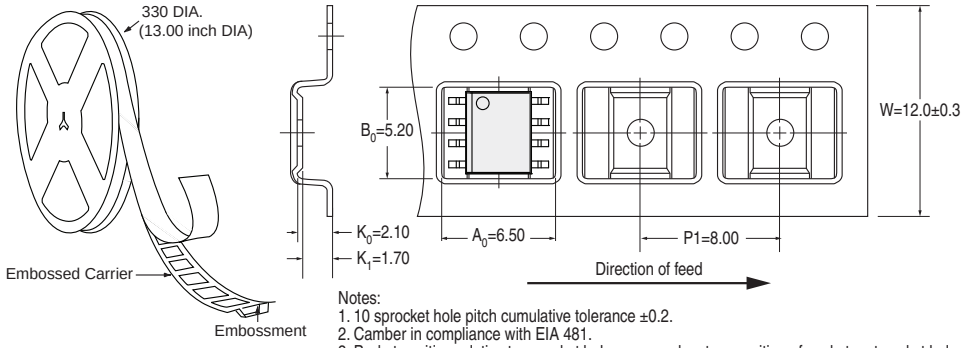
3.5 Mechanical Dimensions

3.5.1 IX4340NE Package Dimensions



Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The thermal pad on the bottom of the device may be connected to GND or left floating; it must not be connected to any other signal. The thermal pad is not intended to carry current.
7. Lead thickness includes plating.

3.5.2 IX4340NETR Tape & Reel Dimensions



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. All dimensions in millimeters.

For additional information please visit our website at: www.ixysic.com

Specification: DS-IX4340NE-R01

12/18/2018

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

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