

MAX40006

Micropower, Rail-to-Rail, 300kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

General Description

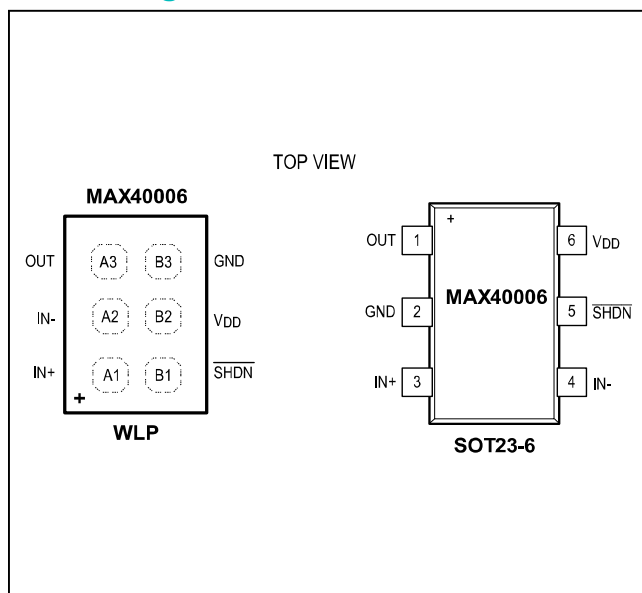
The MAX40006 op amp features a maximized ratio of gain bandwidth (GBW) to supply current and is ideal for battery-powered applications such as handsets, tablets, notebooks, and portable medical equipment. This CMOS op amp features an ultra-low input-bias current of 1pA, rail-to-rail input and output, low supply current of 4.5 μ A, and operates from a single 1.7V to 5.5V supply. For additional power conservation, the IC also features a low-power shutdown mode that reduces supply current to 0.1 μ A and puts the amplifier's outputs in a high-impedance state. This device is unity-gain stable with a 300kHz GBW product.

The MAX40006 is available in a space-saving, 0.73mm x 1.07mm, 6-bump wafer-level package (WLP), as well as a 6-pin SOT-23 package. The device is specified over the -40°C to +125°C automotive operating temperature range.

Applications

- Portable Media Players
- Tablet/Notebook Computers
- Electronic Toys
- Portable Medical Devices
- Wearable Fitness Devices

Pin Configurations

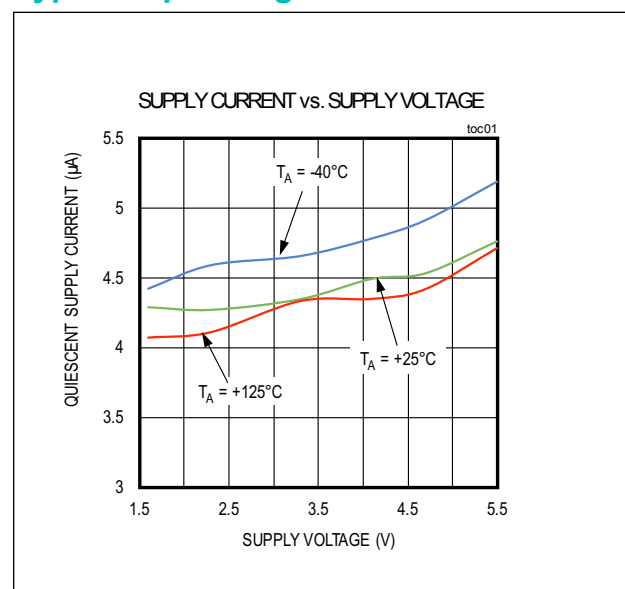


Benefits and Features

- 300kHz GBW
- Ultra-Low 4.5 μ A Supply Current
- Single 1.7V to 5.5V Supply Voltage Range
- Ultra-Low 1pA Input Bias Current
- Rail-to-Rail Input and Output Voltage Ranges
- Low \pm 200 μ V Input Offset Voltage
- Low 0.1 μ A Shutdown Current
- High-Impedance Output During Shutdown
- Unity-Gain Stable
- Available in Tiny, 0.73mm x 1.07mm, 6-Bump WLP and SOT-23 Packages
- -40°C to +125°C Temperature Range

Ordering Information appears at end of data sheet.

Typical Operating Characteristic



Absolute Maximum Ratings

V_{DD} to GND-0.3V to +6V
 IN+, IN-, SHDN, OUT to GND.....-0.3V to (V_{DD} + 0.3V)
 Differential Input Voltage (IN+, IN-) ±(V_{DD} + 0.3V)
 Output Short Circuit Duration to either Supply..... Continuous
 Continuous Current into any input/output..... ±10mA
 Continuous Power Dissipation (T_A = +70°C)
 6-Bump WLP (Derate 10.19mW/°C above +70°C)815mW
 6-Pin SOT (Derate 4.3mW/°C above +70°C)347.8mW

Operating Temperature Range..... -40°C to +125°C
 Junction Temperature..... +150°C
 Storage Temperature Range..... -65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
 Junction-to-Ambient Thermal Resistance (θ_{JA})98.06°C/W

SOT23
 Junction-to-Ambient Thermal Resistance (θ_{JA})230°C/W
 Junction-to-Ambient Thermal Resistance (θ_{JC})76°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

V_{DD} = 3.6V, V_{GND} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_L = ∞, V_{SHDN} = V_{DD}, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE						
Supply Voltage Range	V _{DD}		1.7		5.5	V
Supply Current	I _{DD}	V _{DD} = 3.6V, T _A = +25°C		4.5	5	µA
		V _{DD} = 3.6V, T _A = -40°C to +125°C			6.5	
Shutdown Supply Current	I _{SHDN}	V _{DD} = 3.6V, T _A = -40°C to +125°C		100	550	nA
		V _{DD} = 5.5V, T _A = -40°C to +125°C			900	
Power Up Time		V _{DD} = 0 to 5.5V step, output settles to 5% final value		35		µs
Input Common-Mode Range	V _{CM}	Guaranteed by CMRR test	-0.05		V _{DD} + 0.05	V
Input Offset Voltage	V _{OS}	T _A = +25°C		±0.2	±1	mV
Input Offset Drift		T _A = -40°C to +125°C		10		µV/°C
Input Bias Current	I _B	T _A = +25°C		1	20	pA
		T _A = -40°C to +125°C			3	nA
Input Offset Current	I _{OS}	T _A = +25°C		1	20	pA
		T _A = -40°C to +125°C			3	nA
Input Capacitance	C _{IN}	Either input		3		pF

Electrical Characteristics (continued)

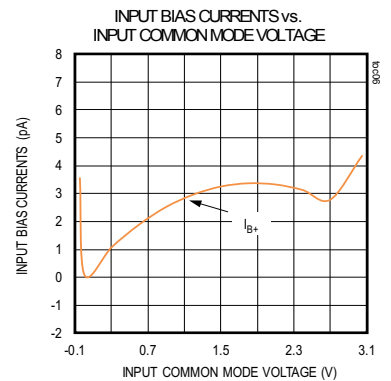
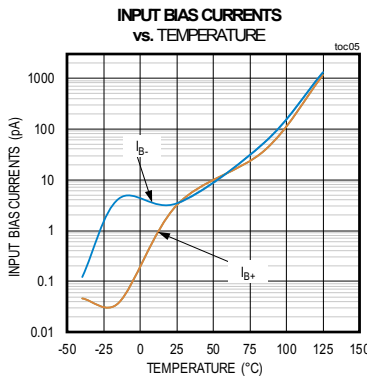
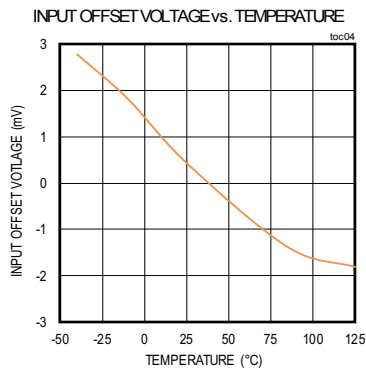
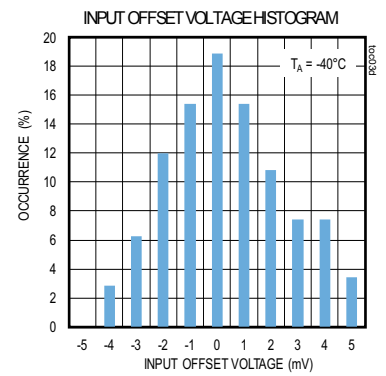
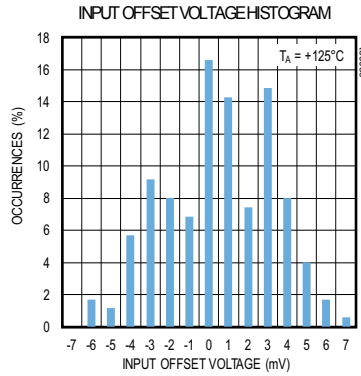
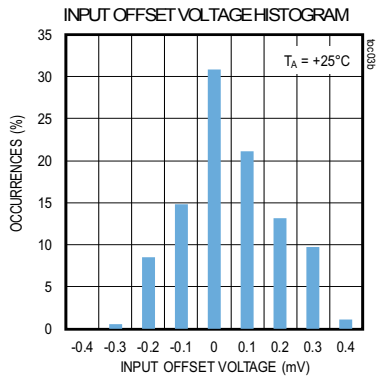
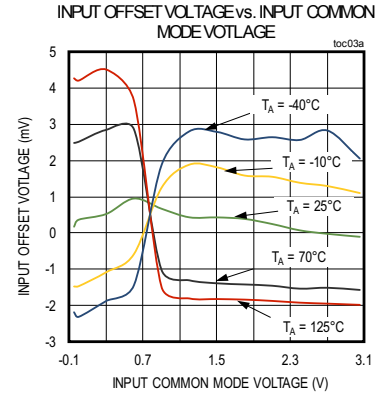
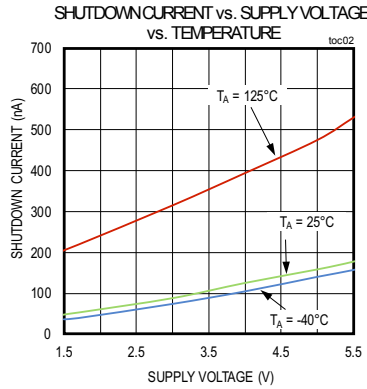
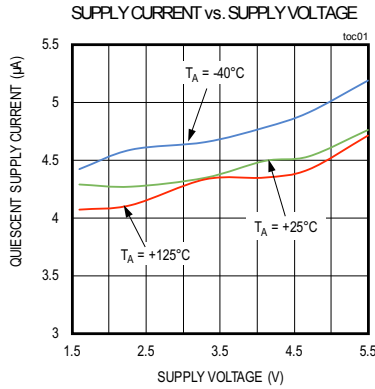
$V_{DD} = 3.6V$, $V_{GND} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$, $V_{SHDN} = V_{DD}$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ C$, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	DC, $V_{DD} = 3.6V$, $-0.05V < V_{CM} < V_{DD} + 0.05V$ $T_A = -40^\circ C$ to $+125^\circ C$	50			dB
		DC, $V_{DD} = 1.7V$, $-0.05V < V_{CM} < V_{DD} + 0.05V$ $T_A = -40^\circ C$ to $+125^\circ C$	42			dB
		AC, 100mV _{PP} at 1kHz		55		dB
Power Supply Rejection Ratio	PSRR	DC, $1.7V < V_{DD} < 5.5V$	60			dB
		AC, 100mV _{PP} at 1kHz		65		
Open Loop Gain	A _{VOL}	$V_{DD} = 3.6V$, $R_L = 100k\Omega$ $25mV < V_{OUT} < V_{DD} - 25mV$	80	100		dB
		$V_{DD} = 1.7V$, $R_L = 100k\Omega$ $25mV < V_{OUT} < V_{DD} - 25mV$	69			
Output Voltage Swing High	V _{OH}	$R_L = 100k\Omega$, measured relative to V_{DD}			5	mV
		$R_L = 5k\Omega$, measured relative to V_{DD}			70	
Output Voltage Swing Low	V _{OL}	$R_L = 100k\Omega$, measured relative to GND			5	mV
		$R_L = 5k\Omega$, measured relative to GND			70	
Short Circuit Current		To V_{DD} or GND		15		mA
Shutdown High Level Input	V _{IH}		0.7 x			V
Shutdown Low Level Input	V _{IL}				0.3 x	V
Shutdown Input Bias Current					0.5	μA
Output Leakage in Shutdown Mode		$0V < V_{OUT} < V_{DD}$			0.5	μA
-3dB Bandwidth		Amplifier connected as unity gain buffer		300		kHz
Phase Margin		Amplifier connected as unity gain buffer		50		°
Slew Rate		$A_V = 1V/V$, $V_{DD}/2 - 0.5V$ to $V_{DD}/2 + 0.5V$ step, $R_L = 100k\Omega$ to $V_{DD}/2$, $C_L = 13pF$		0.14		V/μs
Settling Time		0.1% settling, $A_V = 1V/V$, $V_{DD}/2 - 0.5V$ to $V_{DD}/2 + 0.5V$ step, $R_L = 100k\Omega$ to $V_{DD}/2$, $C_L = 13pF$		12		us
Capacitive Load	C _L	$A_V = 1V/V$, no sustain oscillations		30		pF
Input Voltage Noise Density	e _N	At 10kHz		440		nV/√Hz
Input Current Noise Density	i _N	At 10kHz		0.001		pA/√Hz
Shutdown Delay Time	t _{SHDN}	$V_{DD} = 5.5V$, $V_{SHDN} = 5.5V$ to $0V$ step		2		μs
Enable Delay Time	t _{EN}	$V_{DD} = 5.5V$, $V_{SHDN} = 0V$ to $5.5V$ step		35		μs

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

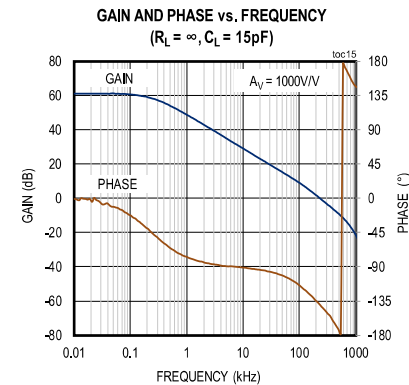
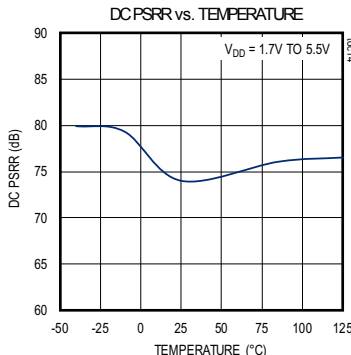
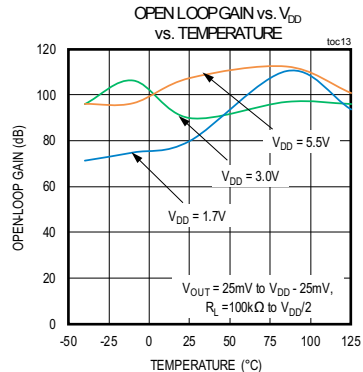
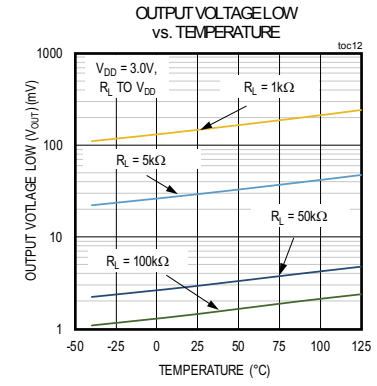
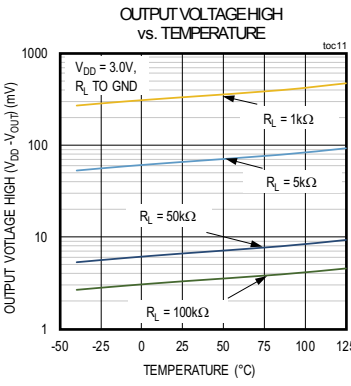
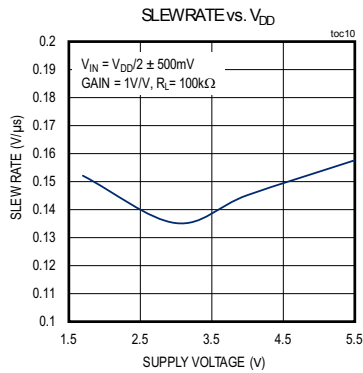
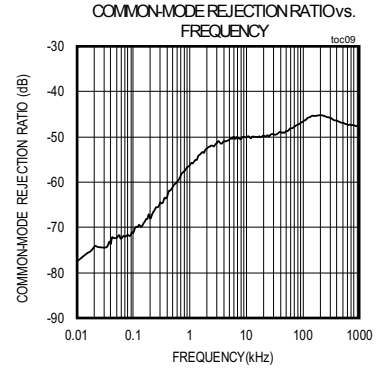
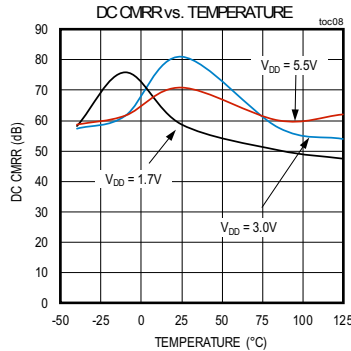
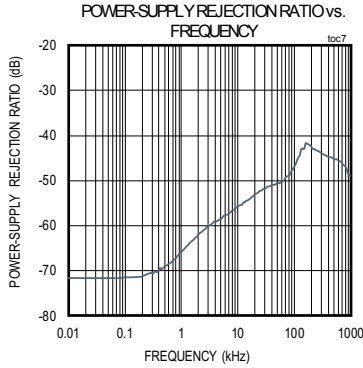
Typical Operating Characteristics

($V_{DD} = 3V$, $V_{GND} = 0V$, $V_{CM} = V_{DD}/2$, $R_L = 100k\Omega$ to $V_{DD}/2$, $T_A = 25^\circ C$, unless otherwise noted.)



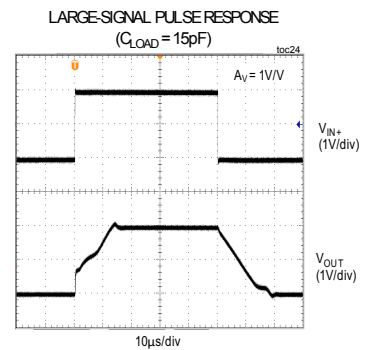
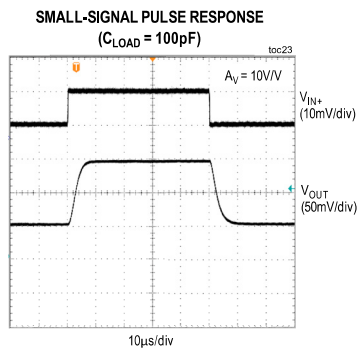
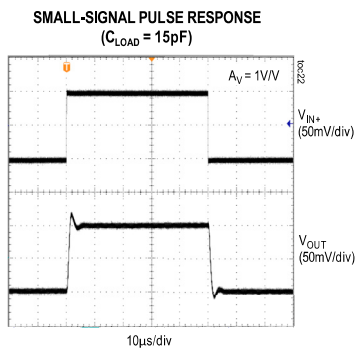
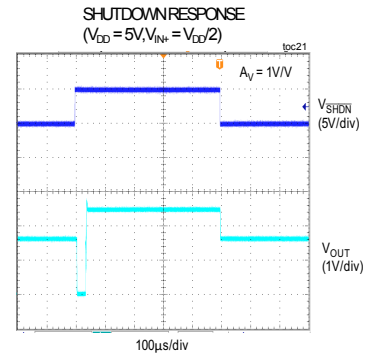
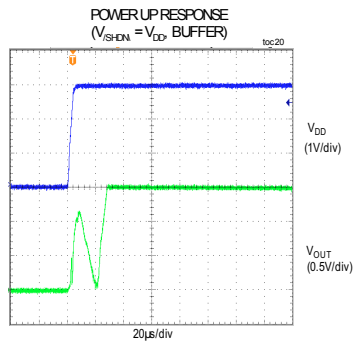
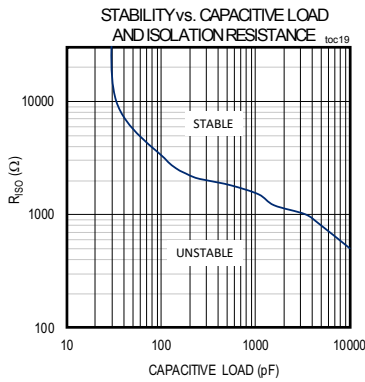
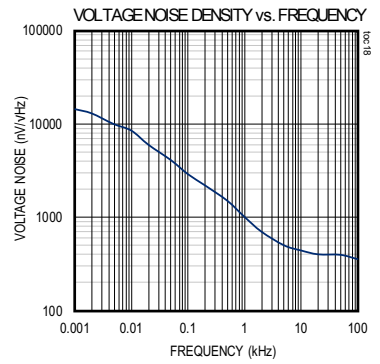
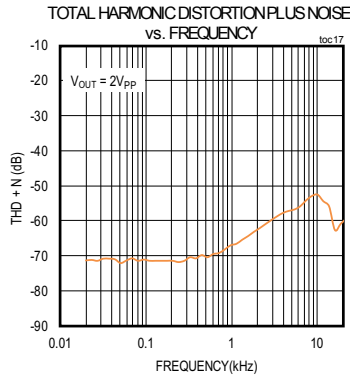
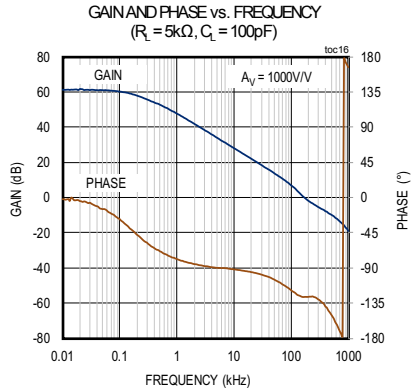
Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $V_{GND} = 0V$, $V_{CM} = V_{DD}/2$, $R_L = 100k\Omega$ to $V_{DD}/2$, $T_A = 25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

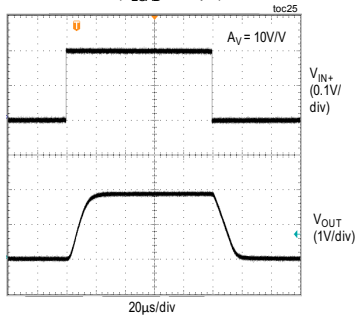
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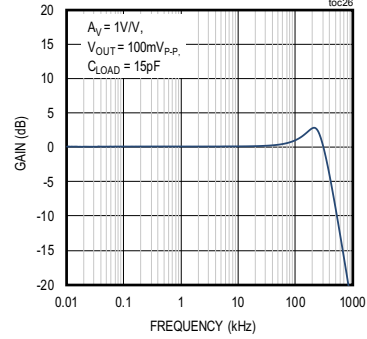
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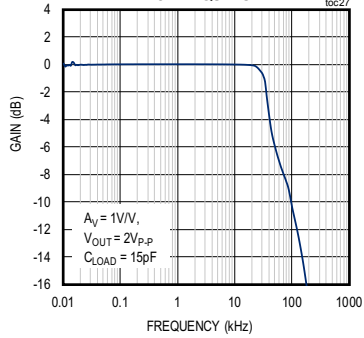
LARGE-SIGNAL PULSE RESPONSE
($C_{LOAD} = 100pF$)



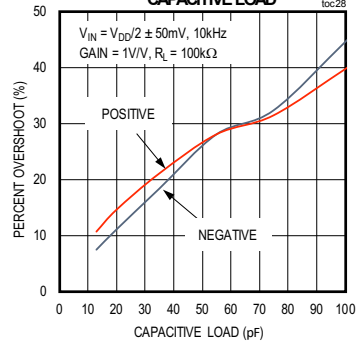
SMALL-SIGNAL GAIN vs. FREQUENCY



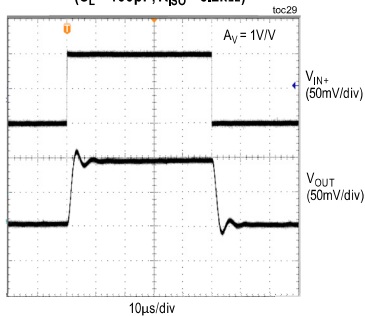
LARGE-SIGNAL GAIN vs. FREQUENCY



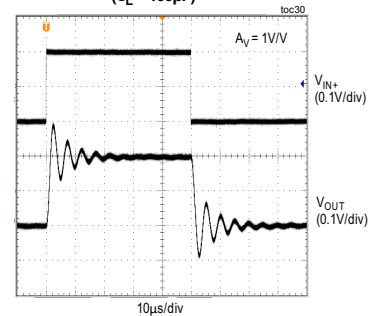
PERCENT OVERSHOOT vs. CAPACITIVE LOAD



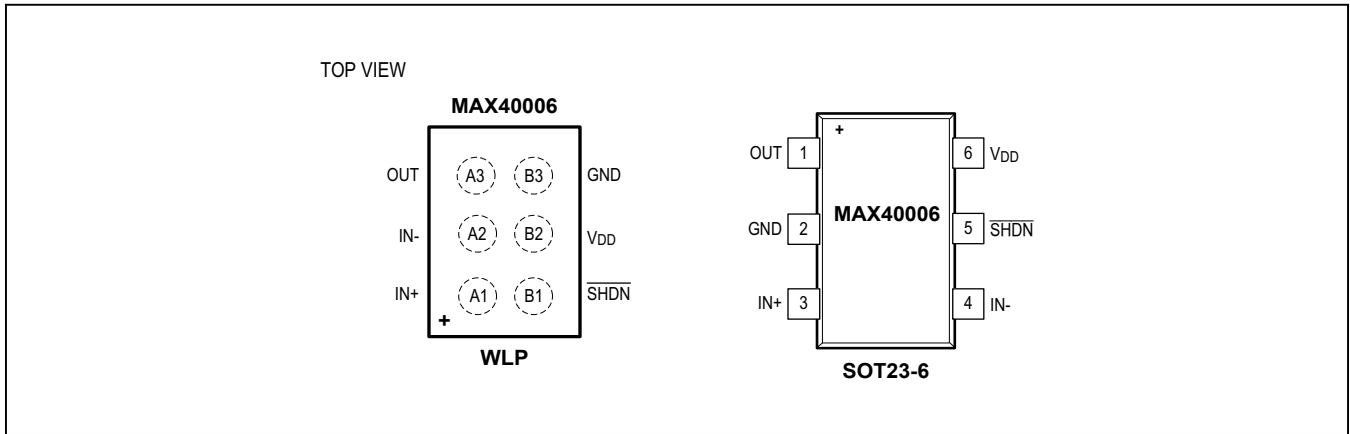
OUTPUT WAVEFORM WITH R_{SO}
($C_L = 100pF$, $R_{SO} = 6.2k\Omega$)



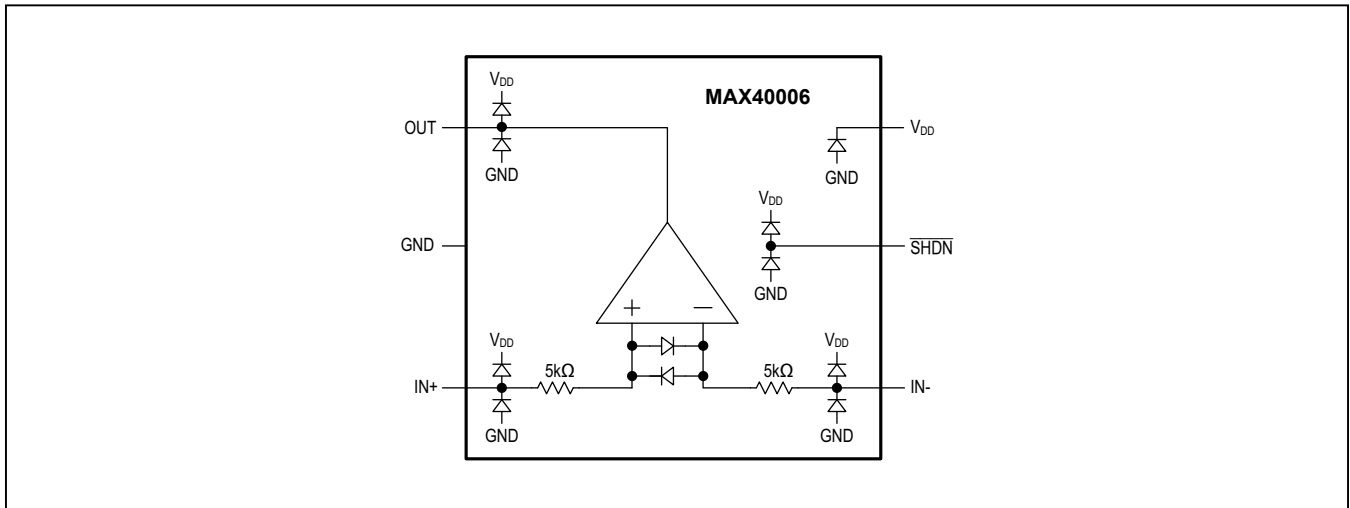
OUTPUT WAVEFORM WITHOUT R_{SO}
($C_L = 100pF$)



Pin Configurations



Functional Block Diagram



Pin Description

PIN		NAME	FUNCTION
WLP	SOT23		
A1	3	IN+	Noninverting Input
A2	4	IN-	Inverting Input
A3	1	OUT	Output
B1	5	SHDN	Active Low Shutdown Input
B2	6	VDD	Positive Supply Voltage
B3	2	GND	Ground

Detailed Description

Featuring a maximized ratio of GBW-to-supply current, low operating supply voltage, low input bias current, and rail-to-rail inputs and outputs, the MAX40006 is an excellent choice for precision or general-purpose, low-current, low-voltage, battery-powered applications. This CMOS device consumes an ultra-low 4.5 μ A (typ) supply current and has a 200 μ V (typ) offset voltage. For additional power conservation, the IC features a low-power shutdown mode that reduces supply current to 0.1 μ A (typ) and puts the amplifier's output in a high-impedance state. This device is unity-gain stable with a 300kHz GBW product, driving capacitive loads up to 30pF. The capacitive load can be increased to 250pF when the amplifier is configured for a 10V/V gain.

Input Differential Voltage Protection

During normal operation, the inverting and noninverting inputs of the device are at essentially the same voltage. However, either due to fast input voltage transients or other fault conditions, these inputs can be forced to be at two different voltages. Internal back-to-back diodes protect the inputs from an excessive differential voltage (see [Functional Block Diagram](#)). Therefore, V_{IN+} and V_{IN-} can be any voltage within the range shown in the [Absolute Maximum Ratings](#) section. Note the protection time is still dependent on the package thermal limits. If the input signal is fast enough to create the internal diodes' forward bias condition, the input signal current must be limited to 5mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. Care should be taken in choosing the input series resistor value, since it degrades the input noise performance of the amplifier.

Rail-to-Rail Inputs and Outputs

The MAX40006 has a parallel-connected n-channel and p-channel differential input stage that allows an input common-mode voltage range that extends 50mV beyond the positive and negative supply rails. This device is capable of driving the output to within 5mV of both supply rails with a 100k Ω load. This device can drive a 5k Ω load with swings to within 70mV of the rails. [Figure 1](#) shows the output voltage swing of the amplifier, configured as a unity-gain buffer, and powered from a single 3V supply.

Low Input Bias Current

The MAX40006 features ultra-low 1pA (typ) input bias current. The variation in the input bias current is minimal with changes in the input voltage due to very high input impedance (in the order of 1G Ω).

Applications Information

Driving Capacitive Loads

The amplifier is unity-gain stable for loads up to 30pF. However, the capacitive load can be increased to 250pF when the amplifier is configured for a minimum gain of 10V/V. Applications that require greater capacitive-drive capability should use an isolation resistor between the output and the capacitive load ([Figure 2](#)). Also, in unity-gain applications with relatively small R_L (approximately 5k Ω), the capacitive load can be increased up to 200pF.

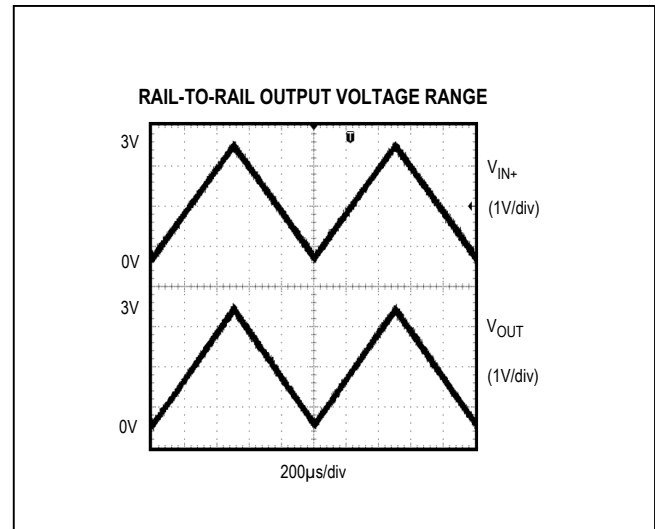


Figure 1. Rail-to-Rail Output Voltage Range

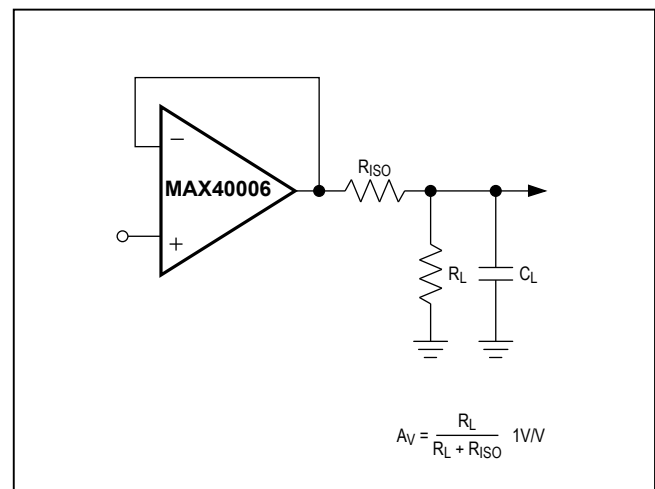


Figure 2. Using a Resistor to Isolate a Capacitive Load from the Op Amp

Power-Supply Considerations

The MAX40006 is optimized for single 1.7V to 5.5V supply operation. A high amplifier power-supply rejection ratio of 80dB (typ) allows the devices to be powered directly from a battery, simplifying design and extending battery life.

Power-Up Settling Time

The MAX40006 settling time depends primarily on the output voltage and is slew rate limited. Figure 3 shows the MAX40006 in a noninverting voltage follower configuration with the input held at midsupply. The output settles in approximately 35μs for V_{DD} = 3V (see the *Typical Operating Characteristics* for power-up settling time).

Power-Supply Bypassing and Layout

To minimize noise, bypass V_{DD} with a 0.1μF capacitor to ground, as close to the pin as possible.

Good layout techniques optimize performance by decreasing the amount of stray capacitance and inductance to the op amps' inputs and outputs. Minimize stray capacitance and inductance by placing external components close to the IC.

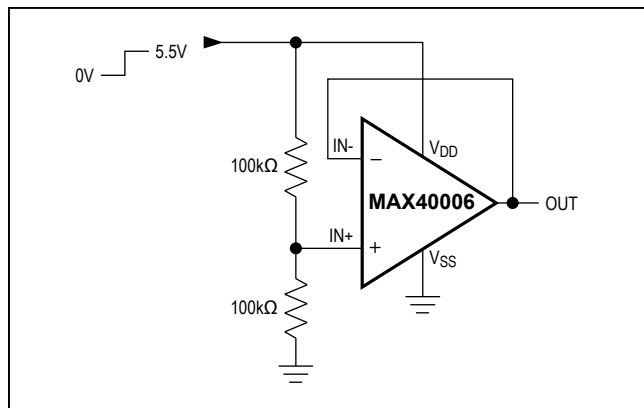


Figure 3. Power-Up Test Configuration

Shutdown

The shutdown input ($\overline{\text{SHDN}}$) is an active-low input. For normal operating conditions, connect $\overline{\text{SHDN}}$ to a logic-high or V_{DD}. Drive $\overline{\text{SHDN}}$ low to place the device in shut down and reduce the supply current to 0.1μA. The MAX40006's output is high impedance in shutdown mode; however, due to the back-to-back diode protection circuit at the inputs and the feedback path, the output sees a voltage of one diode drop below the noninverting input voltage in unity buffer configuration (see Figure 4). The device typically enters shutdown in 2μs and exits in 35μs. Figure 5 and Figure 6 show the output voltage behavior during into and out of the shutdown mode in unity buffer configuration with V_{DD} = 5V, V_{IN+} = 2.5V and 0V, respectively. Figure 7 and Figure 8 show the output with 1MΩ in the feedback path, limiting the leakage current from the positive input due to the internal back-to-back diodes in shutdown mode.

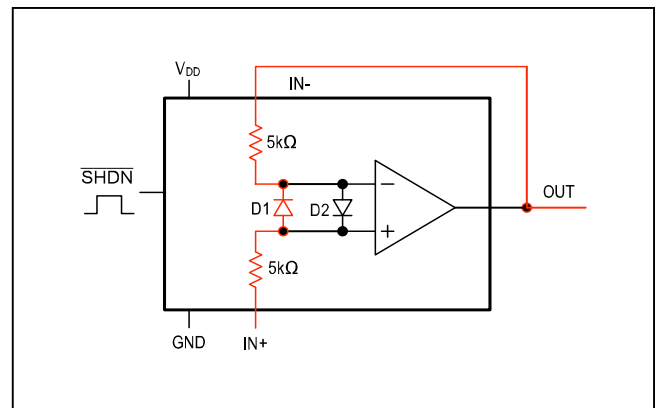
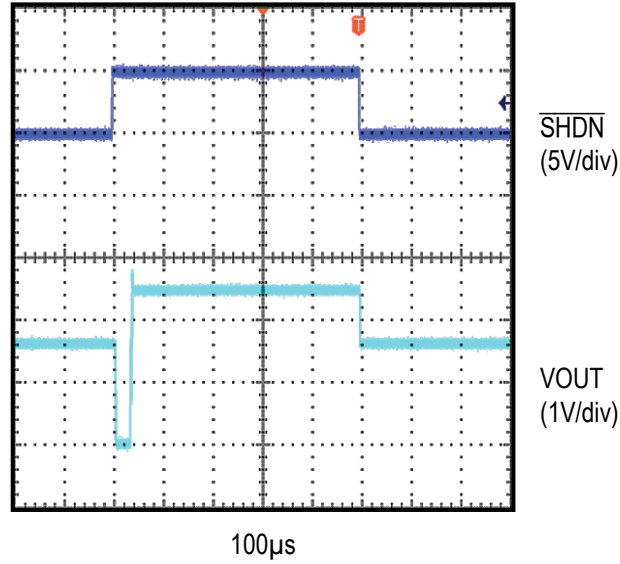
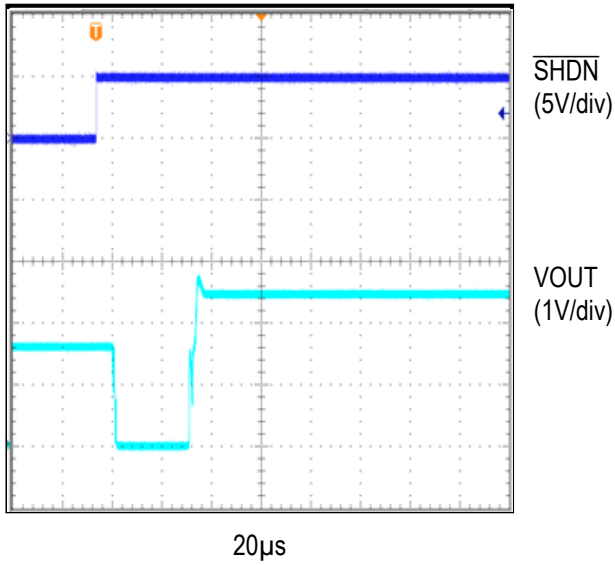


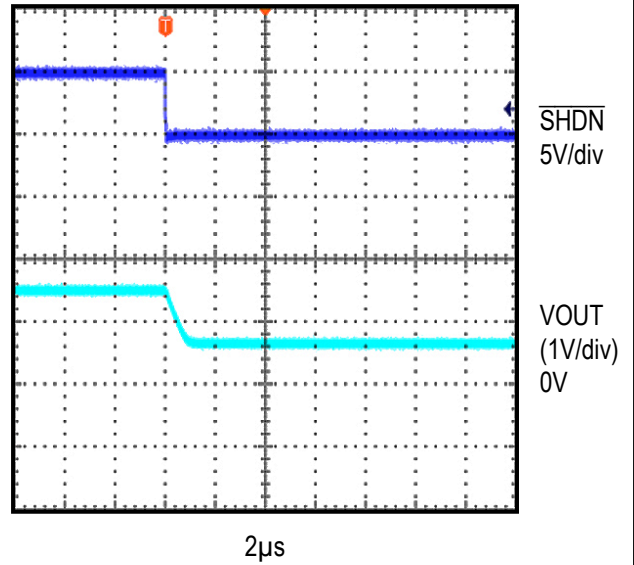
Figure 4. MAX40006 Leakage Path During Shutdown When Configured as A Buffer



a. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$

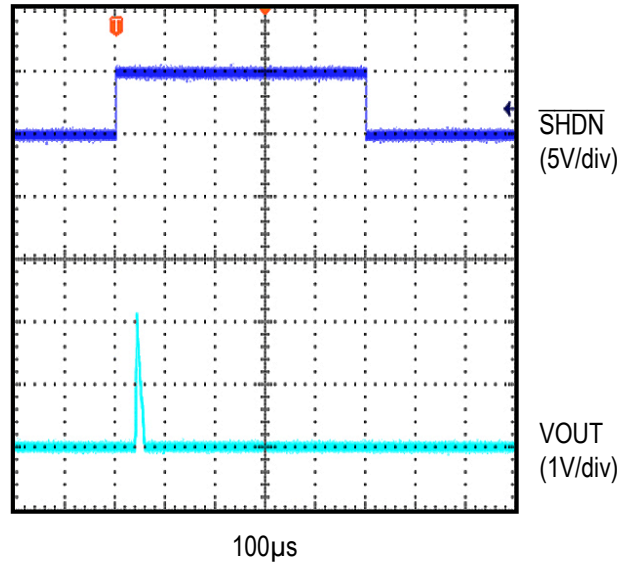


b. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$ (Zoomed In, Rising)

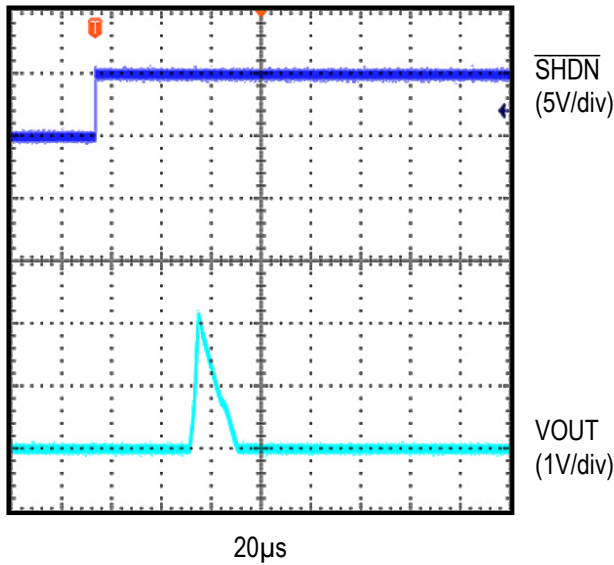


c. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$ (Zoomed In, Falling)

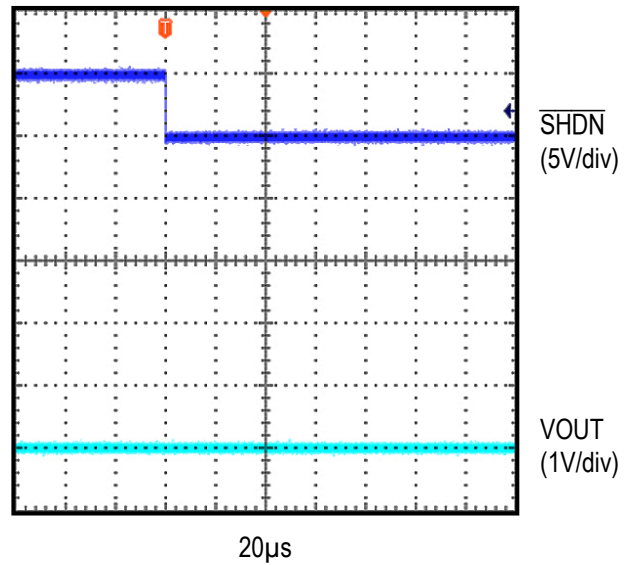
Figure 5. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$



a. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$

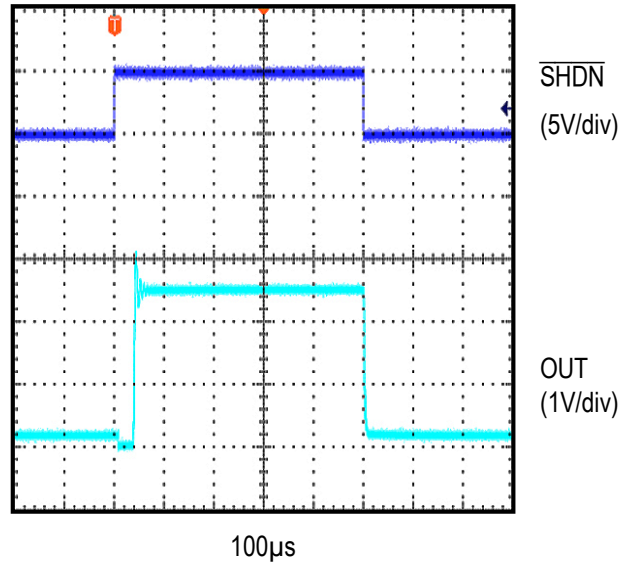


b. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$ (Zoomed In, Rising)

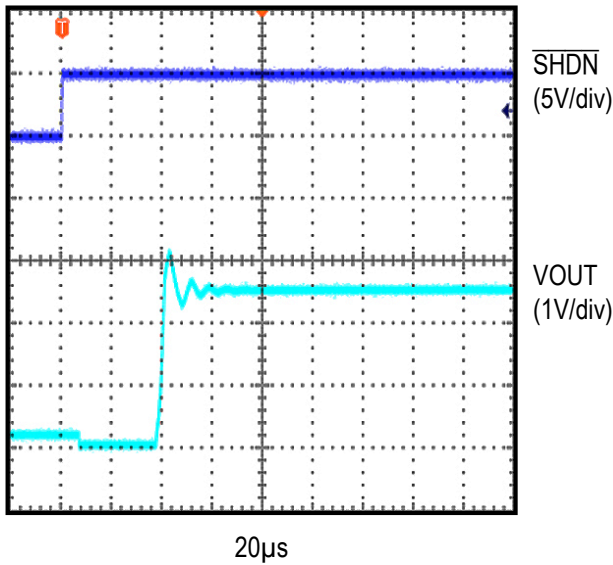


c. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$ (Zoomed In, Falling)

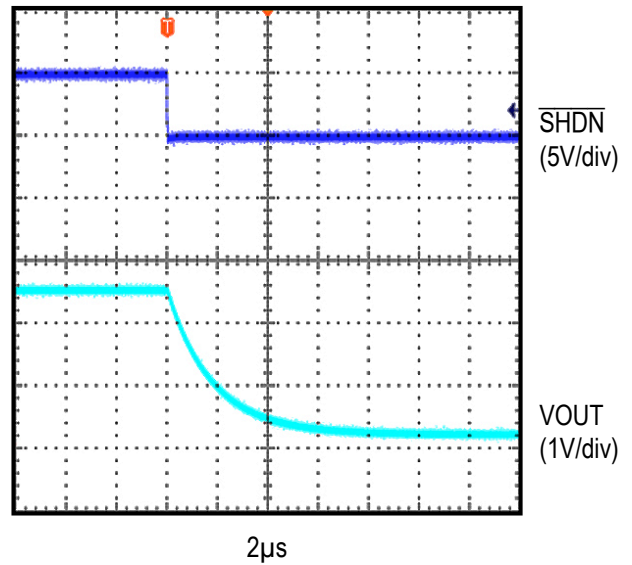
Figure 6. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$



a. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$, $R_{FB} = 1M\Omega$

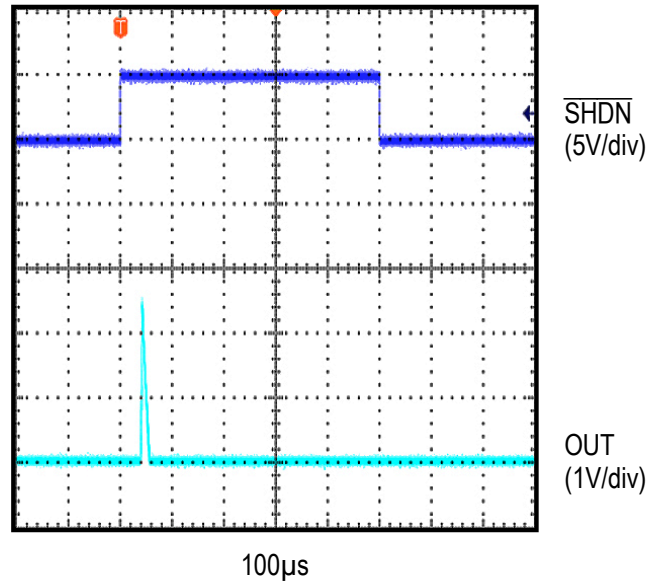


b. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$, $R_{FB} = 1M\Omega$ (Zoomed In, Rising)

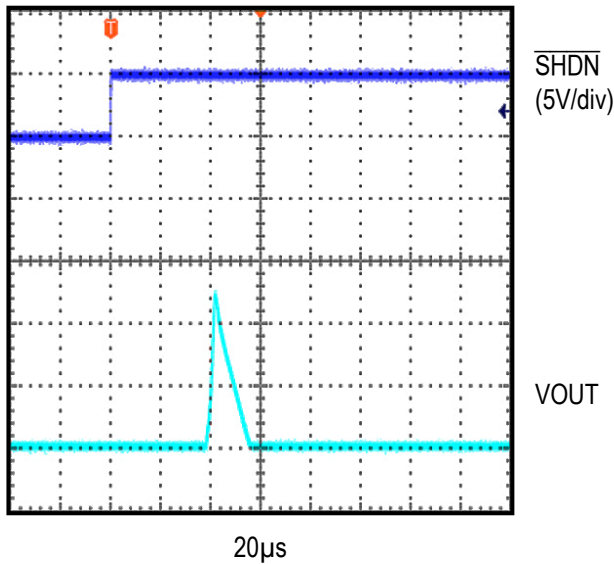


c. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$, $R_{FB} = 1M\Omega$ (Zoomed In, Falling)

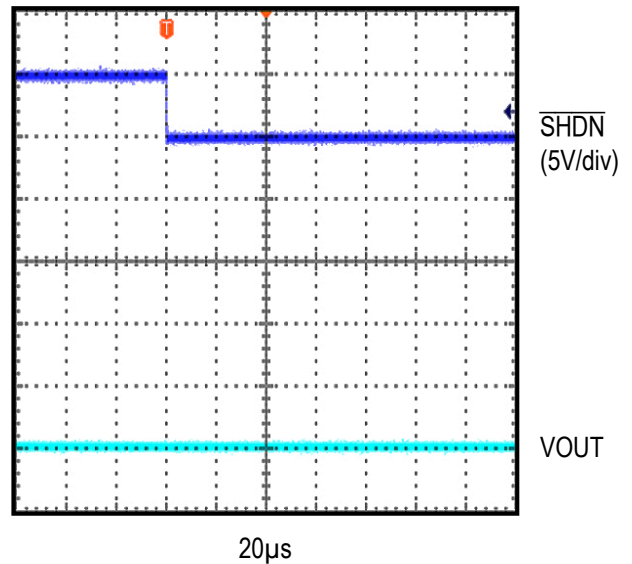
Figure 7. Buffer, $V_{DD} = 5V$, $V_{IN+} = 2.5V$, $R_{FB} = 1M\Omega$



a. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$, $R_{FB} = 1M\Omega$



b. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$, $R_{FB} = 1M\Omega$ (Zoomed In, Rising)



c. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$, $R_{FB} = 1M\Omega$ (Zoomed In, Falling)

Figure 8. Buffer, $V_{DD} = 5V$, $V_{IN+} = 0V$, $R_{FB} = 1M\Omega$

MAX40006

Micropower, Rail-to-Rail, 300kHz Op Amp
with Shutdown in a Tiny, 6-Bump WLP

Chip Information

PROCESS: BICMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX40006ANT+	-40°C to +125°C	6 WLP	+V
MAX40006AUT+	-40°C to +125°C	6 SOT	+ACUQ

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	N60D1+1	21-100086	Refer to Application Note AN1891
6 SOT23	U6-1	21-0058	90-0175

The drawing includes three views: TOP VIEW, FRONT VIEW, and BOTTOM VIEW. The TOP VIEW shows a rectangular package with a Pin 1 Indicator (marked '1') and a 'AAAA' marking. Dimensions E and D are indicated. The FRONT VIEW shows the package profile with dimensions A, A2, A3, and A1. A detail shows a bump with a diameter of 0.05 mm and a shape 'S'. The BOTTOM VIEW shows the bump array with dimensions E1, SE, e, A, B, and D1. Bump diameters are labeled as ϕb with a detail of 0.05 mm and shape 'AB'. A table of common dimensions is provided on the right.

COMMON DIMENSIONS	
A	0.50 MAX
A1	0.17 ±0.03
A2	0.30 REF
A3	0.040 BASIC
b	∅0.23 ±0.03
D	0.727 ±0.025
E	1.077 ±0.025
D1	0.35 BASIC
E1	0.70 BASIC
e	0.35 BASIC
SD	0.175 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:

1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE PACKAGE OUTLINE 6 BUMPS
THIN WLP PKG. 0.35 mm PITCH, N60D1+1

APPROVAL DOCUMENT CONTROL NO. 21-100086 REV. C 1/1

- DRAWING NOT TO SCALE -

MAX40006

Micropower, Rail-to-Rail, 300kHz Op Amp
with Shutdown in a Tiny, 6-Bump WLP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/16	Initial release	—
1	1/18	Updated <i>Ordering Information</i> table	15

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