STN3NF06L

N-channel 60 V, 0.07 Ω typ., 4 A STripFET™ II Power MOSFET in a SOT-223 package

Datasheet - production data

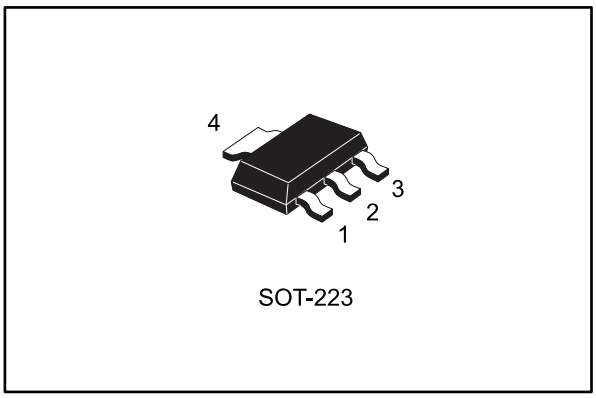
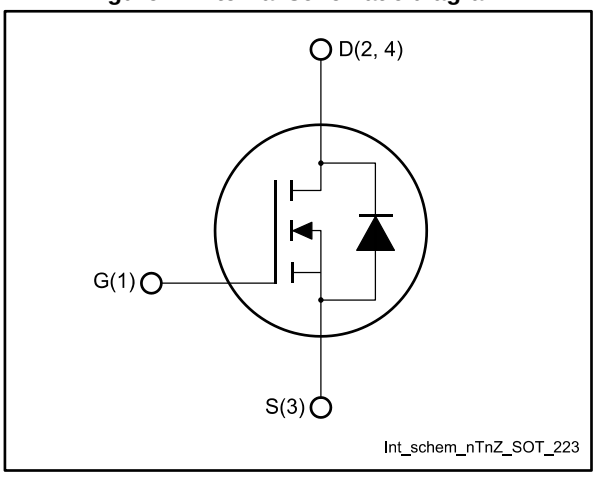


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN3NF06L	60 V	0.1 Ω	4 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STN3NF06L	3NF06L	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±16	V
I_D (1)	Drain current (continuous) at Tc = 25 °C	4	A
I_D	Drain current (continuous) at T_c = 100 °C	2.9	A
I_{DM} (2)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	3.3	W
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (4)	Single pulse avalanche energy	200	mJ
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Current limited by the package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 3 A, di/dt ≤ 150 A/µs, V_{DD} ≤ $V_{(BR)DSS}$

(4)Starting T_j = 25 °C, I_D = 4 A, V_{DD} = 30 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb (1)	38	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb(2)	100	°C/W

Notes:

(1)When Mounted on FR-4 board 1 inch^2 pad, 2 oz. of Cu and t <10 s.

(2)When mounted on minimum recommended footprint.

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 V T_C = 125 °C(1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.8	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 1.5 A		0.07	0.10	Ω
		V_{GS}= 5 V, I_D= 1.5 A		0.085	0.12	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0 V	-	340		pF
C_{oss}	Output capacitance		-	63		pF
C_{rss}	Reverse transfer capacitance		-	30		pF
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 3 A V_{GS}= 0 to 5 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	7	9	nC
Q_{gs}	Gate-source charge		-	1.5		nC
Q_{gd}	Gate-drain charge		-	2.8		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 30 V, I_D = 1.5 A, R_G = 4.7 Ω V_{GS} = 5 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	9	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	20	-	ns
t_f	Fall time		-	10	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD}= 4 A, V_{GS}=0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 4 A, di/dt = 100 A/µs, V_{DD}=25 V, T_j=150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	50		ns
Q_{rr}	Reverse recovery charge		-	88		nC
I_{RRM}	Reverse recovery current		-	3.5		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

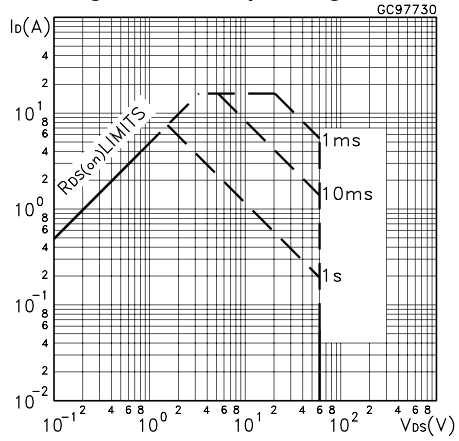


Figure 3: Thermal impedance

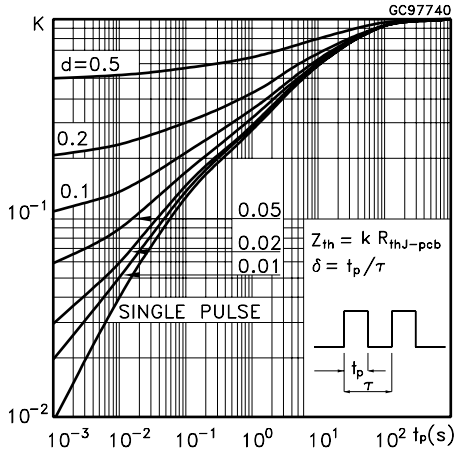


Figure 4: Output characteristics

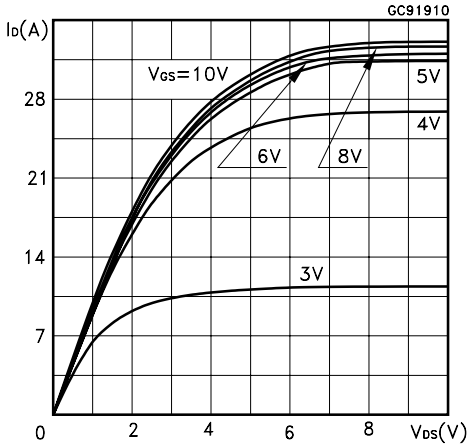


Figure 5: Transfer characteristics

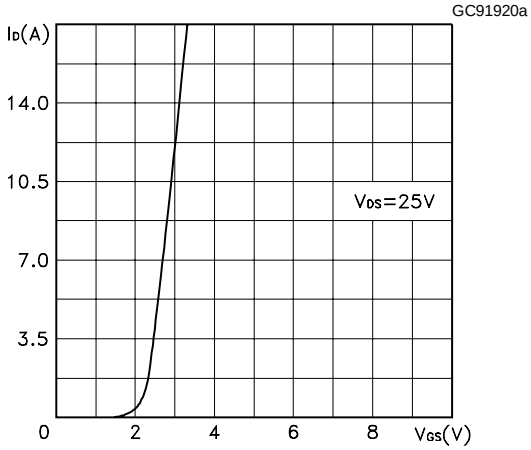


Figure 6: Static drain-source on-resistance

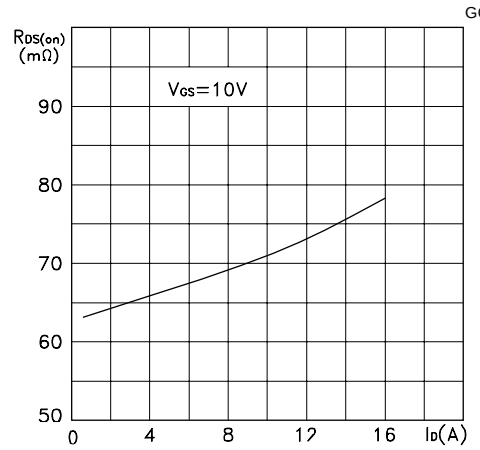


Figure 7: Gate charge vs. gate-source voltage

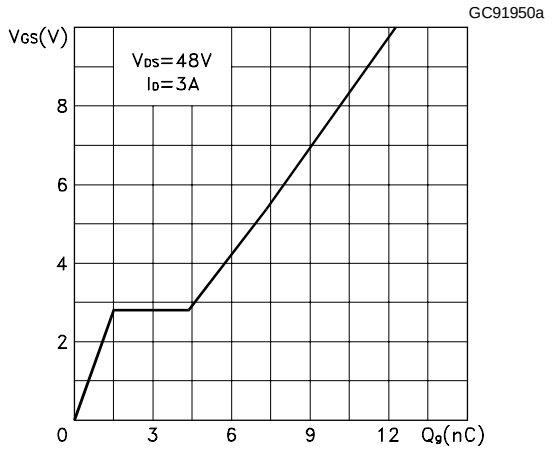


Figure 8: Capacitance variations

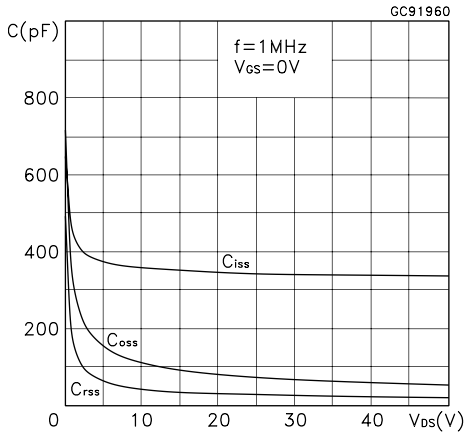


Figure 9: Normalized gate threshold voltage vs temperature

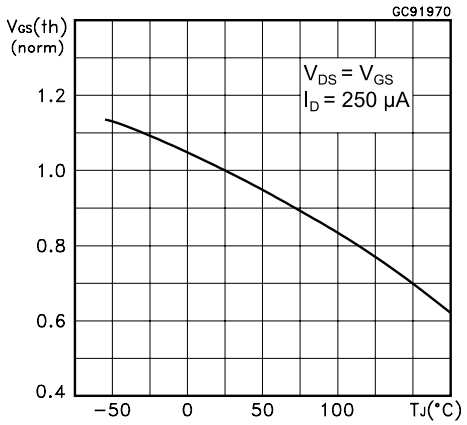


Figure 10: Normalized on-resistance vs temperature

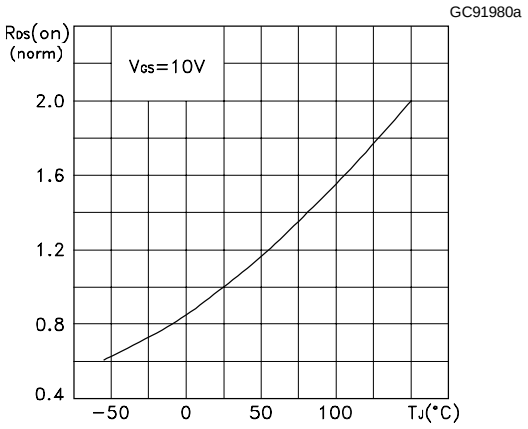


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

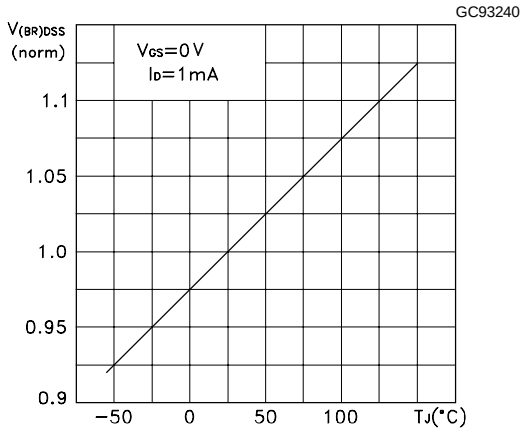
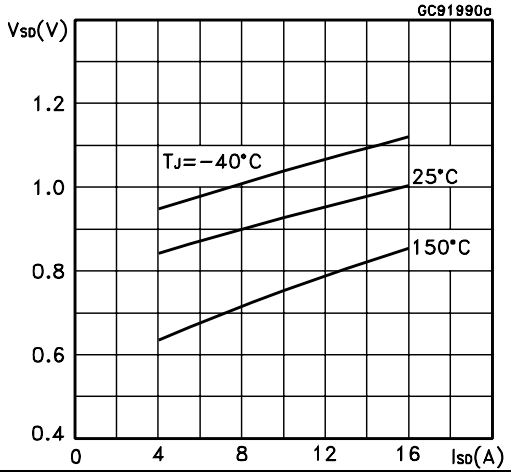


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

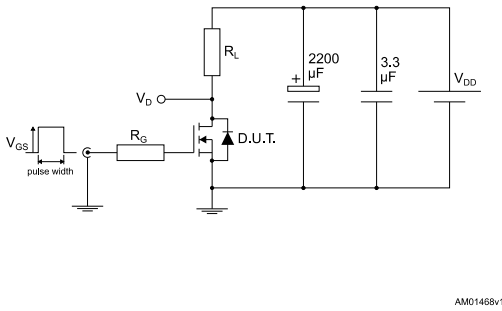


Figure 14: Test circuit for gate charge behavior

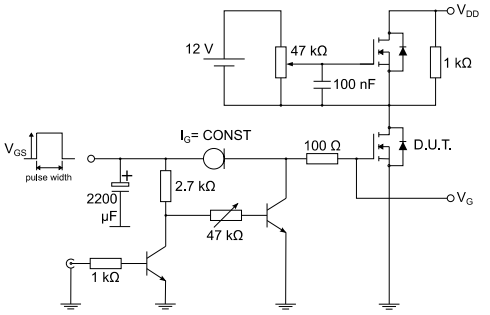


Figure 15: Test circuit for inductive load switching and diode recovery times

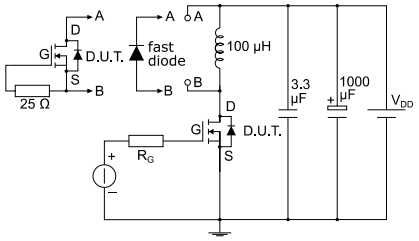


Figure 16: Unclamped inductive load test circuit

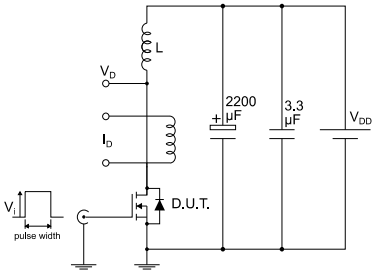


Figure 17: Unclamped inductive waveform

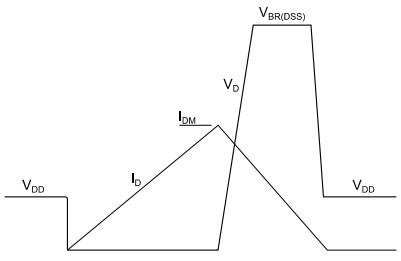
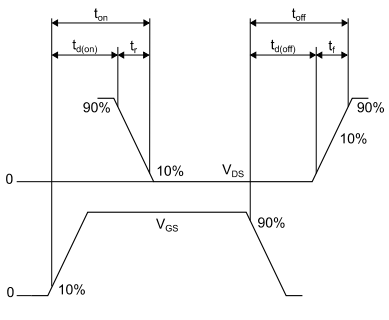


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SOT-223 package information

Figure 19: SOT-223 package outline

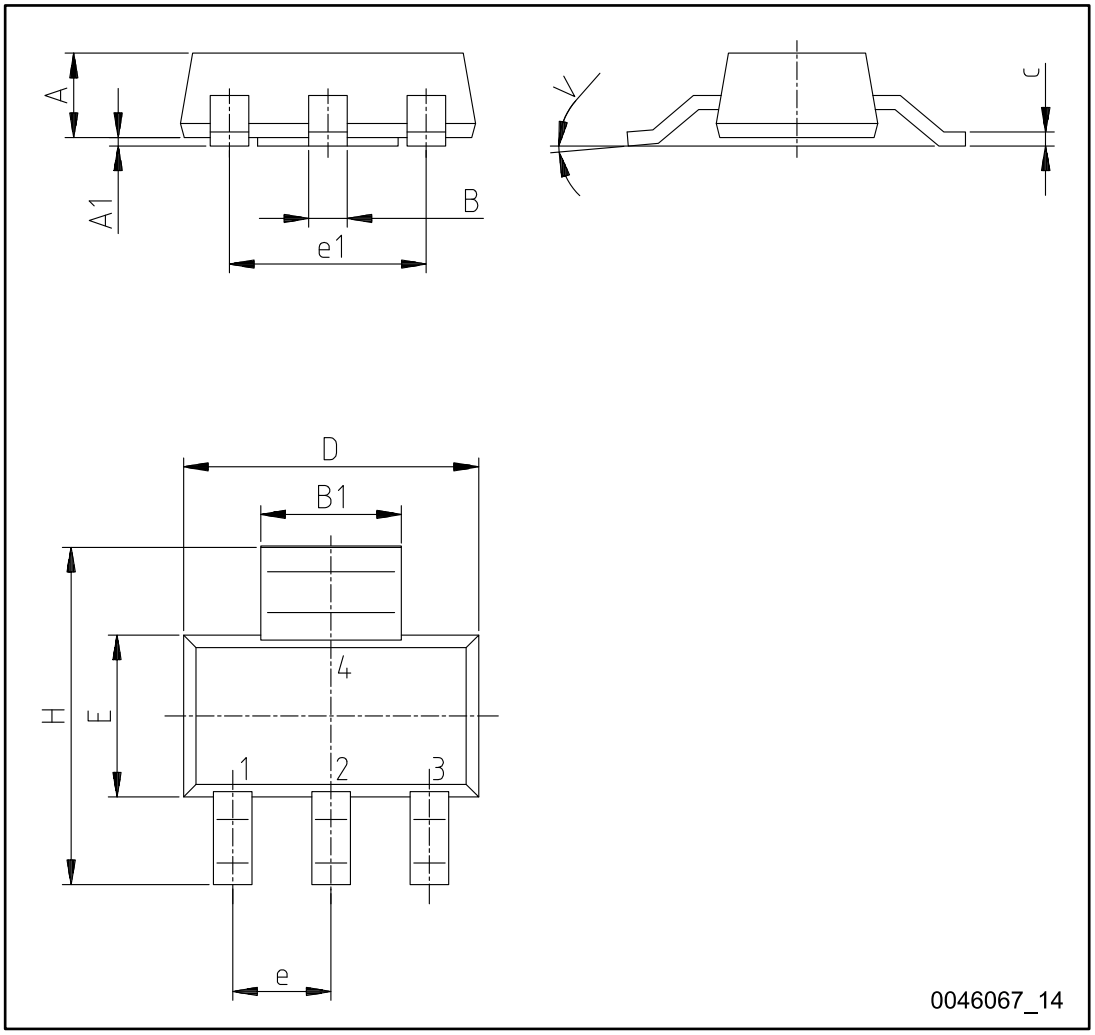
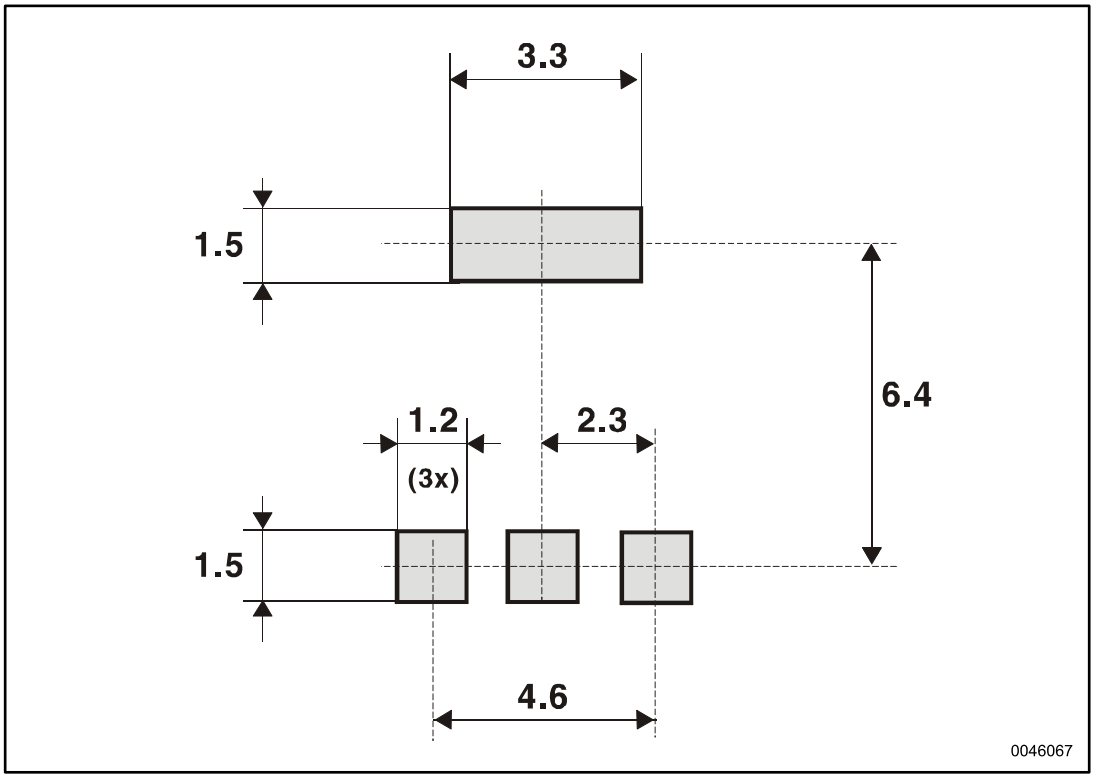


Table 8: SOT-223 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.8
A1	0.02		0.1
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7.0	7.3
V			10º

Figure 20: SOT-223 recommended footprint (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
21-Jun-2004	5	Complete version.
04-Oct-2006	6	New template, no content change.
01-Feb-2007	7	Typo mistake on Table 2.
12-Jun-2008	8	Corrected marking on Table 1
03-Jul-2017	9	Modified internal schematic diagram on cover page. Updated *Section 4: "Package information"*. Minor text changes.

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