Ten LVCMOS Output Low Additive Jitter Fanout Buffer

Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal

- Ten 1.5V/1.8V/2.5V/3.3V LVCMOS outputs

- Supports frequencies from 0 to 250MHz

- Ultra-low system level additive jitter: 17fs (12kHz to 20MHz)

- Ultra-low noise floor of -170dBc/Hz

- Supports crystals from 8MHz to 160MHz

- Supports 2.5V or 3.3V power supplies

- Output to output skew of 30ps (typical)

- Input to output delay of 2ns (typical)

- SPI or Hardware control

Ordering Information

ZL40240LDG1	32 Pin QFN	Trays
ZL40240LDF1	32 pin QFN	Tape and Reel

Package size: 5 x 5 mm
-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired and Wireless communications
- High performance microprocessor clock distribution
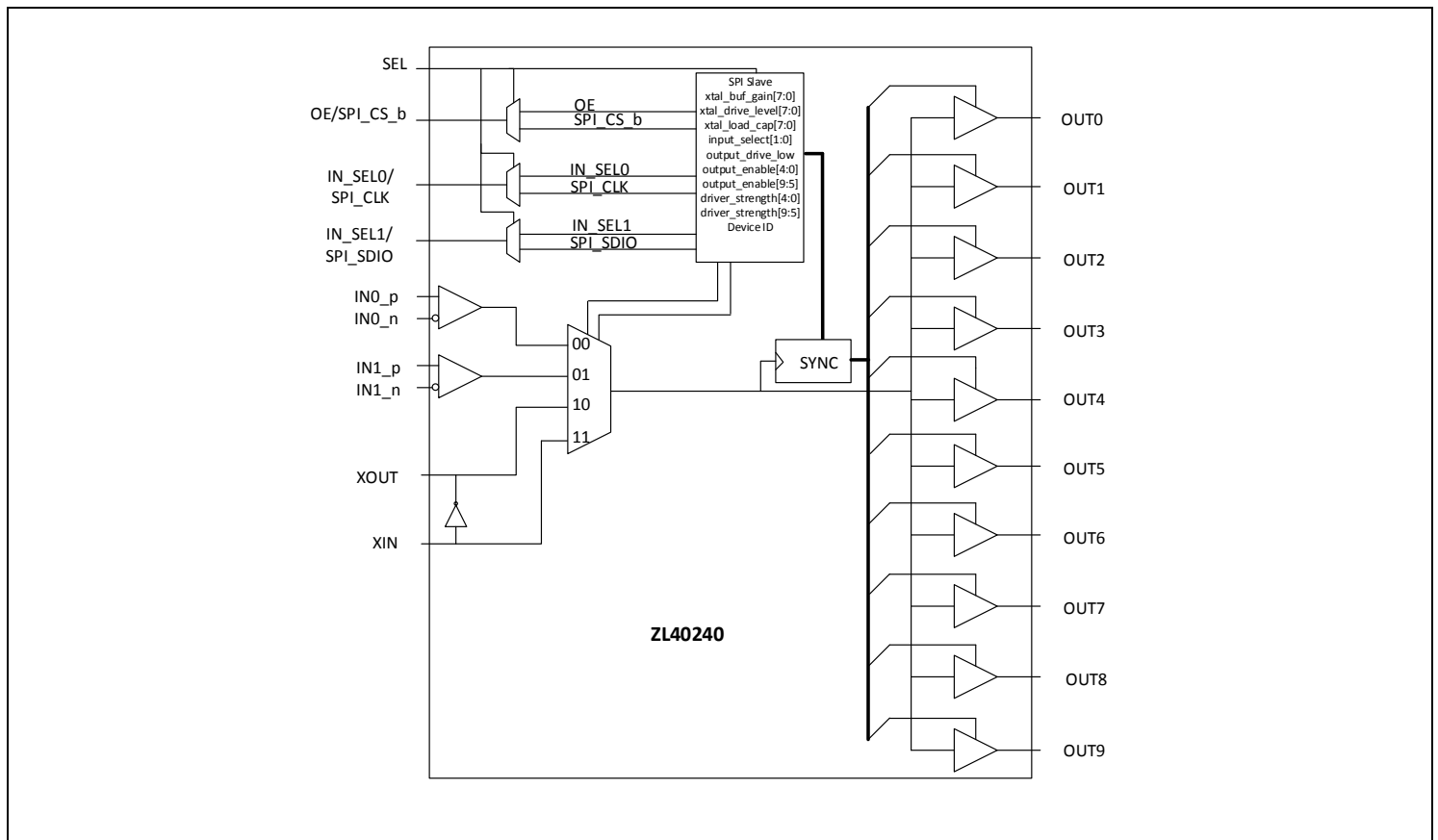- Medical Imaging
- Test equipment

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

Figure 2. Pin Diagram

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 30kΩ internal pull-up resistor, I_{APD} – input with 30kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased at VDD/2 with 60kΩ internal pull-up and 60kΩ pull-down resistors, O – output, I/O – Input/Output pin, P – power supply pin.

Table 1 · Pin Descriptions

#	Name	I/O	Description
Input Reference			
13 14 28 27	IN0_p IN0_n IN1_p IN1_n	I_{APD} $I_{APU/APD}$ I_{APD} $I_{APU/APD}$	**Input Differential or Single Ended References 0 and 1** Input frequency range 0Hz to 250MHz. Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60kΩ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
1 3 5 7 8 17 18 20 22 24	OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9	O	**Ultra Low Additive Jitter LVCMOS Outputs 0 to 9** Output frequency range 0Hz to 250MHz
Control			
30	IN_SEL0/SPI_CLK	I_{PD} or I_{PU}	**Input Select 0/ Clock for Serial Interface.** When SEL pin is low this pin is Input Select 0 hardware control input pin and it is pulled-low with 300 kΩ resistor. When SEL pin is high this pin provides clock for serial micro-port interface and it is pulled-up with 300 kΩ resistor.

IN_SEL1	IN_SEL0	OUTN
0	0	Input 0 (IN0)
0	1	Input 1 (IN1)
1	0	Crystal Oscillator or overdrive
1	1	Crystal Bypass

29	IN_SEL1/SPI_SDI	I$_{PD}$ or I$_{PU}$	**Input Select 1/ Serial Interface Input.** When SEL pin is low this pin is Input Select 1 hardware control pin and it is pulled down with 300 kΩ resistor. When SEL pin is high this pin is serial interface input stream and it is pulled-up with 300 kΩ resistor.. The serial data stream holds the access command, the address and the write data bits. **Note:** this input has low threshold voltage (V$_{IH}$ = 1.2V) so it can be driven by low output voltage device from 1.5V or higher up to VDD
32	SPI_SDO	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits.
31	OE/SPI_CS_b	I$_{PD}$ or I$_{PU}$	**Output Enable/Chip Select for Serial Interface.** When SEL pin is low this pin is Output Enable hardware control input and it is pulled-down with 300 kΩ resistor. When SEL is high this pin is serial interface chip select and it is pulled-up with 300 kΩ resistor--this is an active low signal.

Crystal Oscillator

11	XIN	I	**Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode**
12	XOUT	O	**Crystal Oscillator Output**

Hardware/SPI Control selection

16	SEL	I$_{PD}$	**Select control.** When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE. When this pin is high, the device is controlled via SPI port. Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.

Power and Ground

10	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. VDD voltage must be higher or equal to VDDO.
2 6 19	VDDO	P	**Positive Supply Voltage for LVCMOS Outputs** Connect 3.3V, 2.5V, 1.8V or 1.5V power supply

23			
4 9 15 21 26 25	GND	P	**Ground** Connect to ground
E-Pad	GND	P	**Ground.** Connect to ground

Functional Description

The ZL40240 is a programmable or hardware pin controlled low additive jitter, low power 3 x 10 LVCMOS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40240 has ten LVCMOS outputs which can be powered from 3.3V, 2.5V, 1.8V or 1.5V supply. Each output can be independently enabled/disabled via SPI bus. In addition, the strength of each output can be programmed.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40240 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each so that the transmission line is terminated with matched impedance (50Ω). However, if the driving strength of the output driver is not sufficient resistor values should be increased
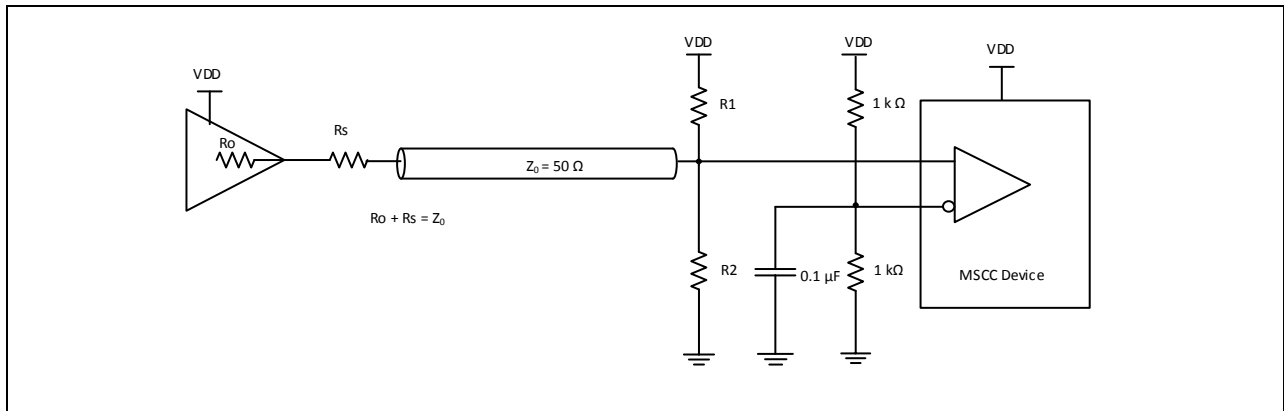
Figure 3. Input driven by a single ended output

VDD	R_{UP}	R_{DWN}
3.3V	125 Ω	84 Ω
2.5V	250 Ω	62.5 Ω
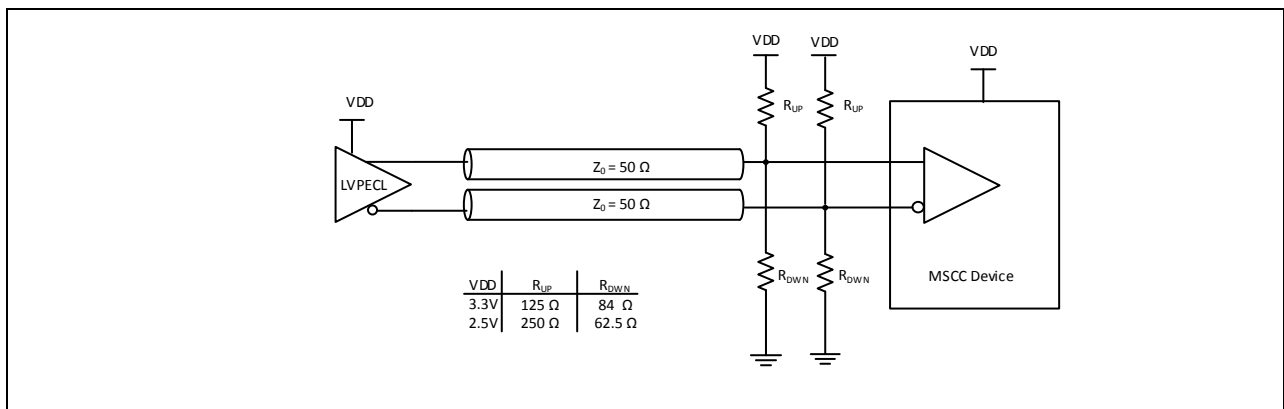
Figure 4. Input driven by DC coupled LVPEVCL output
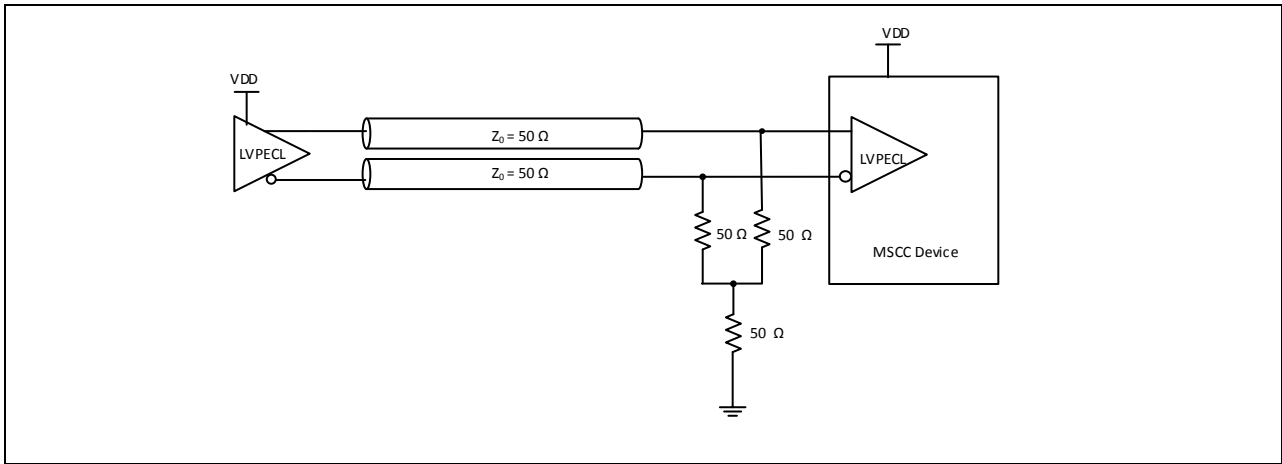
Figure 5. Input driven by DC coupled LVPEVCL output (alternative termination)
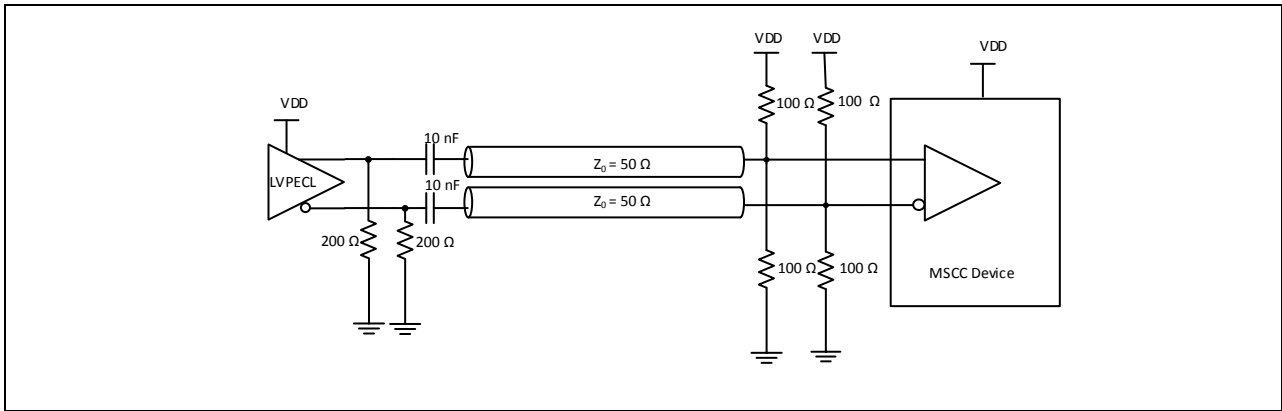
Figure 6. Input driven by AC coupled LVPECL output
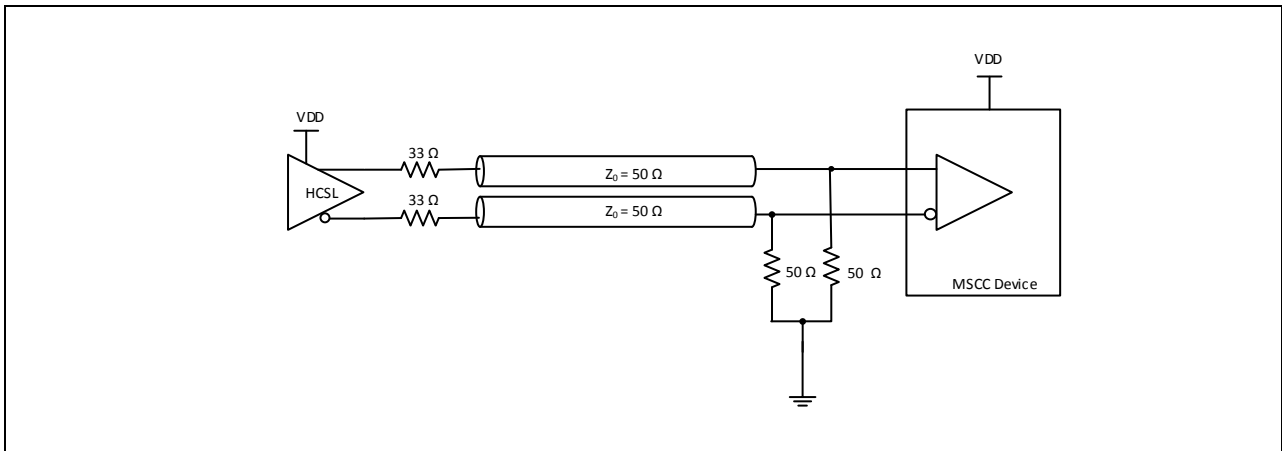
Figure 7. Input driven by HCSL output
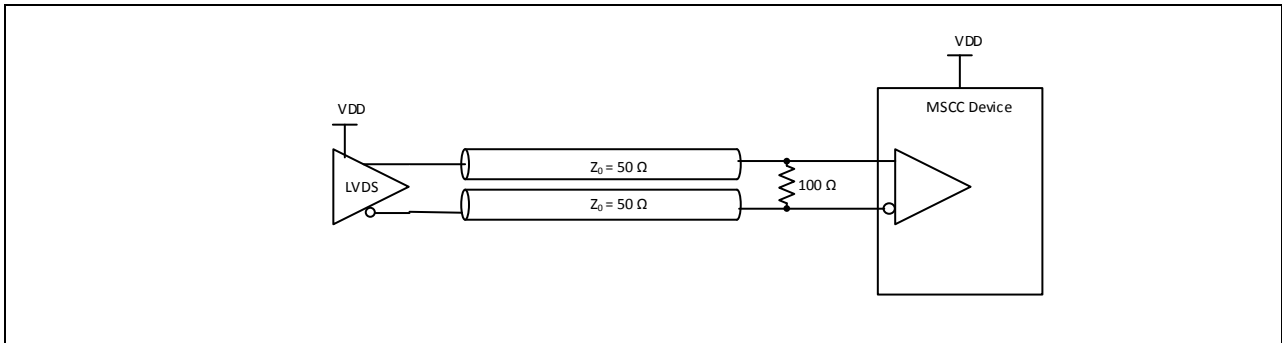
Figure 8. Input driven by LVDS output
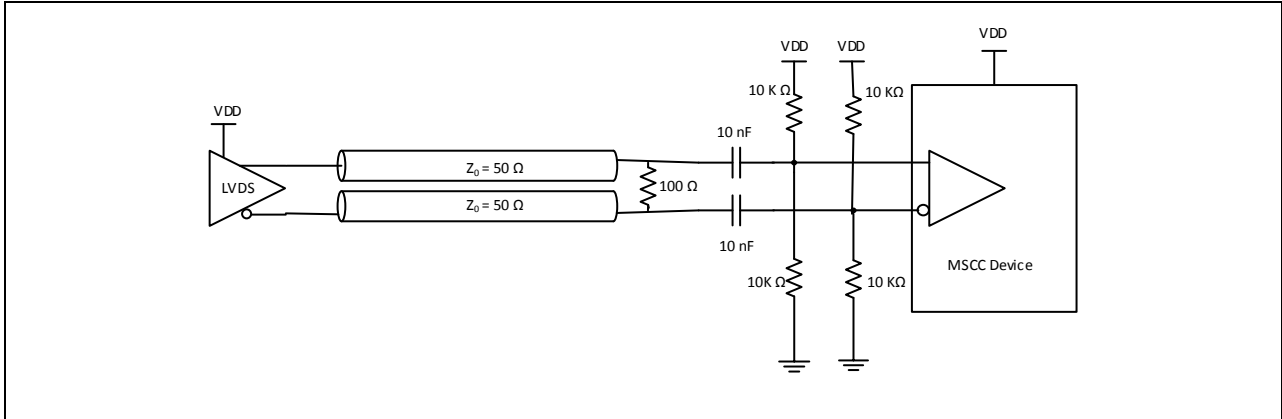
Figure 9. Input driven by AC coupled LVDS
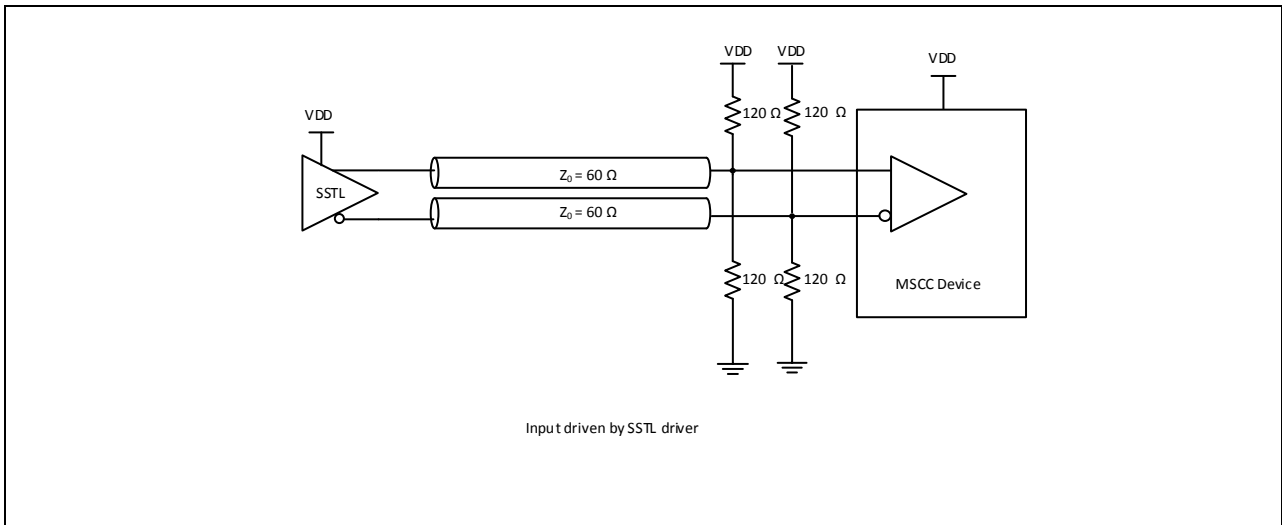
Figure 10.   Input driven by an SSTL output

Clock Outputs

LVCMOS outputs require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 11. The recommended series termination depends on programmed strength of the driver (low or high) and on the output driver supply voltage.
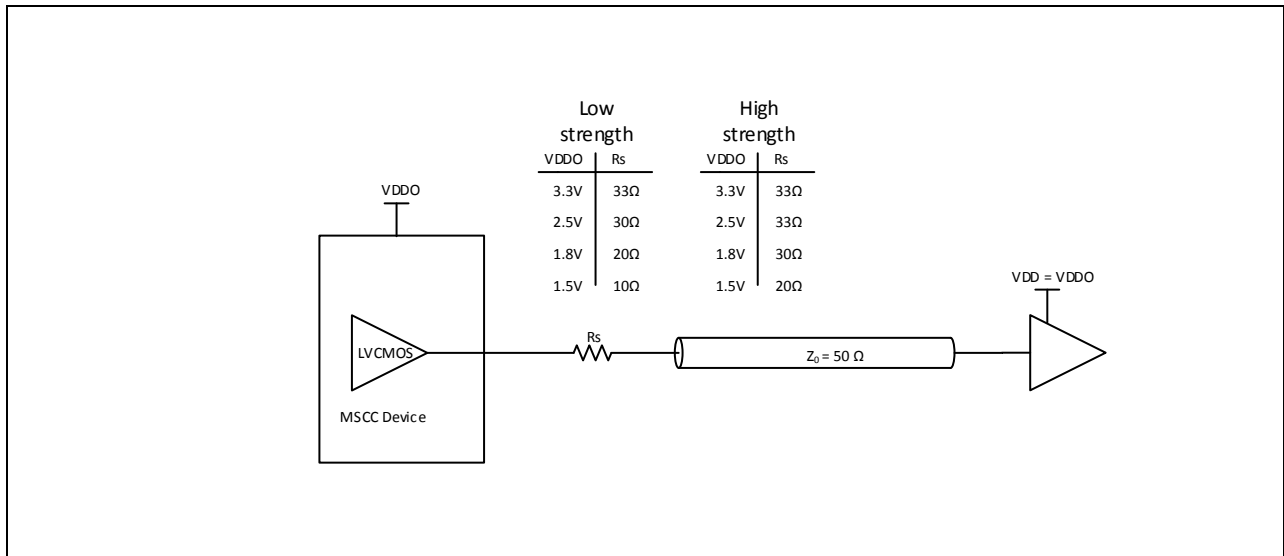
Figure 11.   Termination for LVCMOS outputs

Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 160MHz.   As can be seen in the following figure only crystal resonator is required and all the other components are built-in the device. To be able support crystal resonators with different characteristics all internal components are programmable in SPI Controlled mode.
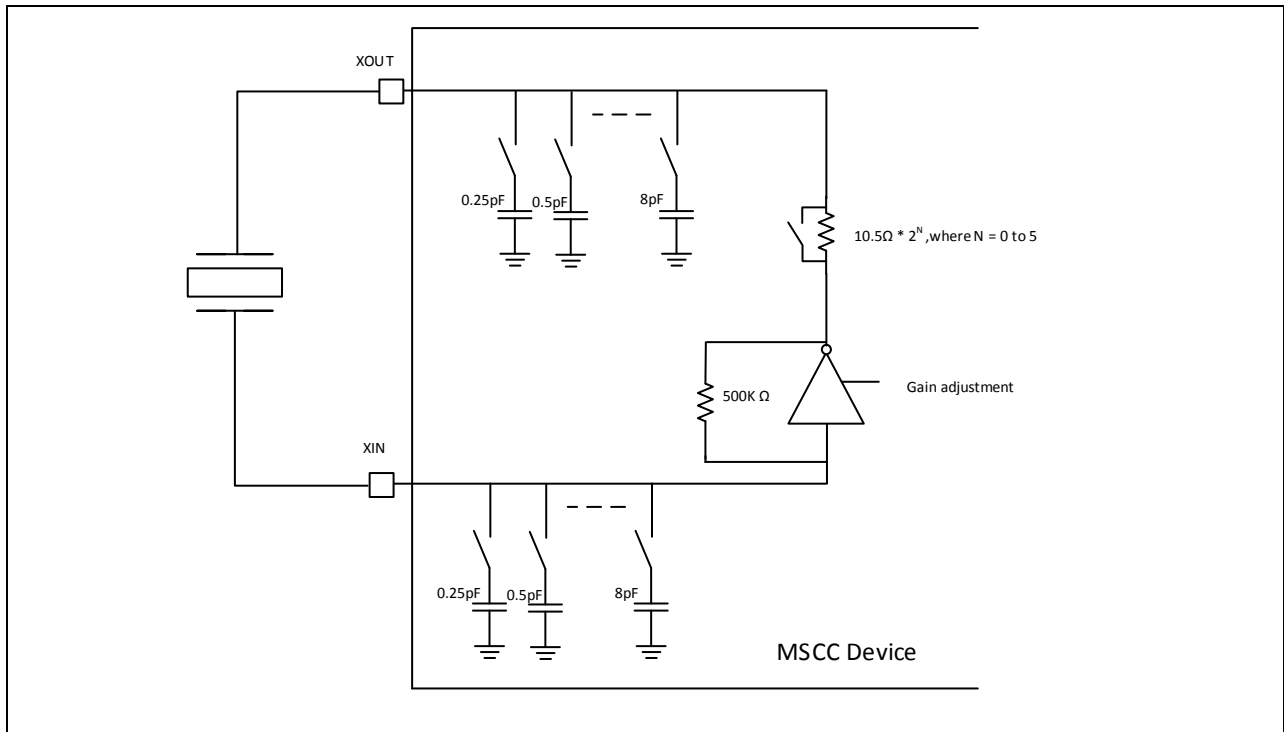
Figure 12.   Crystal Oscillator Circuit in SPI Controlled Mode

Load capacitors can be programmed from 0 to 21.75 pF with resolution of 0.25pF which not only meets load requirement for most crystal resonator but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in eight steps and the series resistor in six steps. Shunt resistor has fixed value of 500KΩ.

In Hardware Controlled mode the capacitive load is set at 8pF and cannot be changed. For Crystal requiring higher load additional capacitance can be added externally as shown in the Figure 13.
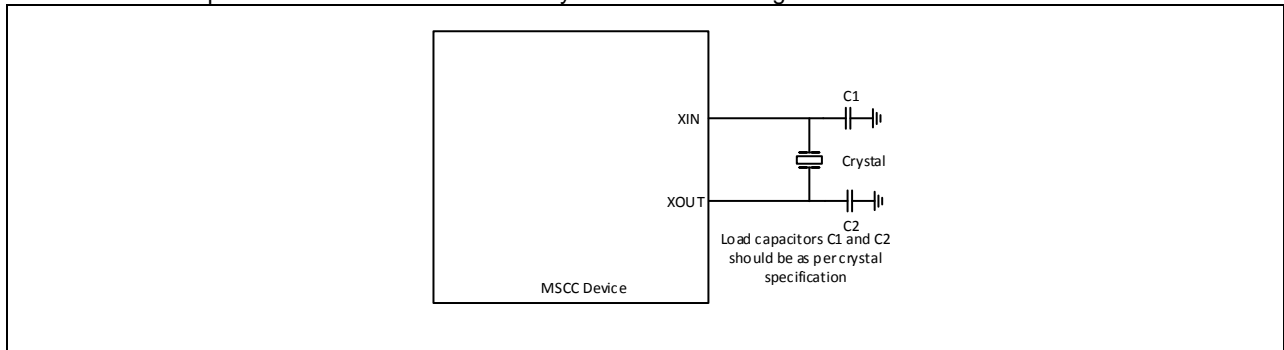
Figure 13.   Crystal Oscillator Circuit in Hardware Controlled Mode

The phase noise plot for 25MHz crystal is shown in Figure 14. The phase noise floor of the device is below -170dBc/Hz as can be seen on the figure.
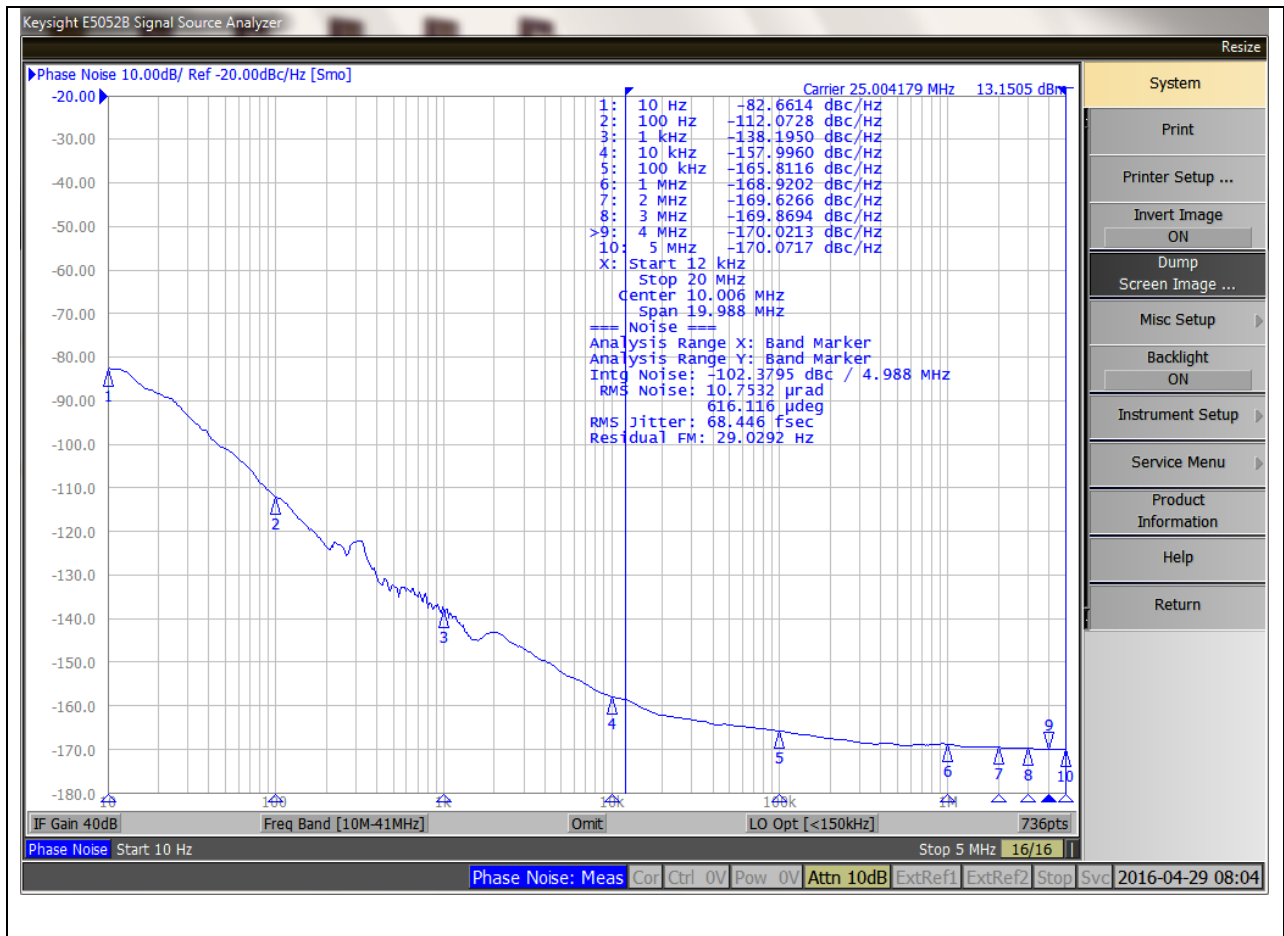
Figure 14.   Phase Noise Plot with 25MHz Crystal

Figure 15 shows the phase noise plot with 125MHz crystal.
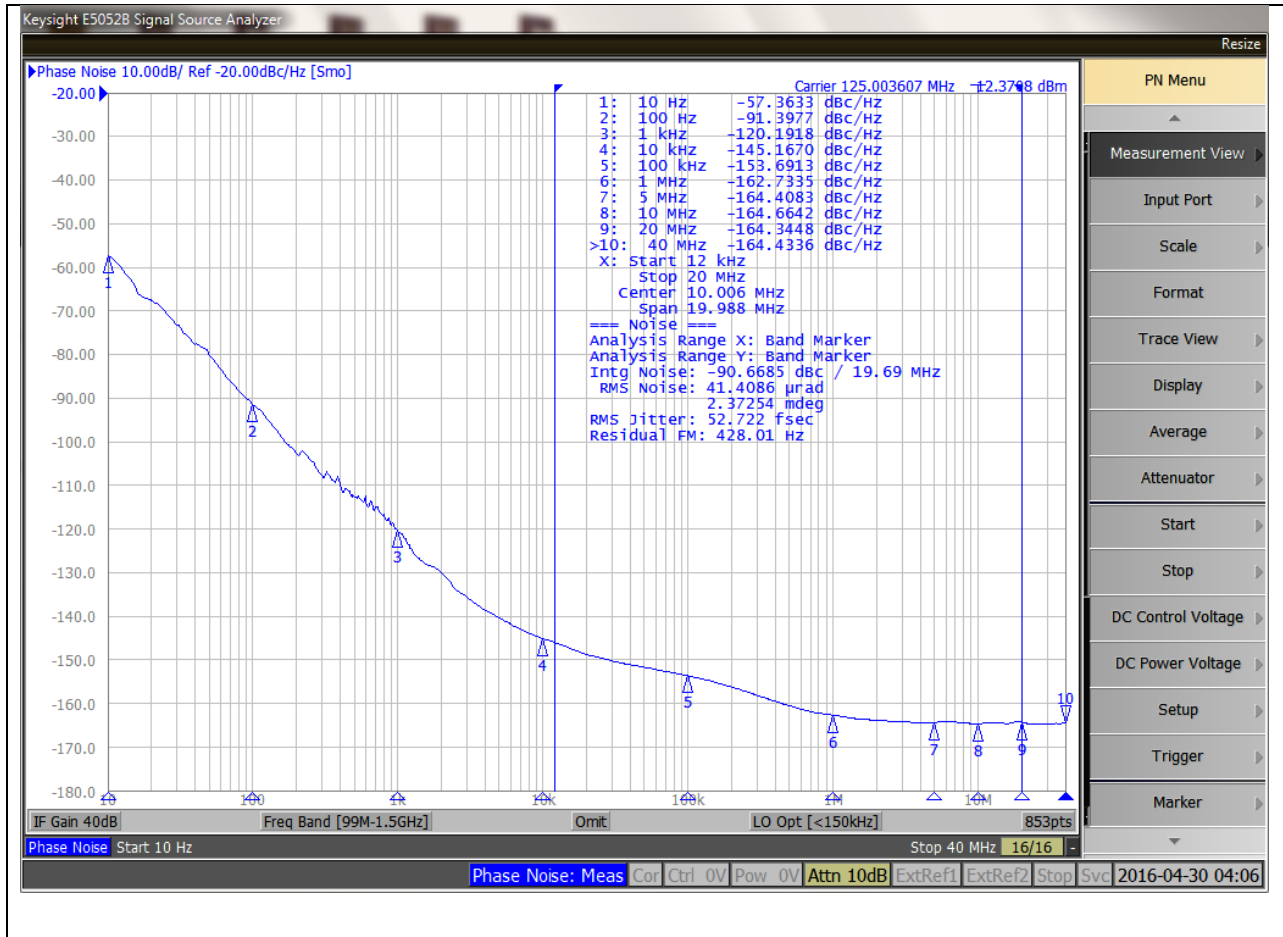
Figure 15.   Phase Noise Plot with 125 MHz Crystal

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1KΩ resistor. Unused outputs should be left unconnected.

Power Consumption

The total device power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_D$$

Where:

$$P_S = V_{DD} \times I_S$$

is static power consumed by input buffers. If XTAL is running this power should be set to zero. where the static current (I_S) is specified in Table 5 ·

$$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$$

is power consumption of XTAL circuit. The current of the XTAL circuit is provided in Table 5 · If XTAL is not used the power consumption is equal to zero.

$$P_C = V_{DDO} \times I_{DDC}$$

Common output power shared among all ten outputs. The current (I_{DDC} is specified in Table 5 · .

$$P_D = V_{DDO} \times (I_{DD} \times n \times f / 100MHz + V_{DDO} \times C_{LOAD} \times f \times n)$$

Dynamic power where dynamic current (I_{DD}) is specified in Table 5 · , C_{LOAD} is capacitive load driven by an output, f is frequency of the output clock and n is number of active outputs.

The power consumption for different clock frequencies and power supply voltages can be quickly estimated from Figure 16, Figure 17 and Figure 17.
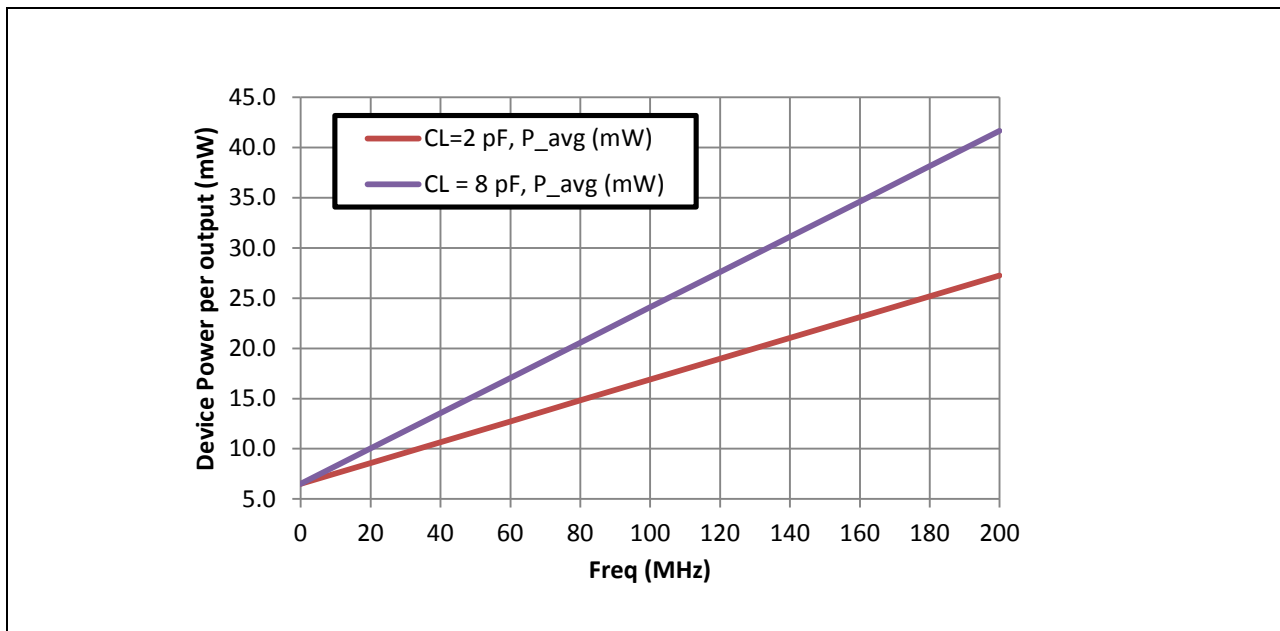
Figure 16.   Device power consumption per output for $V_{DD} = V_{DDO}$ = 3.465V
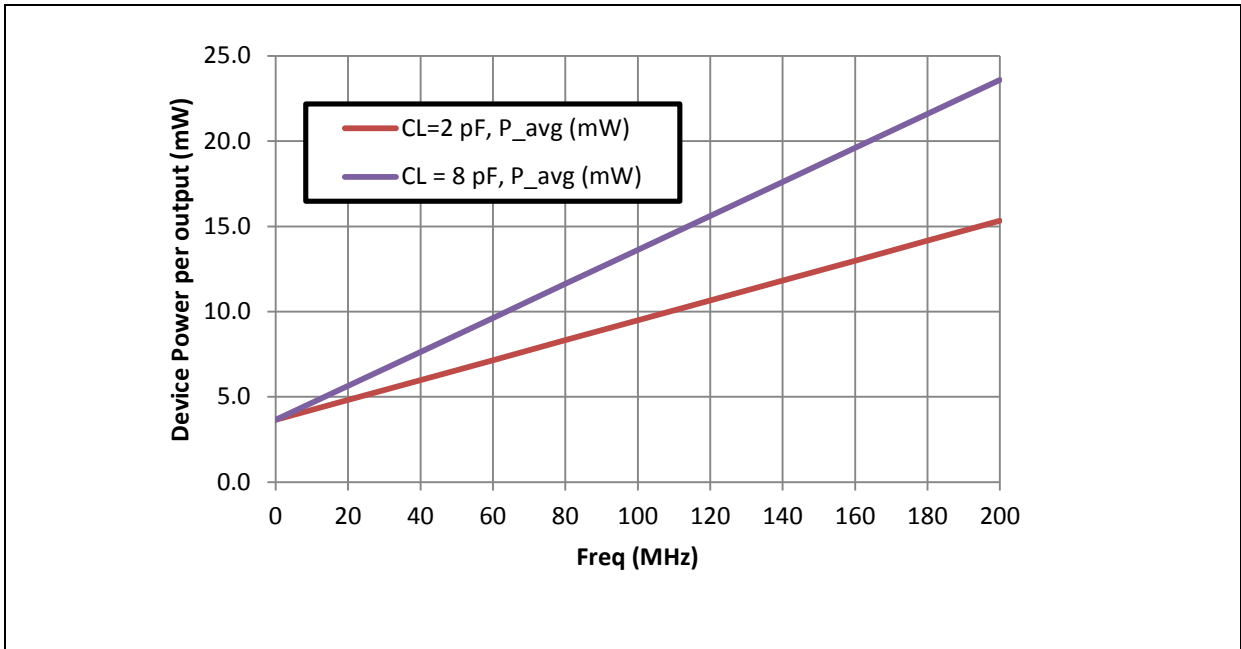
Figure 17.   Device power consumption per output for $V_{DD} = V_{DDO} = 2.625V$
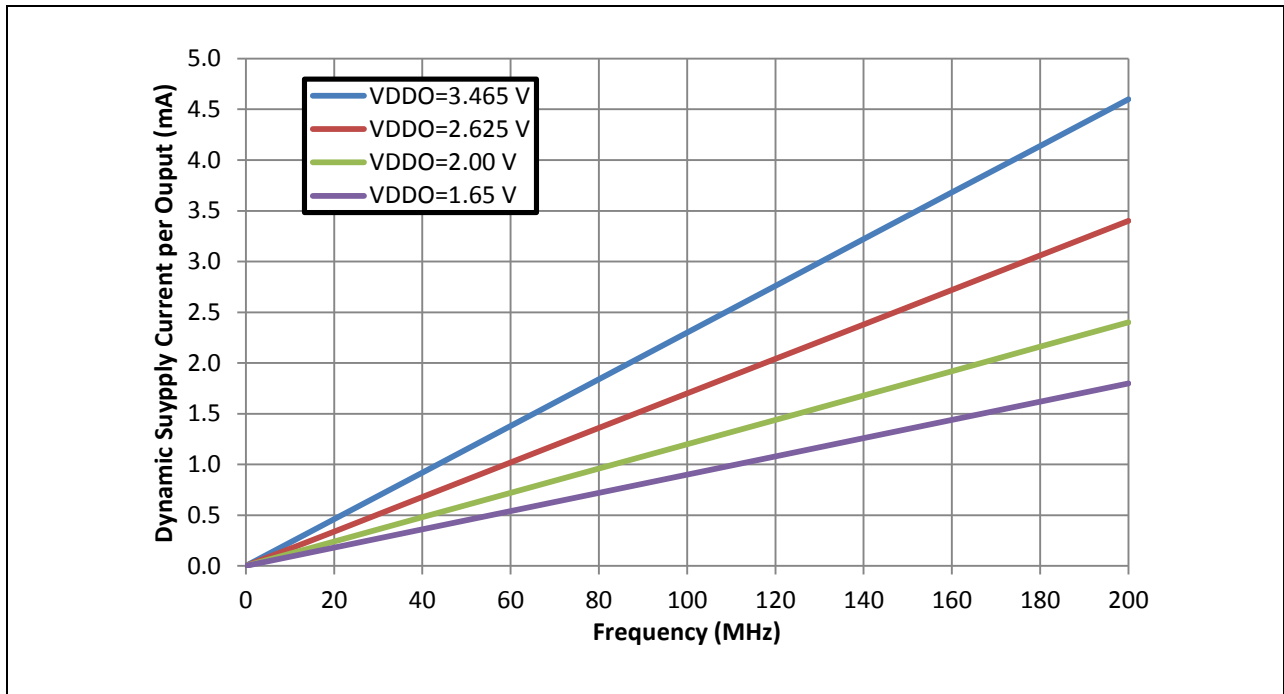
Figure 18.   Dynamic supply current per output for different output supply voltages

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1μF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulted with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.
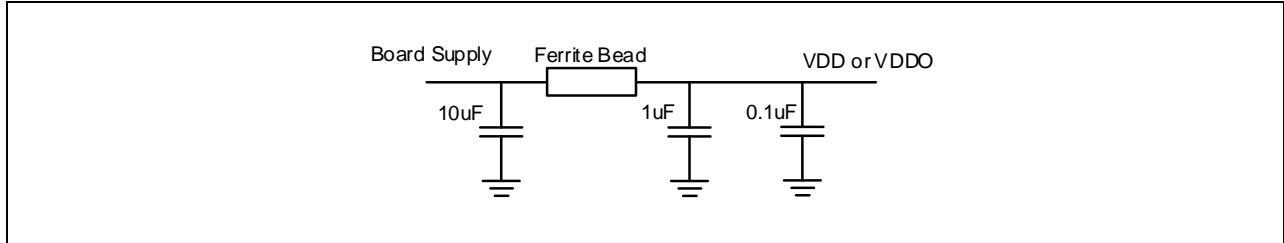
Figure 19.   Power Supply Filtering

Device Control

ZL30240 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

Hardware Control Mode

In this mode, ZL40240 is controlled via Output Enable (OE) and Input Select (SEL0/1) input pins. Output is disabled synchronously on the falling edge of the input (t_2) as shown in Figure 20.
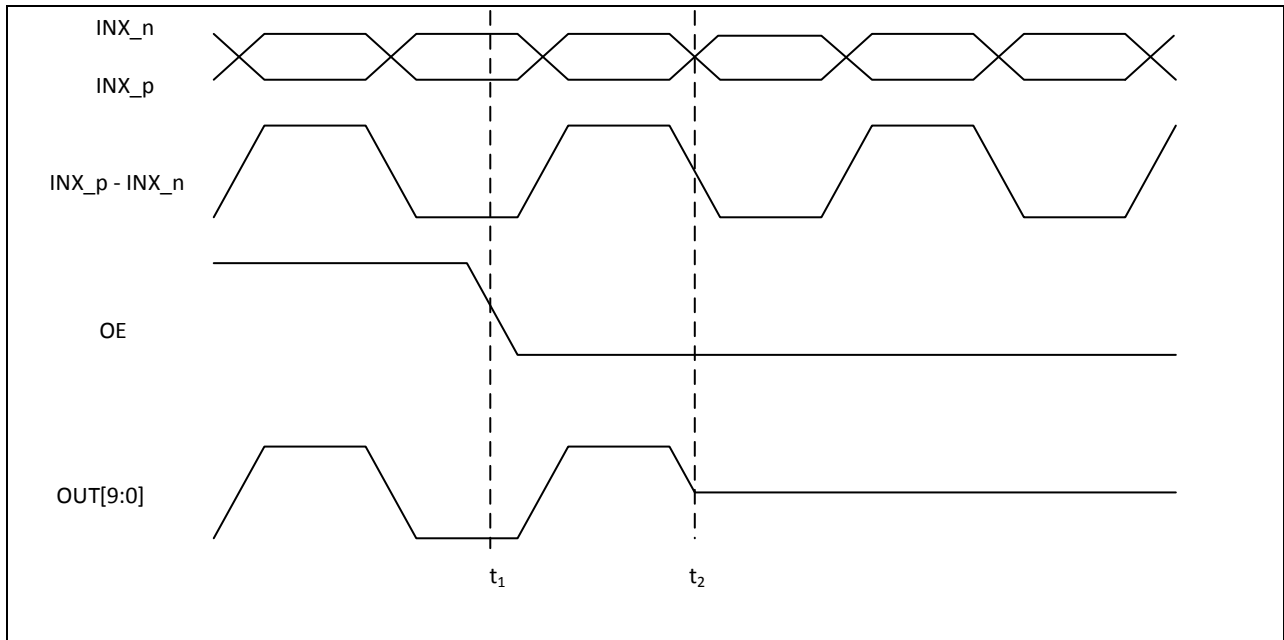
Figure 20.   OE Output Disable

Outputs can be enabled by toggling OE pin high. As soon as OE pin goes high (t_1) the outputs will go from high-Z to low and will start to track the input after the first falling edge (t_2) of the input signal as shown in Figure 21.
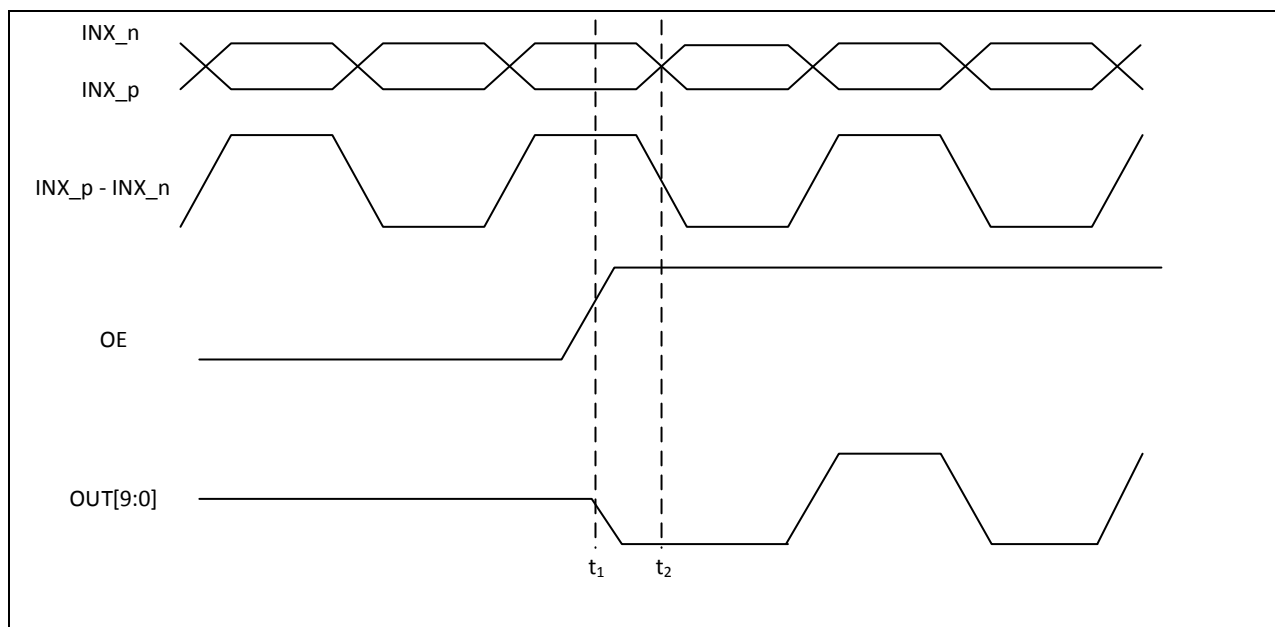
Figure 21.   OE Output Enable

SPI Controlled Mode

In this mode ZL40240 is controlled via four pin SPI slave interface as shown in the following figure.
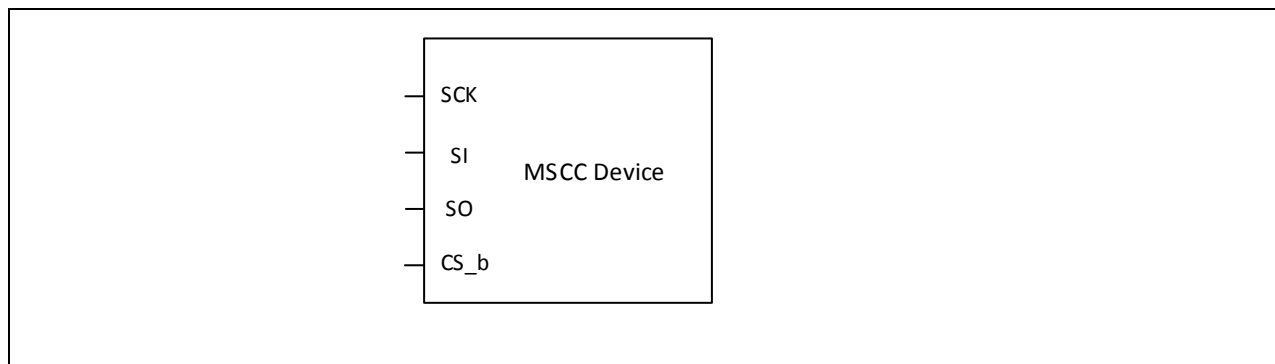
Figure 22.   SPI slave interface

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS_b** pin is active. If the **SCK** pin is low during **CS_b** activation, then MSb first timing is selected. If the **SCK** pin is high during **CS_b** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_b** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS_b** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 23 and Figure 24 respectively. Figure 25 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.
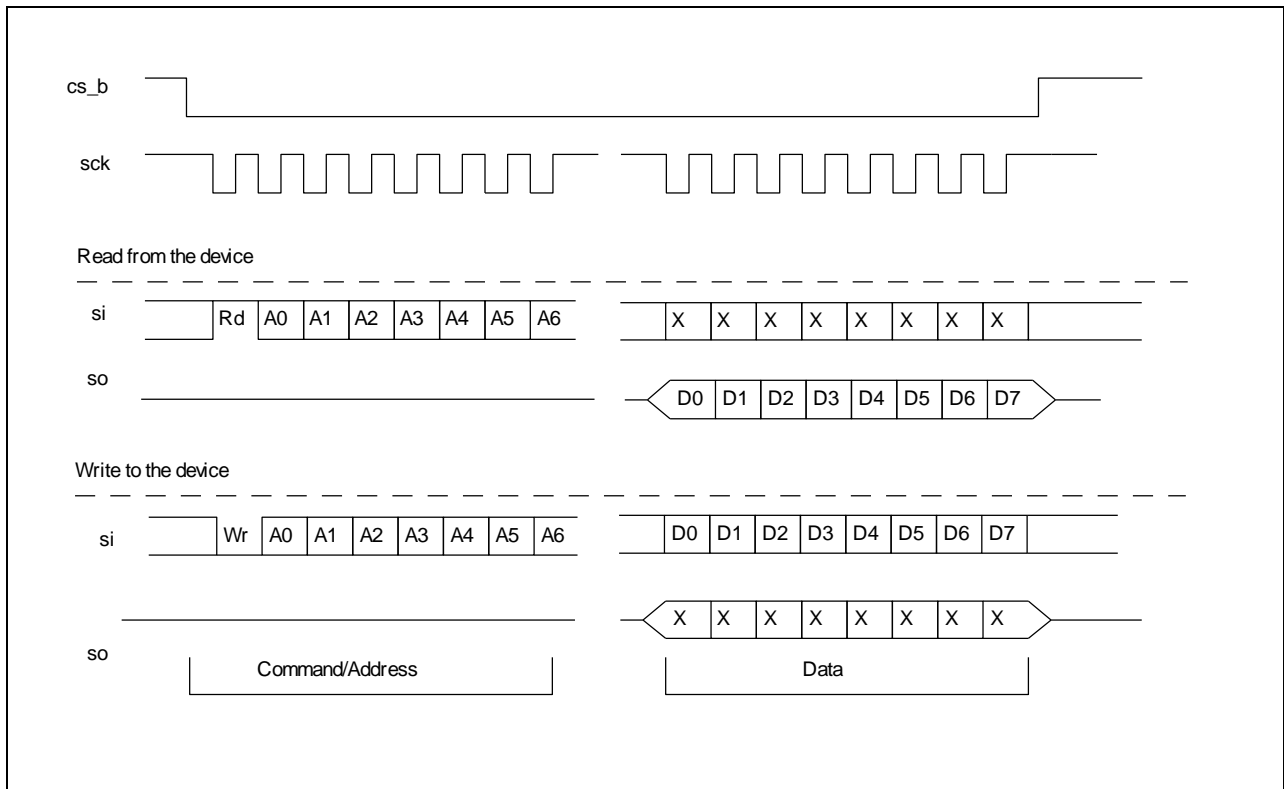
Figure 23.   Serial Peripheral Interface Functional Waveform – LSB First Mode
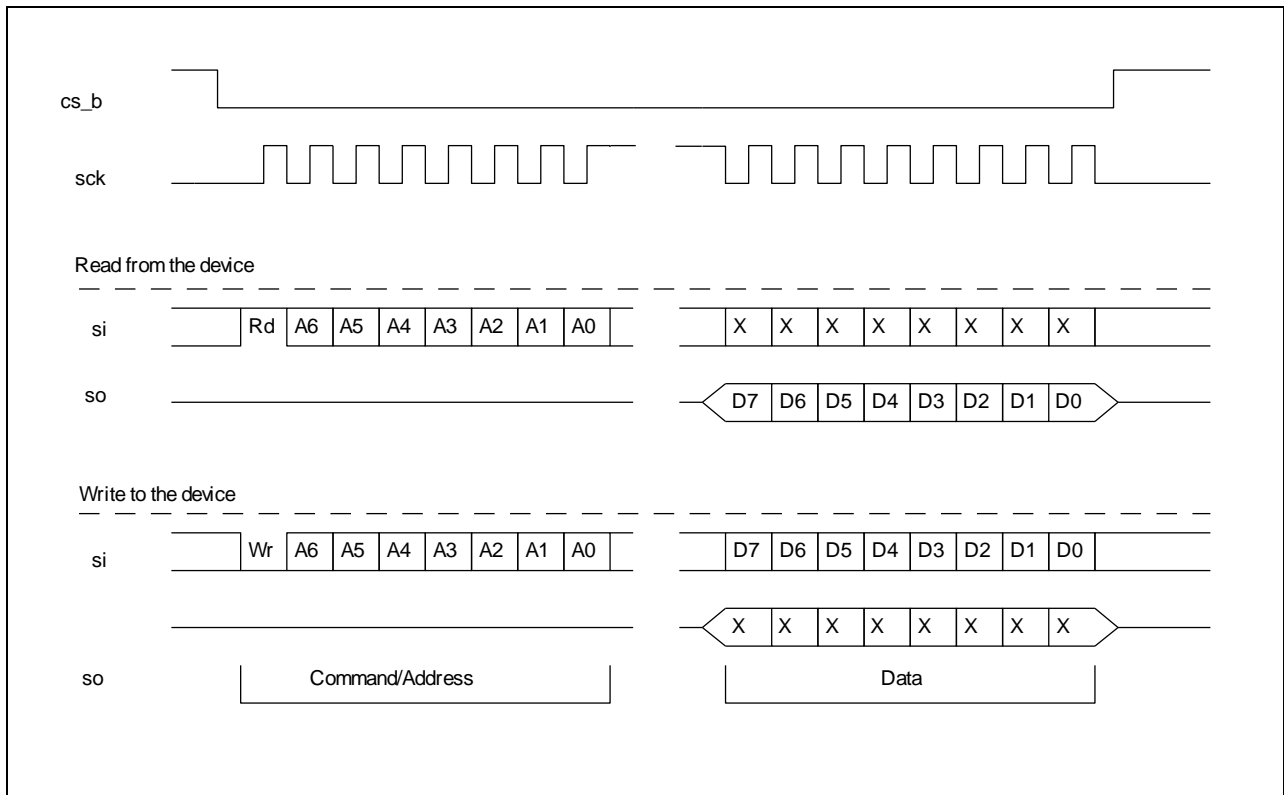
Figure 24.   Serial Peripheral Interface Functional Waveform – MSB First Mode
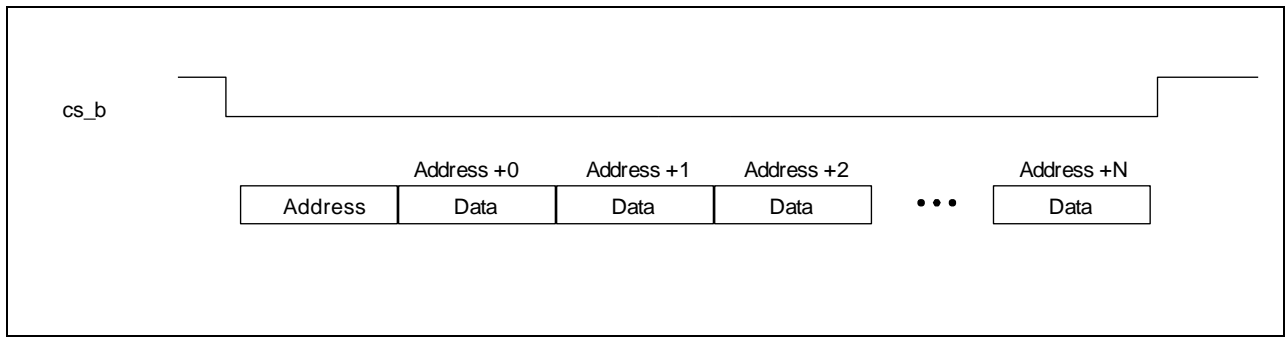
Figure 25.   Example of the Burst Mode Operation

Register Map

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

Table 2 · Register Map

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	-	Not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	OUTEN0	output_enable[4:0]
08	OUTEN1	output_enable[9:5]
09	DRVSTR0	driver_strength[4:0]
0A	DRVSTR1	driver_strength[9:5]
0B/0C/0D/0E	-	Not used
0F/10	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default

Address	0x00			Hex
XTALBG		**XTAL Buffer Gain**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:0	xtal_buf_gain[7:0]	Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared). Minimum gain is 0x00 (default) and 0xFF is maximum gain When reference input mode is "bypass XTAL mode" or "differential input modes" with HIGH xtal_normal_run bit, the buffer is disabled and follows "Input Selection". When xtal_normal_run bit is LOW, XTAL buffer is in the "xtal forced run" mode and keep running. 8'b0000_0000: default crystal buffer strength. 8'b0000_0011: enable additional buffer strength 8'b0000_1100: enable additional buffer strength 8'b0011_0000: enable additional buffer strength 8'b1100_0000: enable additional buffer strength	RW	FF

Address	0x01			Hex
XTALDL		**XTAL Drive Level**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:0	xtal_drive_level[7:0]	Internal damping resistance of crystal circuit to limit external crystal's drive level uW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Resistors are connected in parallel. Hence, 0xFF is the smallest resistance and 0x01 is the highest resistance. 8'b0000_0000: disable all resistors 8'b0000_0001: 312 Ohm resistor 8'b0000_0010: 161 Ohm resistor 8'b0000_0100: 84 Ohm resistor 8'b0000_1000: 42 Ohm resistor 8'b0001_0000: 21 Ohm resistor 8'b0010_0000: 10.5 Ohm resistor 8'b0100_0000: 0 Ohm connection 8'b1000_0000: not used	RW	03

Address	0x02				Hex
XTALLC		**XTAL Load Capacitance**			
Bit	**Name**	**Description**	**Type**	**Reset**	
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 21.75pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors. 8'b0000_0000: disable all xtal load capacitors 8'b0000_0001: enable capacitor 0.25 pF 8'b0000_0010: enable capacitor 0.5 pF 8'b0000_0100: enable capacitor 1 pF 8'b0000_1000: enable capacitor 2 pF 8'b0001_0000: enable capacitor 2 pF 8'b0010_0000: enable capacitor 4 pF 8'b0100_0000: enable capacitor 4 pF 8'b1000_0000: enable capacitor 8 pF	RW	80 (8 pF)	

Address	0x03				Bin
XTALNR		**XTAL Normal Run**			
Bit	**Name**	**Description**	**Type**	**Reset**	
7:1	Unused	Unused	R	1111111	
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance--XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1	

Address	0x05				Bin
INSEL		**Input Select Register**			
Bit	**Name**	**Description**	**Type**	**Reset**	
7:2	Unused	Unused	R	11111	
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required. 2'b00: differential input from IN0_p and IN0_n 2'b01: differential input from IN1_p and IN1_n 2'b10: 1) fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) OR 2) XTAL overdrive mode (single-ended clock signal with XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)	RW	10	

Address	0x06			Bin
OUTLOW		**Output Drive Low**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:1	Unused	Unused	R	1111111
0	output_drive_low	After disabling outputs, output state is known state in logic LOW. (This bit is used for only disabled outputs. Otherwise, enabled outputs are not impacted by this bit.) 1'b0: All LVCMOS outputs will be in high-impedance state. 1'b1: All LVCMOS outputs will drive logic LOW.	RW	0

Address	0x07			Bin
OUTEN0		**Output Enable 0**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:5	Unused	Unused	R	111
4:0	output_enable[4:0]	Output enable for OUT0/1/2/3/4. Disabled state is dependent on "out_drive_low" control bit. Each bit controls one output. 5'b0_0000: disable outputs 5'b0_0001: enable OUT0 5'b0_0010: enable OUT1 5'b0_0100: enable OUT2 5'b0_1000: enable OUT3 5'b1_0000: enable OUT4	RW	11111

Address	0x08			Hex
OUTEN1		**Output Enable 1**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:5	Unused	Unused	R	111
4:0	output_enable[9:5]	Output enable for OUT5/6/7/8/9. Disabled state is dependent on "out_drive_low" control bit. Each bit controls one output. 5'b0_0000: disable outputs 5'b0_0001: enable OUT5 5'b0_0010: enable OUT6 5'b0_0100: enable OUT7 5'b0_1000: enable OUT8 5'b1_0000: enable OUT9	RW	11111

Address	0x09			Hex
DRVSTR0		**Driver Strength 0**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:5	Unused	Unused	R	111
4:0	driver_strength[4:0]	Output driver strength for OUT0/1/2/3/4. Each bit controls one output. Low driver strength and high driver strength. 5'b0_0000: low driver strength outputs 5'b0_0001: high driver strength for OUT0 5'b0_0010: high driver strength for OUT1 5'b0_0100: high driver strength for OUT2 5'b0_1000: high driver strength for OUT3 5'b1_0000: high driver strength for OUT4	RW	11111

Address	0x0A			Hex
DRVSTR1		**Driver Strength 1**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:5	Unused	Unused	R	111
4:0	driver_strength[9:5]	Output driver strength for OUT5/6/7/8/9. Each bit controls one output. Low driver strength and high driver strength. 5'b0_0000: low driver strength outputs 5'b0_0001: high driver strength for OUT5 5'b0_0010: high driver strength for OUT6 5'b0_0100: high driver strength for OUT7 5'b0_1000: high driver strength for OUT8 5'b1_0000: high driver strength for OUT9	RW	11111

Address	0x11			Hex
DEVID		**Device Identification**		
Bit	**Name**	**Description**	**Type**	**Reset**
7:5	Unused	Unused	R	0
4:0	dev_id	Device ID. 5'h01: ZL40240	RO	01

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 3 · Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD}/V_{DDO}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD}/V_{DDO}	-0.5		4.6	V	
3	Supply voltage (1.8V)	V_{DDO}	-0.5		2.5	V	
4	Supply voltage (1.5V)	V_{DDO}	-0.5		2.0	V	
5	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions

Table 4 · Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD}/V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD}/V_{DDO}	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V_{DDO}	1.6	1.8V	2	V	
4	Supply voltage 1.5V	V_{DDO}	1.35	1.5	1.65		
5	Operating temperature	T_A	-40	25	85	°C	
6	Input voltage	V_{DD-IN}	-0.3		V_{DD} + 0.3	V	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V and 2.5V)

Table 5 · Current consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Static device current	$I_{s\_3.3V}$		15	18	mA	VDD= 3.465V
		$I_{s\_2.5V}$		12	15	mA	VDD = 2.625V
2	Device current with 25MHz XTAL input	$I_{DD\_XTAL\_3.3V}$		24	27	mA	VDD= 3.465V
		$I_{DD\_XTAL\_2.5V}$		18	20	mA	VDD= 2.625V
3	Dynamic current per output (f = 100MHz) [1][2] Needs to be scaled for different frequencies by f/100MHz, Driving Strength = 1 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$		4.2	4.7	mA	VDDO= 3.465V
		$I_{DD\_2.5V}$		3.0	3.5	mA	VDDO= 2.625V
		$I_{DD\_1.8V}$		2.1	2.4	mA	VDDO= 2V
		$I_{DD\_1.5V}$		1.6	1.8	mA	VDDO= 1.65V
4	Dynamic current per output (f = 100MHz) [1][2] Needs to be scaled for different frequencies by f/100MHz, Driving Strength = 0 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$		2.3	3.0	mA	VDDO= 3.465V
		$I_{DD\_2.5V}$		1.7	1.8	mA	VDDO= 2.625V
		$I_{DD\_1.8V}$		1.2	1.3	mA	VDDO= 2V
		$I_{DD\_1.5V}$		0.9	1.0	mA	VDDO= 1.65V
5	Common output current[3]	$I_{DDC\_3.3V}$		3.8	4.8	mA	VDDO= 3.465V
		$I_{DDC\_2.5V}$		1.9	2.4	mA	VDDO= 2.625V
		$I_{DDC\_1.8V}$		1.2	1.5	mA	VDDO= 2V
		$I_{DDC\_1.5V}$		1	1.3	mA	VDDO= 1.65V

(1)   Needs to be scaled for different frequencies by f/100MHz
(2)   To calculate total power consumption use following formula: $P = (I_s + I_{DD\_XTAL}) * VDD + (I_{DDC} + I_{DD} * n * f/100MHz + VDDO * C_{LOAD} * f * n) * VDDO$, where
       I_{DD_XTAL}: should be set to zero if XTAL is not used or I_s should be set to zero if XTAL is used.
       n: number of active outputs
       f: frequency of the clock
       C_{LOAD}: is capacitive load driven by an output.
(3)   This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs

Table 6 · Input Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIH}	1.20			V	
2	CMOS low-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIL}			0.45	V	
3	CMOS input leakage current for SPI_CLK, SPI_CS and SPI_SDI	I_{IL}	-40		10	µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	0.5		VDD – 0.85	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n	V_{ID}	0.15		1.3	V	
6	Differential input leakage current for IN0_p/n and IN1_p/n (includes current in pull-up and pull-down resistors)	I_{IL}	-200		100	µA	$V_I = V_{DD}$ or 0 V
7	Single ended input high voltage for IN_0_p and IN_1_p	V_{SIH}	2		VDD + 0.3V	V	VDD = 3.3V+/-5%
		V_{SIH}	1.6		VDD + 0.3V	V	VDD = 2.5V+/-5%
8	Single ended input low voltage for IN_0_p and IN_1_p	V_{SIL}	-0.3		1.3	V	VDD = 3.3V+/-5%
		V_{SIL}	-0.3		0.9	V	VDD = 2.5V+/-5%
9	Input frequency	f_{IN}	0		250	MHz	
10	Input duty cycle	dc	35%		65%		@250MHz; for lower frequencies duty cycle can be scaled proportionally
11	Input slew rate	slew		2		V/ns	
12	Input pull-up/ pull-down resistance	R_{PU}/R_{PD}		60kΩ			
13	Input pull-down resistance (INx_p)	R_{PD}		30kΩ			

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

Table 7 · Crystal Oscillator Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode	Fundamental				
2	Frequency	f	8		160	MHz	
3	On chip load capacitance	C_L	0		21.75	pF	Programmable
4	On chip series resistor	R_S	0		312	Ω	Programmable
5	On chip shunt resistor	R		0.5		MΩ	
6	Maximum frequency in overdrive mode[1]	f_{OV}	0.1		200	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1uF assumed)
7	Maximum frequency in bypass mode[2]	f_{BP}	0		200	MHz	Functional but may not meet AC parameters

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

(1)   Maximum input level is 2V
(2)   Maximum output level is VDD

Table 8 · LVCMOS Output Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{OH}	0.8*VDDO			V	VDDO = 3.3V±5%
		V_{OH}	0.8*VDDO			V	VDDO = 2.5V±5%
		V_{OH}	0.7*VDDO			V	VDDO = 1.8V±10%
		V_{OH}	0.7*VDDO			V	VDDO = 1.5V±10%
2	Output low voltage	V_{OL}			0.2*VDDO	V	VDDO = 3.3V±5%
		V_{OL}			0.2*VDDO	V	VDDO = 2.5V±5%
		V_{OL}			0.3*VDDO	V	VDDO = 1.8V±10%
		V_{OL}			0.3*VDDO	V	VDDO = 1.5V±10%
3	Output impedance	R_O		17		Ω	VDDO = 3.3V
		R_O		21		Ω	VDDO = 2.5V
		R_O		30		Ω	VDDO = 1.8V
		R_O		42		Ω	VDDO = 1.5V
4	Output slew rate-- rise or fall (20% to 80%)	t_r, t_f	3.19	5.14	6.33	V/ns	VDDO = 3.3V±5%
		t_r, t_f	1.72	3.74	4.61	V/ns	VDDO = 2.5V±5%
		t_r, t_f	1.64	2.52	3.32	V/ns	VDDO = 1.8V±10%
		t_r, t_f	1.20	1.96	2.54	V/ns	VDDO = 1.5V±10%
5	Output frequency	F_O	0		250	MHz	
6	Output Duty Cycle		50.26%		53.18%		Input. duty-cycle 50%
7	Output enable or disable time				2	Cycle	
8	Output to output skew	t_{OOSK}			27	ps	
9	Device to device output skew	t_{DOOSK}			1.6	ns	
10	Input to output delay	t_{IOD}	1.15	2.09	2.54	ns	VDD = 3.3V
		t_{IOD}	1.57	2.27	2.77	ns	VDD = 2.5V
11	Input multiplexer isolation	iso	75			dB	tested with 125MHz clocks

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Load 50 Ohm to VDDO/2

Table 9 · LVCMOS Output Additive Jitter and Phase Noise*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	System level additive jitter[1]		17		fs-RMS	VDD = 3.3V, VDDO = 3.3V f_{in} = 125MHz, single ended input
			31		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V fin = 125MHz, single ended input
			22		fs-RMS	VDD = 3.3V, VDDO = 3.3V fin = 125MHz, differential input
			37		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V fin = 125MHz, differential input
2	Additive jitter[2] [3]		45.18	93.11	fs-RMS	VDD = 3.3V, VDDO = 3.3V fin = 125MHz, single ended input
			80.46	126.92	fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V fin = 125MHz, single ended input
			39.95	68.98	fs-RMS	VDD = 3.3V, VDDO = 3.3V fin = 125MHz, differential input
			67.18	117.26	fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V fin = 125MHz, differential input
3	Phase Noise floor (VDD = 3.3V, VDDO = 3.3V)		-145.08	-138.67	dBc/Hz	@10kHz, f_{in} = 125MHz, single ended input
			-152.46	-145.82	dBc/Hz	@100kHz, f_{in} = 125MHz, single ended input
			-160.67	-155.66	dBc/Hz	@1MHz, f_{in} = 125MHz, single ended input
			-162.66	-160.55	dBc/Hz	@10MHz, f_{in} = 125MHz, single ended input
			-162.71	-160.19	dBc/Hz	@20MHz, f_{in} = 125MHz, single ended input
			-145.34	-137.83	dBc/Hz	@10kHz, f_{in} = 125MHz, differential input
			-152.60	-146.93	dBc/Hz	@100kHz, f_{in} = 125MHz, differential input
			-161.06	-156.99	dBc/Hz	@1MHz, f_{in} = 125MHz, differential input
			-163.22	-160.84	dBc/Hz	@10MHz, f_{in} = 125MHz, differential input
			-163.38	-161.42	dBc/Hz	@20MHz, f_{in} = 125MHz, differential input
4	Phase Noise floor (VDD = 2.5V, VDDO = 2.5V)		-139.93	-134.59	dBc/Hz	@10kHz, fin = 125MHz, single ended input
			-147.22	-144.21	dBc/Hz	@100kHz, fin = 125MHz, single ended input
			-157.11	-154.78	dBc/Hz	@1MHz, fin = 125MHz, single ended input
			-160.58	-158.21	dBc/Hz	@10MHz, fin = 125MHz, single ended input
			-160.78	-158.19	dBc/Hz	@20MHz, fin = 125MHz, single ended input
			-141.69	-134.26	dBc/Hz	@10kHz, fin = 125MHz, differential input
			-149.19	-144.73	dBc/Hz	@100kHz, fin = 125MHz, differential input
			-158.66	-156.22	dBc/Hz	@1MHz, fin = 125MHz, differential input
			-161.60	-159.32	dBc/Hz	@10MHz, fin = 125MHz, differential input
			-161.85	-159.36	dBc/Hz	@20MHz, fin = 125MHz, differential input

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

(1)   System level additive jitter is calculated as $J_{RMS\_SYS\_AJ}$ = J_{RMS_OUT} - J_{RMS_IN}
(2)   Additive jitter is calculated as J_{RMS_AJ} = sqrt ($J_{RMS\_OUT}^2$ - $J_{RMS\_IN}^2$) where jitter is integrated in 12 kHz to 20 MHz band
(3)   Tester measures jitter at 156.25MHz. Since this freq won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed
        by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution.

Table 10 · LVCMOS Output Jitter Phase Noise with 25MHz XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		72.63		fs	VDD = 3.3V, VDDO = 3.3V
			87.59		fs	VDD = 2.5V; VDDO = 2.5V
2	Phase Noise floor		-75.96		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107.50		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-132.34		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-157.36		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-165.82		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-168.85		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-168.88		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-70.52		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-102.60		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-129.14		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-153.93		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-164.00		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-167.34		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-167.41		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Xtal frequency is 25 MHz

Table 11 · LVCMOS Output Jitter Phase Noise with 125MHz XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		48.70		fs	VDD = 3.3V, VDDO = 3.3V
			66.69		fs	VDD = 2.5V; VDDO = 2.5V
2	Phase Noise floor		-54.84		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-83.69		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-122.61		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-145.38		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-154.19		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-163.44		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-163.88		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-54.21		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-82.60		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-119.11		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-140.96		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-152.05		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-160.86		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-161.44		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Xtal frequency is 125 MHz

**Table 12 · AC Electrical Characteristics* - SPI (Serial Peripheral Interface) Timing**

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	sck period	tcyc	124			ns	See Figure 26& Figure 27
2	sck pulse width low	tclkl	62			ns	
3	sck pulse width high	tclkh	62			ns	
4	si setup (write) from sck rising edge	trxs	10			ns	
5	si hold (write) from sck rising edge	trxh	10			ns	
6	so delay (read) from sck falling edge	txd			25	ns	
7	cs_b to output high impedance	tohz			60	ns	
8	cs_b setup from sck falling edge (LSB first)	tcssi	20			ns	See Figure 26
9	cs_b hold from sck rising edge (LSB first)	tcshi	10			ns	
10	cs_b setup from sck rising edge (MSB first)	tcssm	20			ns	See Figure 27
11	cs_b hold from sck falling edge (MSB first)	tcshm	10			ns	

* Values are over Recommended Operating Conditions
* For LSB first mode timing diagram, refer to Figure 26
* For MSB first mode timing diagram, refer to Figure 27
* Values shown are proposed for the data sheet, these values are to be confirmed
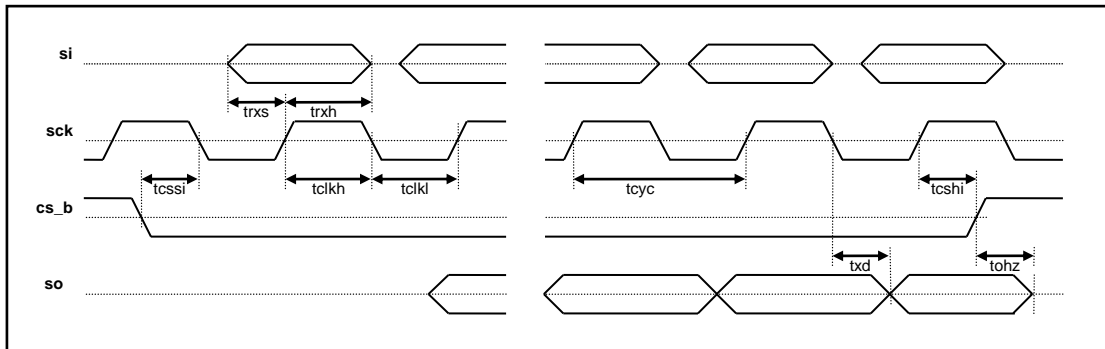
Figure 26.   SPI (Serial Peripheral Interface) Timing - LSB First Mode
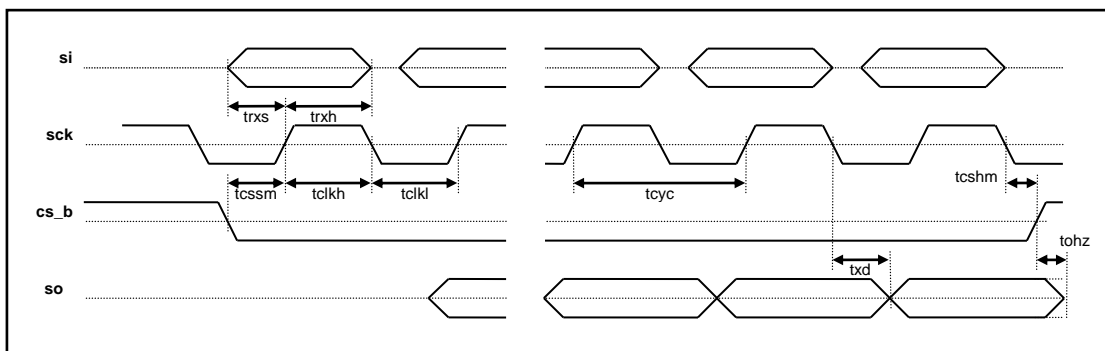
Figure 27.   SPI (Serial Peripheral Interface) Timing - MSB First Mode
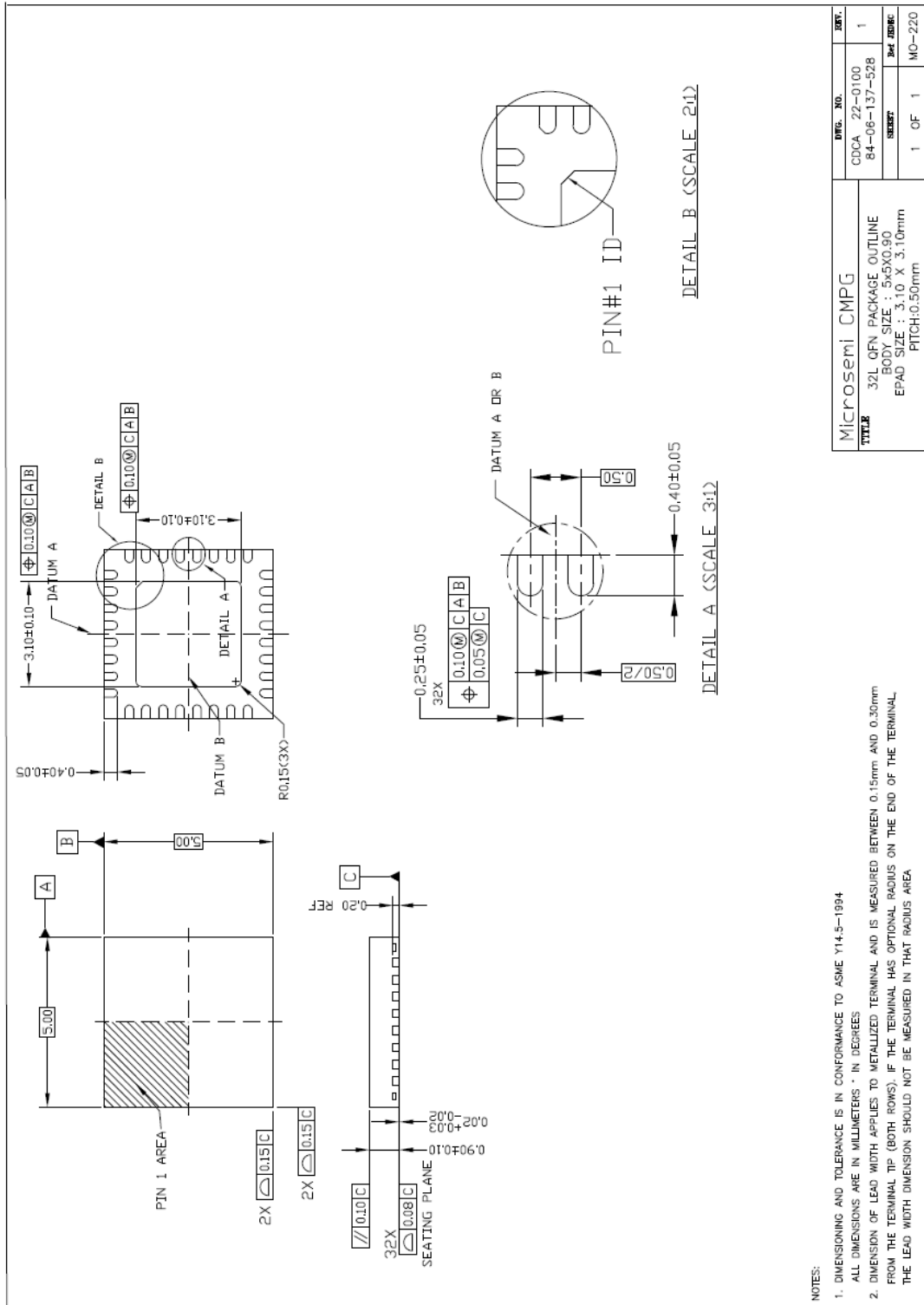
Table 13 · 5x5mm QFN Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance[1] (Note 1)	θ_{JA}	still air	26.8	°C/W
		1m/s airflow	21.8	
		2.5m/s airflow	19.9	
Junction to Board Thermal Resistance	θ_{JB}		10.8	°C/W
Junction to Case Thermal Resistance	θ_{JC}		19.5	°C/W
Junction to Pad Thermal Resistance[2]	θ_{JP}	Still air	6.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ_{JT}	Still air	0.6	°C/W

(1)   Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power

(2)   Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline

DETAIL B (SCALE 2:1)

PIN#1 ID

DETAIL A (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm
   FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL
   THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG

TITLE: 32L QFN PACKAGE OUTLINE
BODY SIZE : 5x5X0.90
EPAD SIZE : 3.10 X 3.10mm
PITCH:0.50mm

DWG. NO. CDCA 22-0100
84-06-137-528
REV. 1
SHEET 1 OF 1
Ref JEDEC MO-220
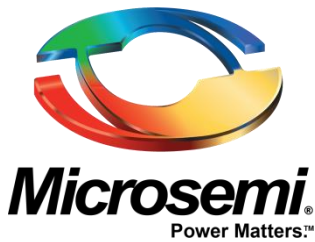
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