LMH6624 and LMH6626 Single/Dual Ultra Low Noise Wideband Operational Amplifier

1 Features

- V_S = ±6 V, T_A = 25°C, A_V = 20 (Typical Values Unless Specified)
- Gain Bandwidth (LMH6624) 1.5 GHz
- Input Voltage Noise 0.92 nV/√Hz
- Input Offset Voltage (limit over temp) 700 µV
- Slew Rate 350 V/µs
- Slew Rate (A_V = 10) 400 V/µs
- HD2 at f = 10 MHz, R_L = 100 Ω −63 dBc
- HD3 at f = 10 MHz, R_L = 100 Ω −80 dBc
- Supply Voltage Range (Dual Supply) 2.5 V to 6 V
- Supply Voltage Range (Single Supply) 5 V to 12 V
- Improved Replacement for the CLC425 (LMH6624)
- Stable for Closed Loop $|A_V| \geq 10$

2 Applications

- Instrumentation Sense Amplifiers
- Ultrasound Pre-amps
- Magnetic Tape & Disk Pre-amps
- Wide Band Active Filters
- Professional Audio Systems
- Opto-electronics
- Medical Diagnostic Systems

3 Description

The LMH6624 and LMH6626 devices offer wide bandwidth (1.5 GHz for single, 1.3 GHz for dual) with very low input noise (0.92 nV/√Hz, 2.3 pA/√Hz) and ultra-low dc errors (100 µV V_{OS}, ±0.1 µV/°C drift) providing very precise operational amplifiers with wide dynamic range. This enables the user to achieve closed-loop gains of greater than 10, in both inverting and non-inverting configurations.

The LMH6624 (single) and LMH6626 (dual) traditional voltage feedback topology provide the following benefits: balanced inputs, low offset voltage and offset current, very low offset drift, 81dB open loop gain, 95dB common mode rejection ratio, and 88dB power supply rejection ratio.

The LMH6624 and LMH6626 devices operate from ±2.5 V to ±6 V in dual supply mode and from 5 V to 12 V in single supply configuration.

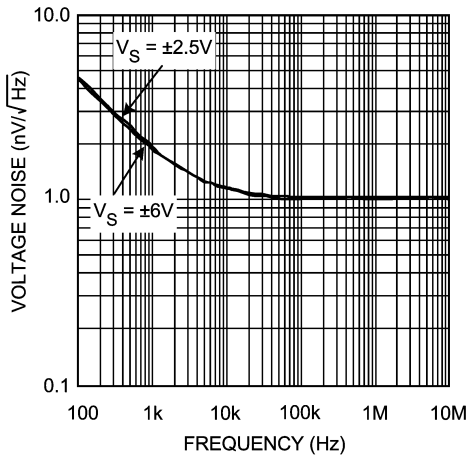
LMH6624 is offered in SOT-23-5 and SOIC-8 packages. The LMH6626 is offered in SOIC-8 and VSSOP-8 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6624	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
LMH6626	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Voltage Noise vs. Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G — **Page**

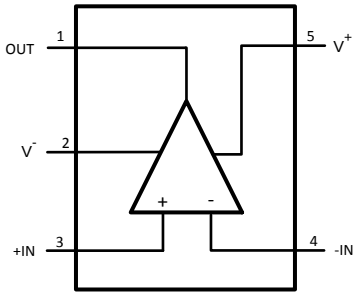
- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Added Input Current parameter in Absolute Maximum Ratings ... 4
- Added Operating supply voltage (V+ - V-) parameter in Recommended Operating Conditions ... 4
- Revised paragraph beginning with "As seen in ..." in *Total Input Noise vs. Source Resistance* ... 19
- Changed from 33.5 Ω to 26 Ω in *Total Input Noise vs. Source Resistance* ... 19
- Changed from 6.43 kΩ to 3.1 kΩ in *Total Input Noise vs. Source Resistance* ... 19

Changes from Revision E (March 2013) to Revision F — **Page**

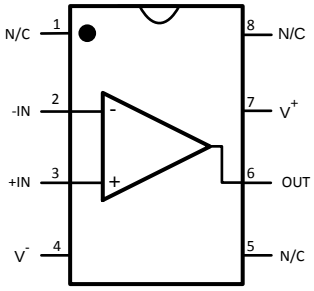
- Changed layout of National Data Sheet to TI format ... 1
- Changed from 464 Ω to 283 Ω ... 19

5 Pin Configuration and Functions

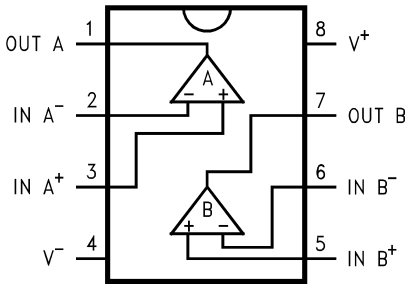
5-Pin SOT-23 (LMH6624)
Package DBV
Top View



8-Pin SOIC (LMH6624)
Package D
Top View



8-Pin SOIC Package D and VSSOP (LMH6626)
Package D or DGK
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NUMBER				
	LMH6624		LMH6626		
	DBV	D	DGK or D		
-IN	4	2	–	I	Inverting Input
+IN	3	3	–	I	Non-inverting Input
IN A-	–	–	2	I	Inverting Input Channel A
IN B-	–	–	6	I	Inverting Input Channel B
IN A+	–	–	3	I	Non-inverting Input Channel A
IN B+	–	–	5	I	Non-inverting Input Channel B
N/C	–	1, 5, 8	–	—	No Connection
OUT	1	6	–	O	Output
OUT A	–	–	1	O	Output Channel A
OUT B	–	–	7	O	Output Channel B
V-	2	4	4	I	Negative Supply
V+	5	7	8	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} Differential			±1.2	V
Supply voltage (V^+ - V^-)			13.2	V
Voltage at Input pins			V^+ +0.5, V^- −0.5	V
Input Current			±10	mA
Soldering information	Infrared or convection (20 sec.)		235	°C
	Wave soldering (10 sec.)		260	°C
Junction temperature(2)			150	°C
Storage temperature		-65	150	°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model(2)	±200	

(1) Human body model, 1.5 kΩ in series with 100 pF. JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) Machine Model, 0 Ω in series with 200 pF. JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Operating temperature(2)	−40	+125	°C
Operating supply voltage (V+ - V-)	±2.25	±6.3	V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.4 Thermal Information

THERMAL METRIC(1)		LMH6624		LMH6626		UNIT
		DBV	D	DGK	D	
		5 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	265	166	235	166	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 Electrical Characteristics ±2.5 V

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 2.5 V, V^- = −2.5 V, V_{CM} = 0 V, A_V = +20, R_F = 500 Ω, R_L = 100 Ω. See (1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
DYNAMIC PERFORMANCE							
f_{CL}	−3dB BW	V_O = 400 mV_{PP} (LMH6624)			90		MHz
		V_O = 400 mV_{PP} (LMH6626)			80		
SR	Slew rate(4)	V_O = 2 V_{PP}, A_V = +20 (LMH6624)			300		V/µs
		V_O = 2 V_{PP}, A_V = +20 (LMH6626)			290		
		V_O = 2 V_{PP}, A_V = +10 (LMH6624)			360		
		V_O = 2 V_{PP}, A_V = +10 (LMH6626)			340		
t_r	Rise time	V_O = 400 mV Step, 10% to 90%			4.1		ns
t_f	Fall time	V_O = 400 mV Step, 10% to 90%			4.1		ns
t_s	Settling time 0.1%	V_O = 2 V_{PP} (Step)			20		ns
DISTORTION and NOISE RESPONSE							
e_n	Input referred voltage noise	f = 1 MHz (LMH6624)			0.92		nV/√Hz
		f = 1 MHz (LMH6626)			1.0		
i_n	Input referred current noise	f = 1 MHz (LMH6624)			2.3		pA/√Hz
		f = 1 MHz (LMH6626)			1.8		
HD2	2nd harmonic distortion	f_C = 10 MHz, V_O = 1 V_{PP}, R_L 100 Ω			−60		dBc
HD3	3rd harmonic distortion	f_C = 10 MHz, V_O = 1 V_{PP}, R_L 100 Ω			−76		dBc
INPUT CHARACTERISTICS							
V_{OS}	Input offset voltage	V_{CM} = 0 V		−0.75	−0.25	+0.75	mV
			-40°C ≤ T_J ≤ 125°C	−0.95		+0.95	
	Average drift(5)	V_{CM} = 0 V			±0.25		µV/°C
I_{OS}	Input offset current	V_{CM} = 0 V		−1.5	−0.05	+1.5	µA
			-40°C ≤ T_J ≤ 125°C	−2.0		+2.0	
	Average drift(5)	V_{CM} = 0 V			2		nA/°C
I_B	Input bias current	V_{CM} = 0 V			13	+20	µA
			-40°C ≤ T_J ≤ 125°C			+25	
	Average drift(5)	V_{CM} = 0 V			12		nA/°C
R_{IN}	Input resistance(6)	Common Mode			6.6		MΩ
		Differential Mode			4.6		kΩ
C_{IN}	Input capacitance(6)	Common Mode			0.9		pF
		Differential Mode			2.0		
CMRR	Common mode rejection ratio	Input Referred, V_{CM} = −0.5 to +1.9 V		87	90		dB
		Input Referred, V_{CM} = −0.5 to +1.75 V	-40°C ≤ T_J ≤ 125°C	85			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the slowest of the rising and falling slew rates.
(5) Average drift is determined by dividing the change in parameter at temperature extremes into the total temperature change.
(6) Simulation results.

Electrical Characteristics ±2.5 V (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 2.5 V, V^- = −2.5 V, V_{CM} = 0 V, A_V = +20, R_F = 500 Ω, R_L = 100 Ω. See (1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
TRANSFER CHARACTERISTICS							
A_{VOL}	Large signal voltage gain	(LMH6624) R_L = 100 Ω, V_O = −1 V to +1 V		75	79		dB
			-40°C ≤ T_J ≤ 125°C	70			
		(LMH6626) R_L = 100 Ω, V_O = −1 V to +1 V		72	79		
			-40°C ≤ T_J ≤ 125°C	67			
X_t	Crosstalk rejection	f = 1 MHz (LMH6626)			−75		dB
OUTPUT CHARACTERISTICS							
V_O	Output swing	R_L = 100 Ω		±1.1	±1.5		V
			-40°C ≤ T_J ≤ 125°C	±1.0			
		No Load		±1.4	±1.7		
			-40°C ≤ T_J ≤ 125°C	±1.25			
R_O	Output impedance	f ≤ 100 KHz			10		mΩ
I_{SC}	Output short circuit current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200 mV (7)(8)		90	145		mA
			-40°C ≤ T_J ≤ 125°C	75			
		(LMH6624) Sinking to Ground ΔV_{IN} = −200 mV (7)(8)		90	145		
			-40°C ≤ T_J ≤ 125°C	75			
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200 mV (7)(8)		60	120		
			-40°C ≤ T_J ≤ 125°C	50			
		(LMH6626) Sinking to Ground ΔV_{IN} = −200 mV (7)(8)		60	120		
			-40°C ≤ T_J ≤ 125°C	50			
I_{OUT}	Output current	(LMH6624) Sourcing, V_O = +0.8 V Sinking, V_O = −0.8 V			100		mA
		(LMH6626) Sourcing, V_O = +0.8 V Sinking, V_O = −0.8 V			75		
POWER SUPPLY							
PSRR	Power supply rejection ratio	V_S = ±2.0 V to ±3.0 V		82	90		dB
			-40°C ≤ T_J ≤ 125°C	80			
I_S	Supply current (per channel)	No Load			11.4	16	mA
			-40°C ≤ T_J ≤ 125°C			18	

(7) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(8) Short circuit test is a momentary test. Output short circuit duration is 1.5 ms.

6.6 Electrical Characteristics ±6 V

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 6 V, V^- = −6 V, V_{CM} = 0 V, A_V = +20, R_F = 500 Ω, R_L = 100 Ω. See (1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
DYNAMIC PERFORMANCE							
f_{CL}	−3dB BW	V_O = 400 mV_{PP} (LMH6624)			95		MHz
		V_O = 400 mV_{PP} (LMH6626)			85		
SR	Slew rate(4)	V_O = 2 V_{PP}, A_V = +20 (LMH6624)			350		V/µs
		V_O = 2 V_{PP}, A_V = +20 (LMH6626)			320		
		V_O = 2 V_{PP}, A_V = +10 (LMH6624)			400		
		V_O = 2 V_{PP}, A_V = +10 (LMH6626)			360		
t_r	Rise time	V_O = 400 mV Step, 10% to 90%			3.7		ns
t_f	Fall time	V_O = 400 mV Step, 10% to 90%			3.7		ns
t_s	Settling time 0.1%	V_O = 2 V_{PP} (Step)			18		ns
DISTORTION and NOISE RESPONSE							
e_n	Input referred voltage noise	f = 1 MHz (LMH6624)			0.92		nV/√Hz
		f = 1 MHz (LMH6626)			1.0		
i_n	Input referred current noise	f = 1 MHz (LMH6624)			2.3		pA/√Hz
		f = 1 MHz (LMH6626)			1.8		
HD2	2nd harmonic distortion	f_C = 10 MHz, V_O = 1 V_{PP}, R_L = 100 Ω			−63		dBc
HD3	3rd harmonic distortion	f_C = 10 MHz, V_O = 1 V_{PP}, R_L = 100 Ω			−80		dBc
INPUT CHARACTERISTICS							
V_{OS}	Input offset voltage	V_{CM} = 0 V		−0.5	±0.10	+0.5	mV
			-40°C ≤ T_J ≤ 125°C	−0.7		+0.7	
	Average drift(5)	V_{CM} = 0 V			±0.2		µV/°C
I_{OS}	Input offset current	(LMH6624) V_{CM} = 0 V		−1.1	0.05	1.1	µA
			-40°C ≤ T_J ≤ 125°C	−2.5		2.5	
		(LMH6626) V_{CM} = 0 V		−2.0	0.1	2.0	
			-40°C ≤ T_J ≤ 125°C	−2.5		2.5	
	Average drift(5)	V_{CM} = 0 V			0.7		nA/°C
I_B	Input bias current	V_{CM} = 0 V			13	+20	µA
			-40°C ≤ T_J ≤ 125°C			+25	
	Average drift(5)	V_{CM} = 0 V			12		nA/°C
R_{IN}	Input resistance(6)	Common Mode			6.6		MΩ
		Differential Mode			4.6		kΩ
C_{IN}	Input capacitance(6)	Common Mode			0.9		pF
		Differential Mode			2.0		
CMRR	Common mode rejection ratio	Input Referred, V_{CM} = −4.5 to +5.25 V		90	95		dB
		Input Referred, V_{CM} = −4.5 to +5.0 V	-40°C ≤ T_J ≤ 125°C	87			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the slowest of the rising and falling slew rates.
(5) Average drift is determined by dividing the change in parameter at temperature extremes into the total temperature change.
(6) Simulation results.

Electrical Characteristics ±6 V (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 6 V, V^- = −6 V, V_{CM} = 0 V, A_V = +20, R_F = 500 Ω, R_L = 100 Ω. See (1).

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
TRANSFER CHARACTERISTICS							
A_{VOL}	Large signal voltage gain	(LMH6624) R_L = 100 Ω, V_O = −3 V to +3 V		77	81		dB
			-40°C ≤ T_J ≤ 125°C	72			
		(LMH6626) R_L = 100 Ω, V_O = −3 V to +3 V		74	80		
			-40°C ≤ T_J ≤ 125°C	70			
X_t	Crosstalk rejection	f = 1MHz (LMH6626)			−75		dB
OUTPUT CHARACTERISTICS							
V_O	Output swing	(LMH6624) R_L = 100 Ω		±4.4	±4.9		V
			-40°C ≤ T_J ≤ 125°C	±4.3			
		(LMH6624) No Load		±4.8	±5.2		
			-40°C ≤ T_J ≤ 125°C	±4.65			
		(LMH6626) R_L = 100 Ω		±4.3	±4.8		
			-40°C ≤ T_J ≤ 125°C	±4.2			
		(LMH6626) No Load		±4.8	±5.2		
			-40°C ≤ T_J ≤ 125°C	±4.65			
R_O	Output impedance	f ≤ 100 KHz			10		mΩ
I_{SC}	Output short circuit current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200 mV (7)(8)		100	156		mA
			-40°C ≤ T_J ≤ 125°C	85			
		(LMH6624) Sinking to Ground ΔV_{IN} = −200 mV (7)(8)		100	156		
			-40°C ≤ T_J ≤ 125°C	85			
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200 mV (7)(8)		65	120		
			-40°C ≤ T_J ≤ 125°C	55			
		(LMH6626) Sinking to Ground ΔV_{IN} = −200 mV (7)(8)		65	120		
			-40°C ≤ T_J ≤ 125°C	55			
I_{OUT}	Output current	(LMH6624) Sourcing, V_O = +4.3 V Sinking, V_O = −4.3 V			100		mA
		(LMH6626) Sourcing, V_O = +4.3 V Sinking, V_O = −4.3 V			80		
POWER SUPPLY							
PSRR	Power supply rejection ratio	V_S = ±5.4 V to ±6.6 V		82	88		dB
			-40°C ≤ T_J ≤ 125°C	80			
I_S	Supply current (per channel)	No Load			12	16	mA
			-40°C ≤ T_J ≤ 125°C			18	

(7) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(8) Short circuit test is a momentary test. Output short circuit duration is 1.5 ms.

6.7 Typical Characteristics

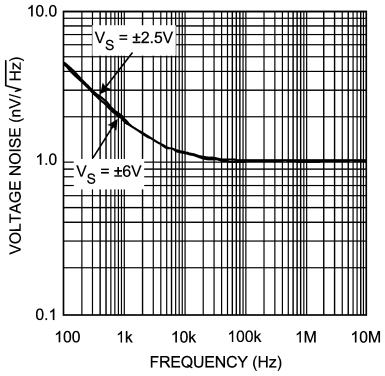


Figure 1. Voltage Noise vs. Frequency

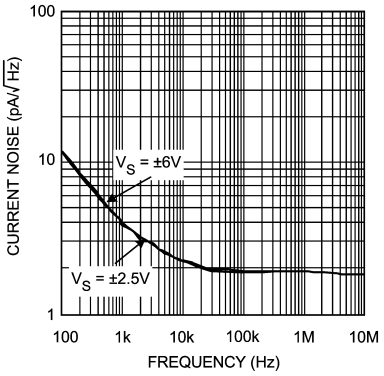
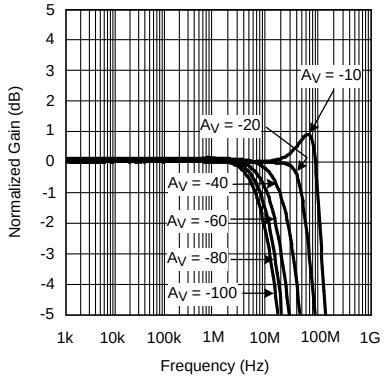
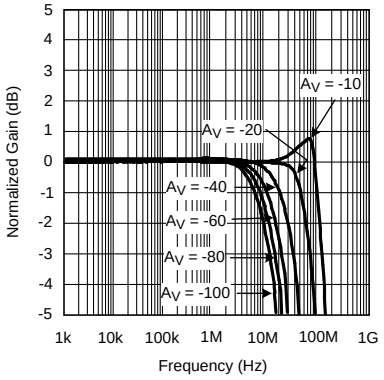


Figure 2. Current Noise vs. Frequency



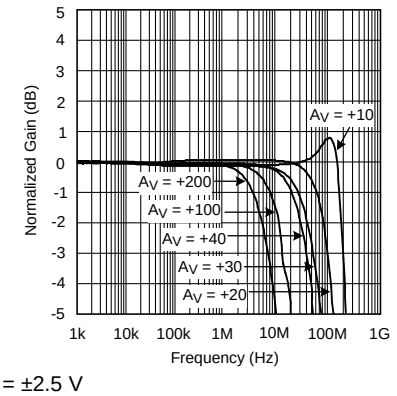
V_S = ±2.5 V
V_{IN} = 5 mVpp
R_L = 100 Ω

Figure 3. Inverting Frequency Response



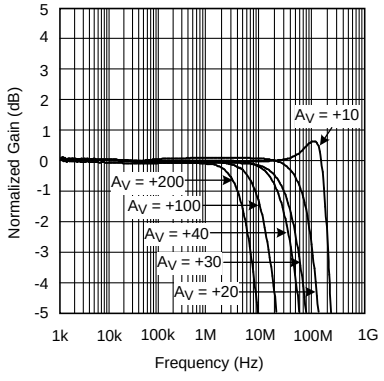
V_S = ±6V
V_{IN} = 5 mVpp
R_L = 100 Ω

Figure 4. Inverting Frequency Response



V_S = ±2.5 V
R_F = 500 Ω
V_O = 2 Vpp

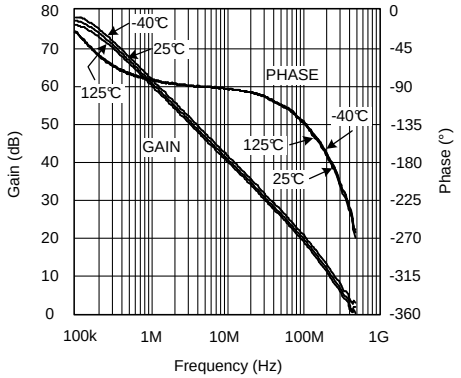
Figure 5. Non-Inverting Frequency Response



V_S = ±6 V
R_F = 500 Ω
V_O = 2 Vpp

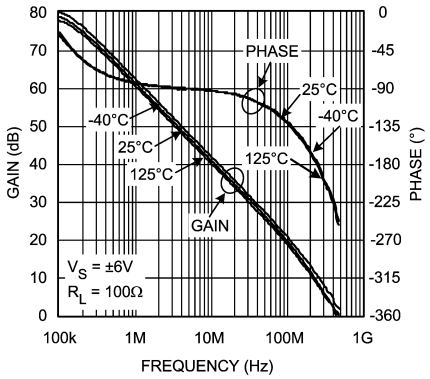
Figure 6. Non-Inverting Frequency Response

Typical Characteristics (continued)



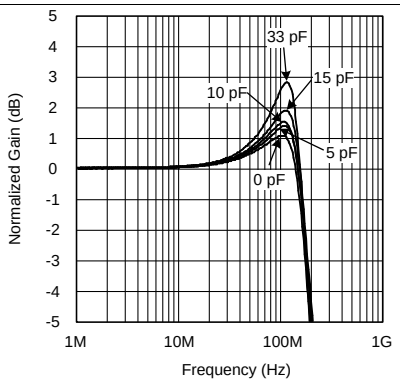
V_S = ±2.5 V

Figure 7. Open Loop Frequency Response Over Temperature



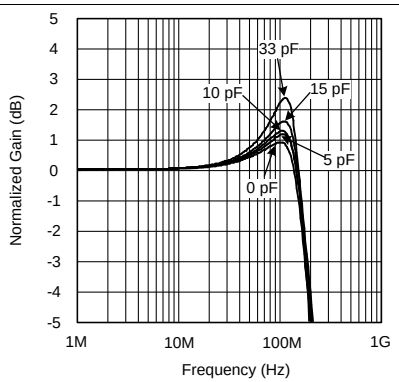
V_S = ±6V
R_L = 100 Ω

Figure 8. Open Loop Frequency Response Over Temperature



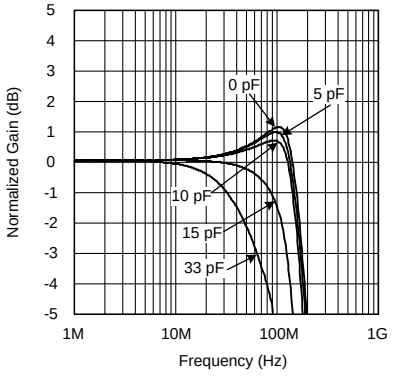
V_S = ±2.5V
A_V = +10
R_F = 250 Ω
R_{ISO} = 10 Ω
R_L = 1 kΩ||C_L

Figure 9. Frequency Response with Cap. Loading



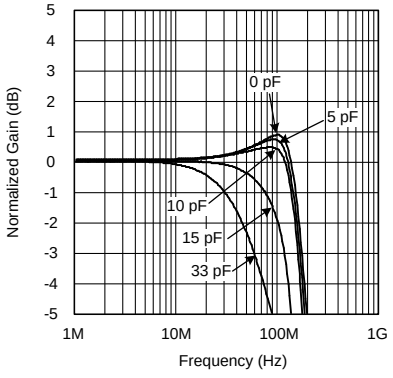
V_S = ±6V
A_V = +10
R_F = 250 Ω
R_{ISO} = 10 Ω
R_L = 1 kΩ||C_L

Figure 10. Frequency Response with Cap. Loading



V_S = ±2.5 V
A_V = +10
R_F = 250 Ω
R_{ISO} = 100 Ω
R_L = 1 kΩ||C_L

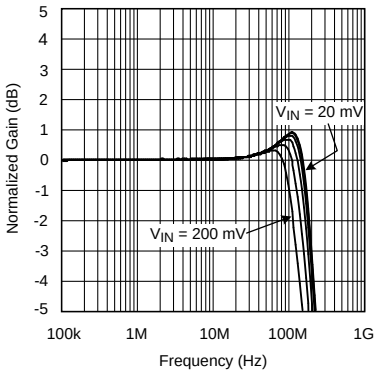
Figure 11. Frequency Response with Cap. Loading



V_S = ±6 V
A_V = +10
R_F = 250 Ω
R_{ISO} = 10 Ω
R_L = 1 kΩ||C_L

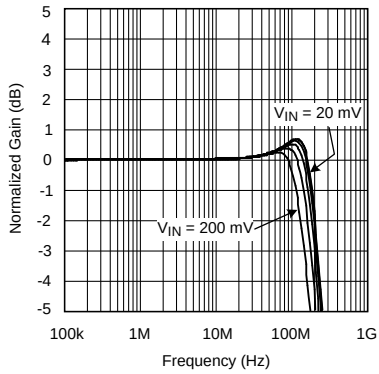
Figure 12. Frequency Response with Cap. Loading

Typical Characteristics (continued)



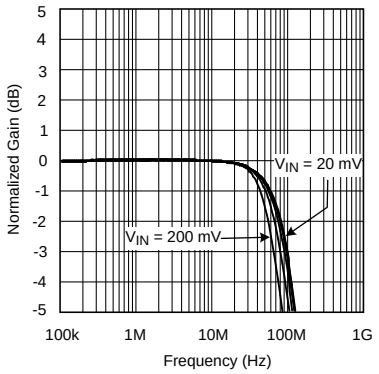
V_S = ±-2.5 V
A_V = +10
R_F = 500 Ω

Figure 13. Non-Inverting Frequency Response Varying V_{IN}



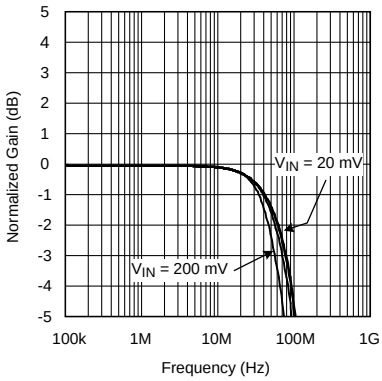
V_S = ±6 V
A_V = +10
R_F = 500 Ω

Figure 14. Non-Inverting Frequency Response Varying V_{IN}



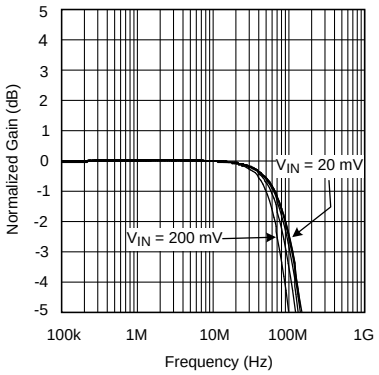
V_S = ±2.5 V
A_V = +20
R_F = 500 Ω

Figure 15. Non-Inverting Frequency Response Varying V_{IN} (LMH6624)



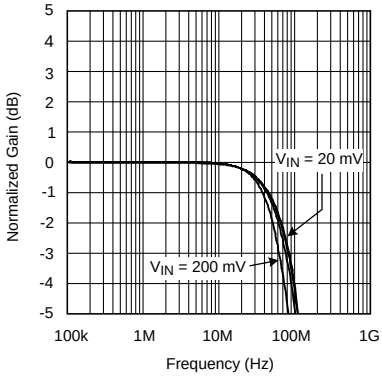
V_S = ±2.5 V
A_V = +20
R_F = 500 Ω

Figure 16. Non-Inverting Frequency Response Varying V_{IN} (LMH6626)



V_S = ±6 V
A_V = +20
R_F = 500 Ω

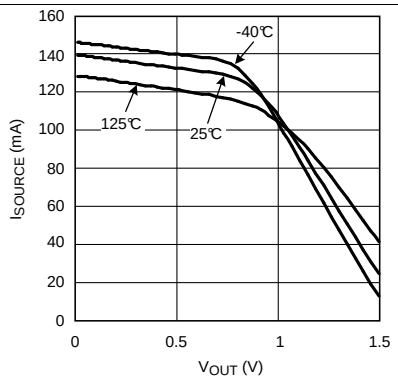
Figure 17. Non-Inverting Frequency Response Varying V_{IN} (LMH6624)



V_S = ±6 V
A_V = +20
R_F = 500 Ω

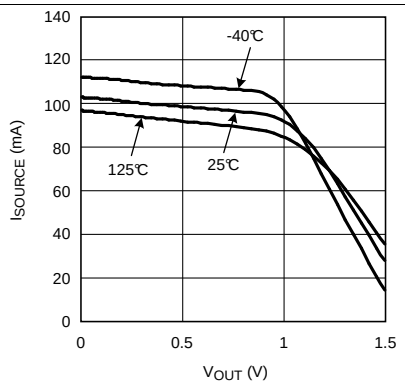
Figure 18. Non-Inverting Frequency Response Varying V_{IN} (LMH6626)

Typical Characteristics (continued)



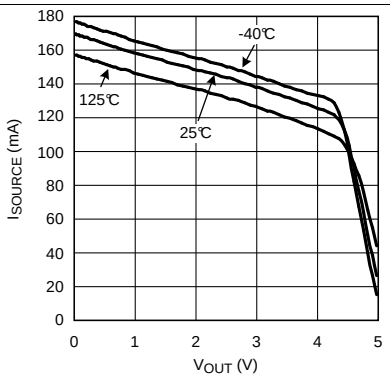
V_S = ±2.5 V

Figure 19. Sourcing Current vs. V_{OUT} (LMH6624)



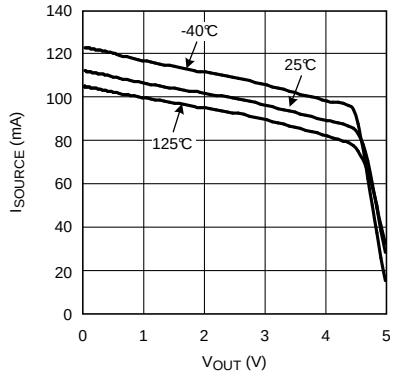
V_S = ±2.5 V

Figure 20. Sourcing Current vs. V_{OUT} (LMH6626)



V_S = ±6 V

Figure 21. Sourcing Current vs. V_{OUT} (LMH6624)



V_S = ±6 V

Figure 22. Sourcing Current vs. V_{OUT} (LMH6626)

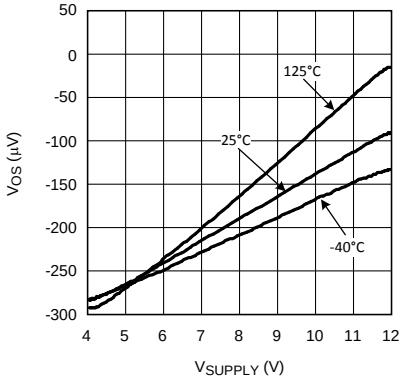


Figure 23. V_{OS} vs. V_{SUPPLY} (LMH6624)

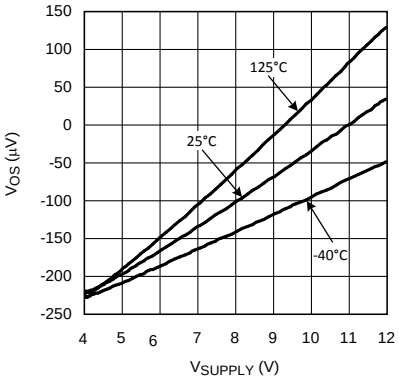
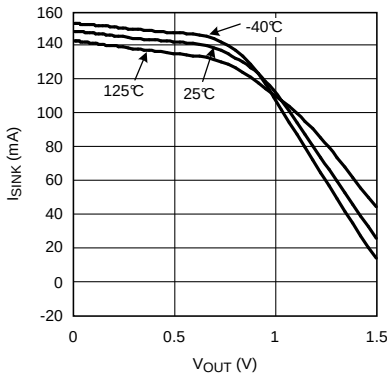


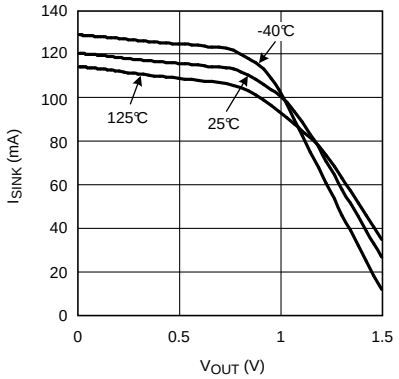
Figure 24. V_{OS} vs. V_{SUPPLY} (LMH6626)

Typical Characteristics (continued)



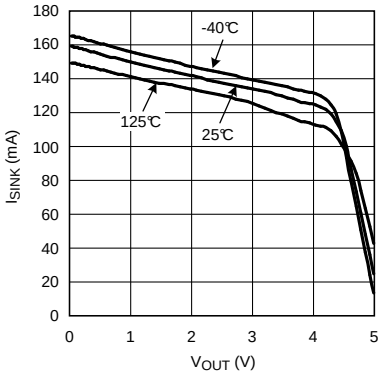
V_S = ±2.5 V

Figure 25. Sinking Current vs. V_{OUT} (LMH6624)



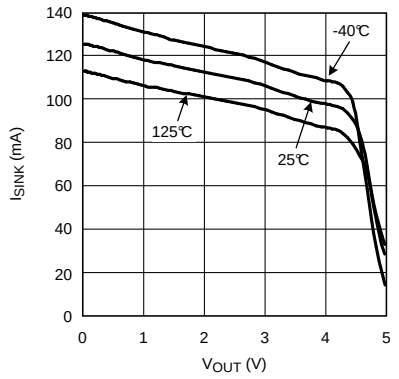
V_S = ±2.5V

Figure 26. Sinking Current vs. V_{OUT} (LMH6626)



V_S = ±6 V

Figure 27. Sinking Current vs. V_{OUT} (LMH6624)



V_S = ±6 V

Figure 28. Sinking Current vs. V_{OUT} (LMH6626)

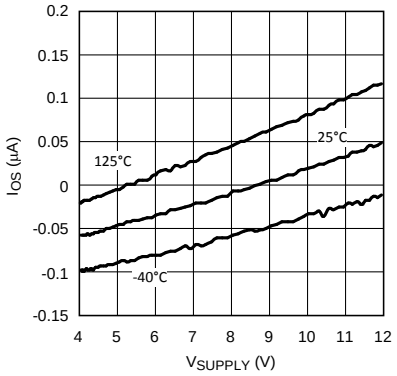
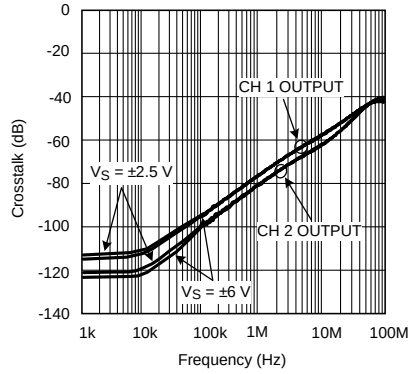


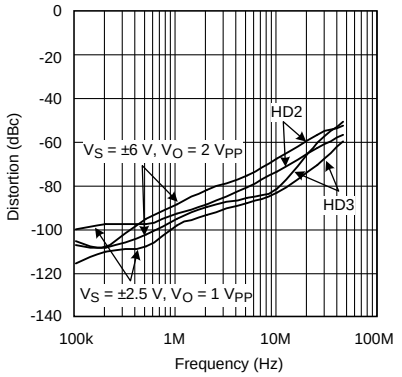
Figure 29. I_{OS} vs. V_{SUPPLY}



V_{IN} = 60 mVpp
A_V = +20
R_L = 100 Ω

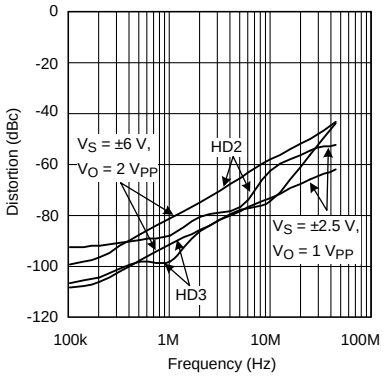
Figure 30. Crosstalk Rejection vs. Frequency (LMH6626)

Typical Characteristics (continued)



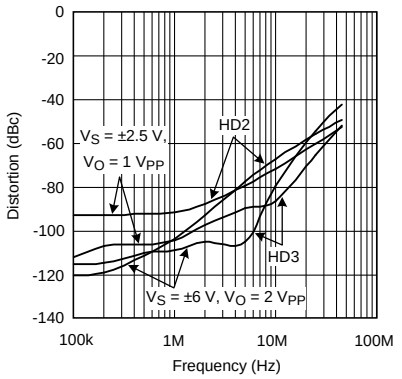
A_V = +10
R_L = 100 Ω

Figure 31. Distortion vs. Frequency



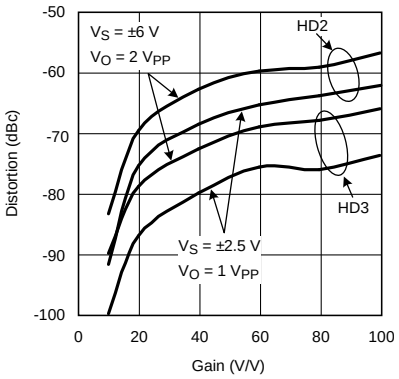
A_V = +20
R_L = 100 Ω

Figure 32. Distortion vs. Frequency



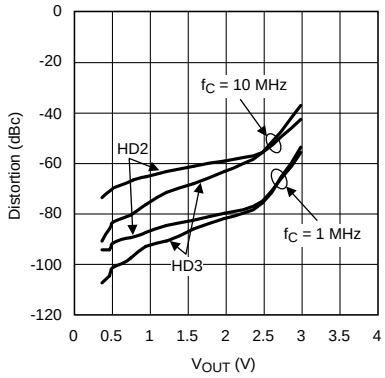
A_V = +20
R_L = 500 Ω

Figure 33. Distortion vs. Frequency



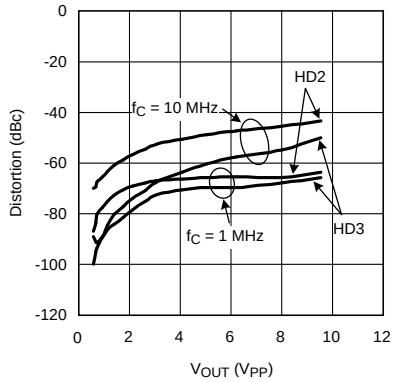
V_S = ±6 V
V_O = 2 Vpp

Figure 34. Distortion vs. Gain



A_V = +20
A_V = ±2.5V
R_L = 100 Ω

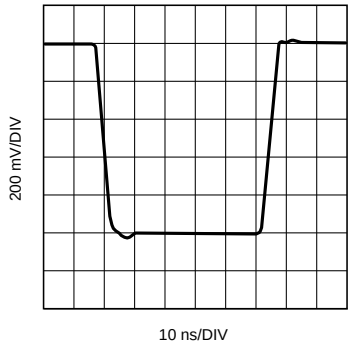
Figure 35. Distortion vs. V_{OUT} Peak to Peak



A_V = +20
V_S = ±6 V
R_L = 100 Ω

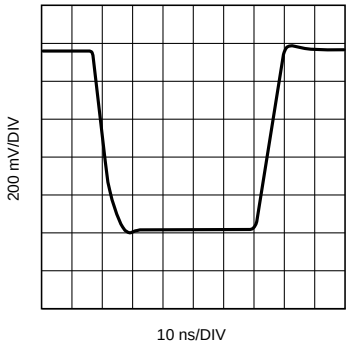
Figure 36. Distortion vs. V_{OUT} Peak to Peak

Typical Characteristics (continued)



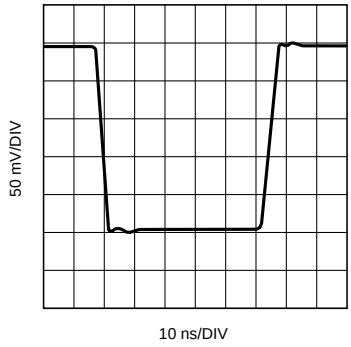
V_S = ±2.5 V
V_O = 1 Vpp
A_V = +10
R_L = 100 Ω

Figure 37. Non-Inverting Large Signal Pulse Response



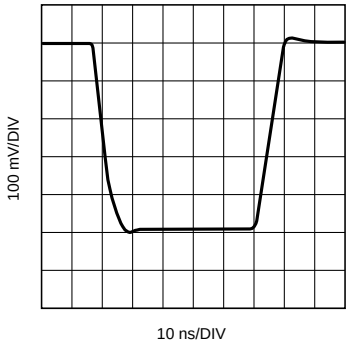
V_S = ±6 V
V_O = 1 Vpp
A_V = +20
R_L = 100 Ω

Figure 38. Non-Inverting Large Signal Pulse Response



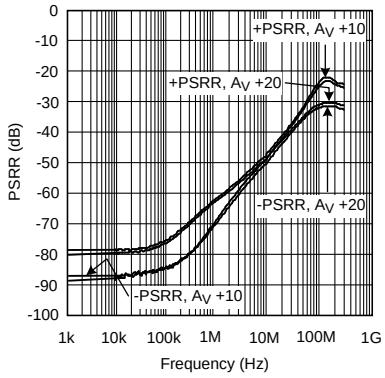
V_S = ±2.5 V
V_O = 200 mv
A_V = +10
R_L = 100 Ω

Figure 39. Non-Inverting Small Signal Pulse Response



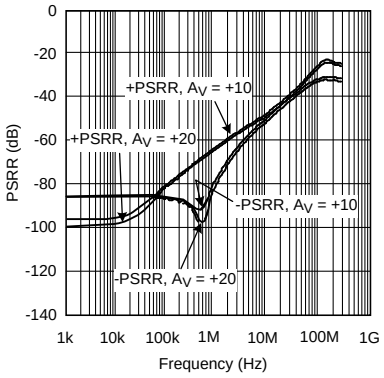
V_S = ±6 V
V_O = 500 mv
A_V = +20
R_L = 100 Ω

Figure 40. Non-Inverting Small Signal Pulse Response



V_S = ±2.5 V

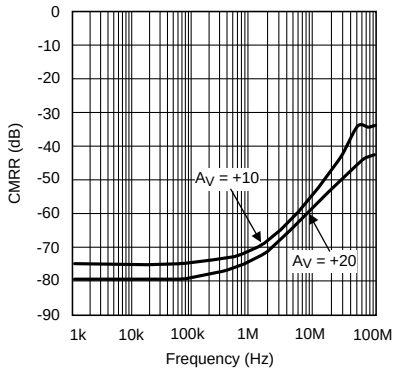
Figure 41. PSRR vs. Frequency



V_S = ±6 V

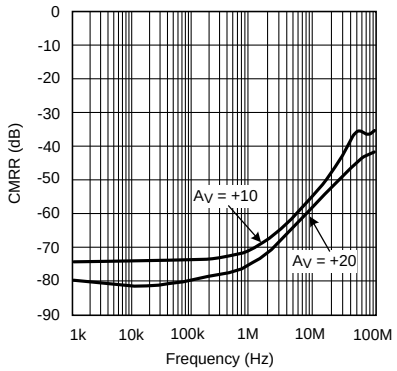
Figure 42. PSRR vs. Frequency

Typical Characteristics (continued)



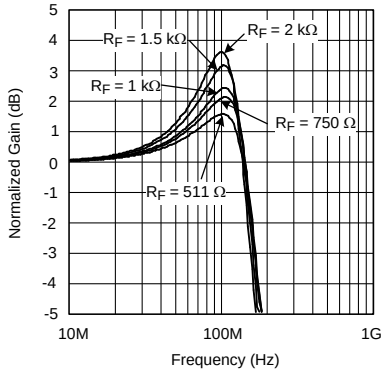
V_S = ±2.5V
V_{IN} = 5 mVpp

Figure 43. Input Referred CMRR vs. Frequency



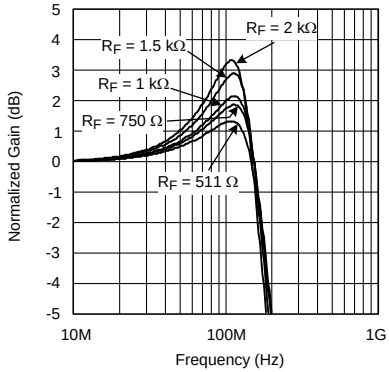
V_S = ±6 V
V_{IN} = 5 mVpp

Figure 44. Input Referred CMRR vs. Frequency



V_S = ±2.5 V
A_V = +10
R_L = 100 Ω

Figure 45. Amplifier Peaking with Varying R_F



V_S = ±6 V
A_V = +10 V
R_L = 100 Ω

Figure 46. Amplifier Peaking with Varying R_F

7 Detailed Description

7.1 Overview

The LMH6624 and LMH6626 devices are very wide gain bandwidth, ultra low noise voltage feedback operational amplifiers. Their excellent performances enable applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high frequency signal-to-noise ratios. The set of characteristic plots in *Typical Characteristics* illustrates many of the performance trade-offs. The following discussion will demonstrate the proper selection of external components to achieve optimum system performance.

7.2 Feature Description

7.2.1 Bias Current Cancellation

To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 47. Combining this constraint with the non-inverting gain equation also seen in Figure 47, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \quad (1)$$

$$R_g = R_f/(A_V-1) \quad (2)$$

When driven from a 0-Ω source, such as the output of an op amp, the non-inverting input of the LMH6624 and LMH6626 should be isolated with at least a 25-Ω series resistor.

As seen in Figure 48, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f||(R_g+R_s)$). R_b should to be no less than 25 Ω for optimum LMH6624 and LMH6626 performance. A shunt capacitor can minimize the additional noise of R_b.

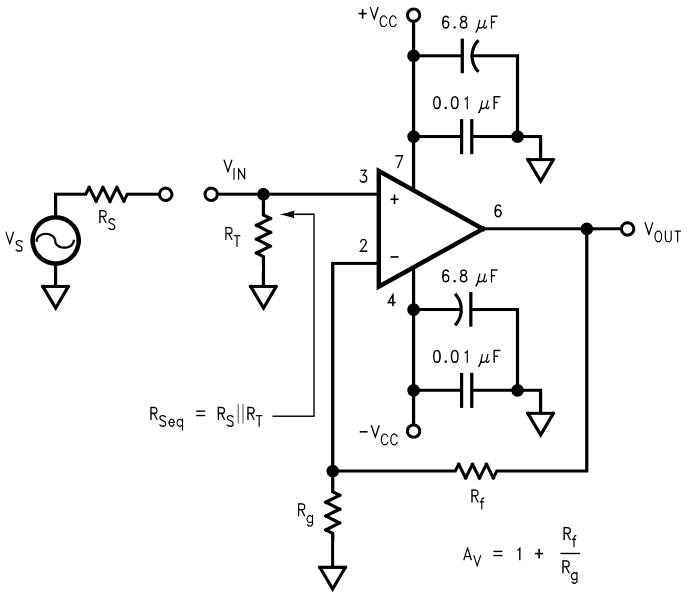


Figure 47. Non-Inverting Amplifier Configuration

Feature Description (continued)

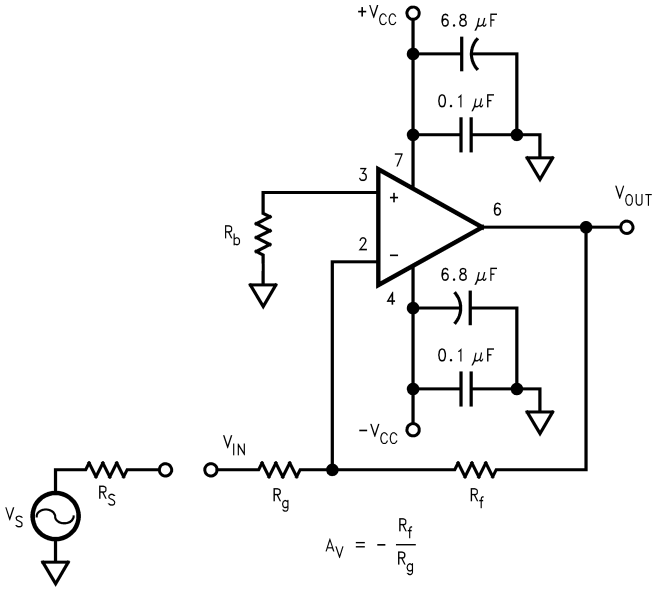


Figure 48. Inverting Amplifier Configuration

7.2.2 Total Input Noise vs. Source Resistance

To determine maximum signal-to-noise ratios from the LMH6624 and LMH6626, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 49 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors. Equation 3 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 4 is a simplification of Equation 3 that assumes $R_f||R_g = R_{seq}$ for bias current cancellation. Figure 50 illustrates the equivalent noise model using this assumption. Figure 51 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise sources of Equation 4. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_V$.

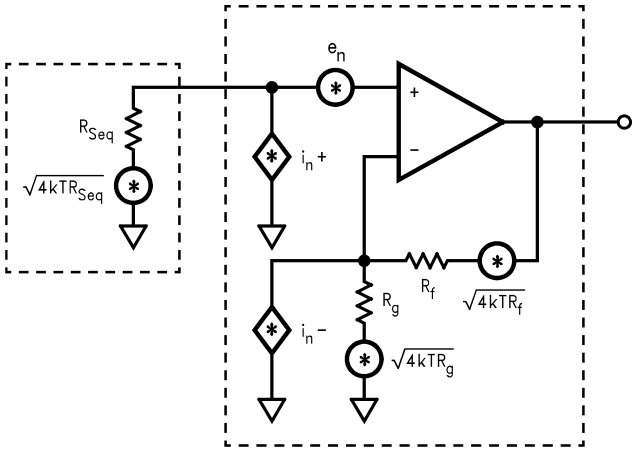


Figure 49. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f||R_g\right)\right)^2 + 4kT\left(R_f||R_g\right)} \quad (3)$$

Feature Description (continued)

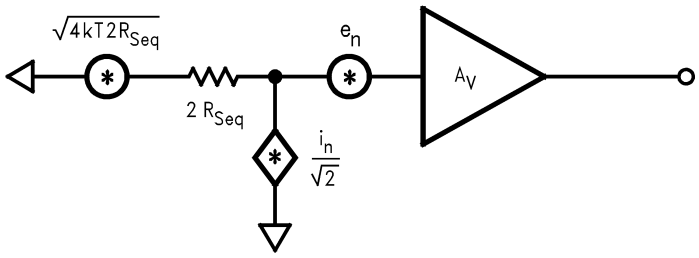


Figure 50. Noise Model with $R_f||R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})} \quad (4)$$

As seen in Figure 51, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 26 Ω. Between 26 Ω and 3.1 kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$ of the equivalent source resistance R_{seq}. Above 3.1 kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{2}\, i_n R_{seq}$). When R_{seq} = 283 Ω (that is, $R_{seq} = e_n/\sqrt{2}\ i_n$) the contribution from voltage noise and current noise of LMH6624 and LMH6626 is equal. For example, configured with a gain of +20V/V giving a −3 dB of 90 MHz and driven from $R_{seq} = Rf \,||\, Rg = 25\ \Omega$ (e_{ni} = 1.3 nV√Hz from Figure 51), the LMH6624 produces a total output noise voltage (e_{ni} × 20 V/V × √(1.57 × 90 MHz)) of 309 µVrms.

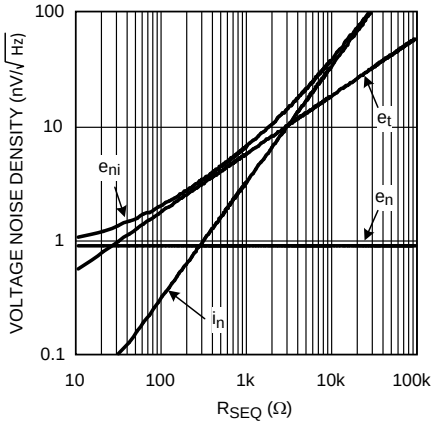


Figure 51. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f \,||\, R_g$ need not equal R_{seq}. In this case, according to Equation 3, $R_f \,||\, R_g$ should be as low as possible to minimize noise. Results similar to Equation 3 are obtained for the inverting configuration of Figure 48 if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, Equation 3 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Feature Description (continued)

7.2.3 Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\} \quad (5)$$

The Noise Figure formula is shown in Equation 5. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10\ LOG\left[\frac{e_n^2 + i_n^2 (R_{Seq}^2 + (R_f||R_g)^2) + 4KT\ (R_{Seq} + (R_f||R_g))}{4KT\ (R_{Seq} + (R_f||R_g))}\right] \quad (6)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize "Noise Figure":

- Minimize R_f || R_g
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx \frac{e_n}{i_n} \quad (7)$$

7.2.4 Low Noise Integrator

The LMH6624 and LMH6626 devices implement a deBoo integrator shown in Figure 52. Positive feedback maintains integration linearity. The low input offset voltage of the LMH6624 and LMH6626 devices and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN}\ \frac{K_O}{sR_SC}\ ;\ K_O = 1 + \frac{R_F}{R_G}$$

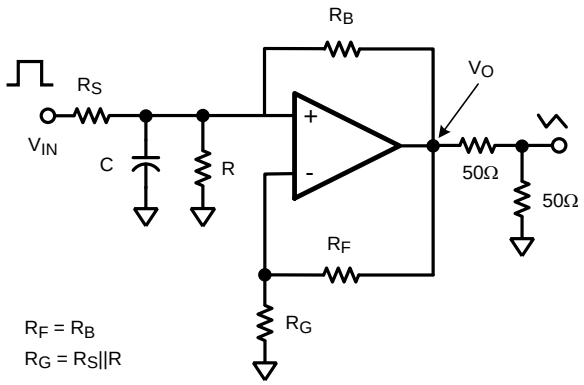


Figure 52. Low Noise Integrator

Feature Description (continued)

7.2.5 High-gain Sallen-key Active Filters

The LMH6624 and LMH6626 devices are well suited for high gain Sallen-Key type of active filters. Figure 53 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods discussed in Application Note OA-21, *Component Pre-Distortion for Sallen Key Filters* (SNOA369) will enable the proper selection of components for these high-frequency filters.

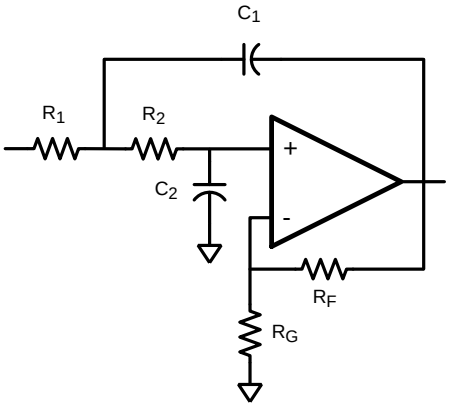
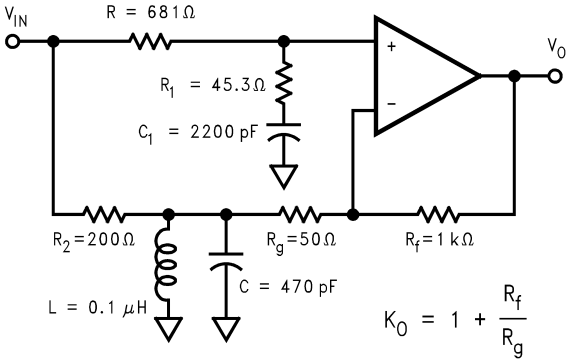


Figure 53. Sallen-Key Active Filter Topology

7.2.6 Low Noise Magnetic Media Equalizer

The LMH6624 and LMH6626 devices implement a high-performance low noise equalizer for such application as magnetic tape channels as shown in Figure 54. The circuit combines an integrator with a bandpass filter to produce the low noise equalization. The circuit's simulated frequency response is illustrated in Figure 55.



$$\frac{V_O}{V_{IN}} = K_O \left(\frac{sC_1 R_1 + 1}{sC_1 (R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2 LCR_2 R_g + sL(R_2 + R_g) + R_2 R_g} \right)$$

Figure 54. Low Noise Magnetic Media Equalizer

Feature Description (continued)

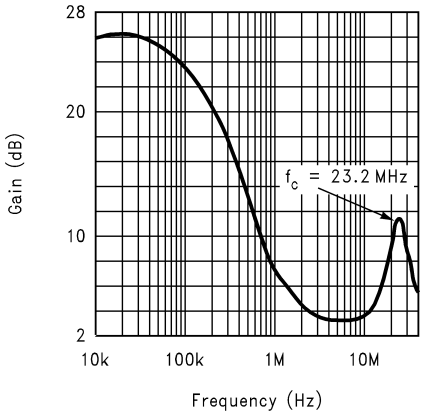


Figure 55. Equalizer Frequency Response

7.3 Device Functional Modes

7.3.1 Single Supply Operation

The LMH6624 and LMH6626 devices can be operated with single power supply as shown in Figure 56. Both the input and output are capacitively coupled to set the DC operating point.

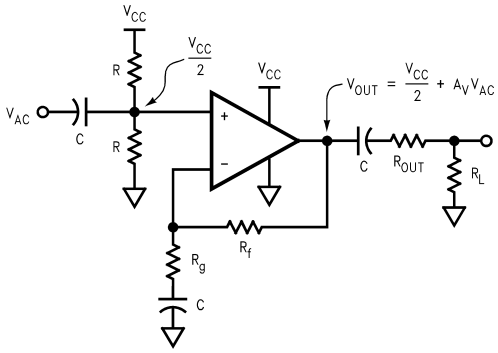


Figure 56. Single Supply Operation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A Transimpedance amplifier is used to convert the small output current of a photodiode to a voltage, while maintaining a near constant voltage across the photodiode to minimize non-linearity. Extracting the small signal requires high gain and a low noise amplifier, and therefore, the LMH6624 and LMH6626 devices are ideal for such an application in order to maximize SNR. Furthermore, because of the large gain (R_F value) needed, the device used must be high speed so that even with high noise gain (due to the interaction of the feedback resistor and photodiode capacitance), bandwidth is not heavily impacted.

Figure 47 implements a high-speed, single supply, low-noise Transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_F.

8.2 Typical Application

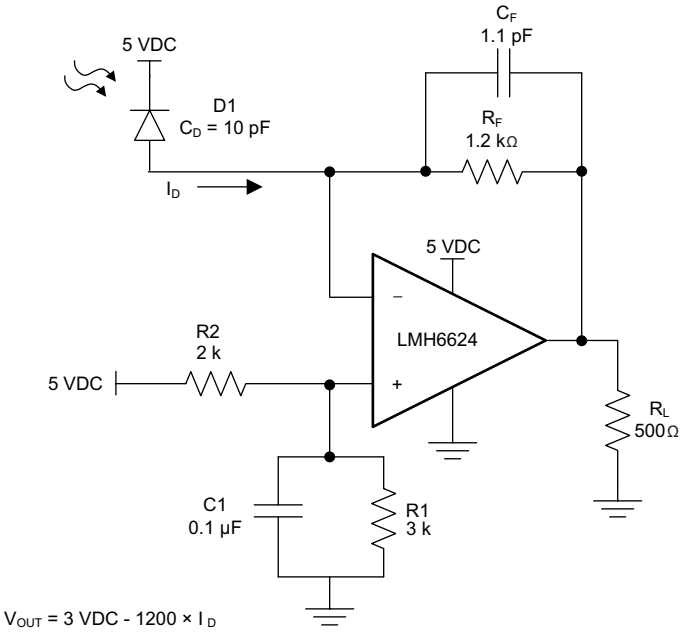


Figure 57. LMH6624 Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Figure 58 shows the Noise Gain (NG) and transfer function (I-V Gain). As with most Transimpedance amplifiers, it is required to compensate for the additional phase lag (Noise Gain zero at f_Z) created by the total input capacitance: C_D (diode capacitance) + C_{CM} (LMH6624 CM input capacitance) + C_{DIFF} (LMH6624 DIFF input capacitance) looking into R_F. This is accomplished by placing C_F across R_F to create enough phase lead (Noise Gain pole at f_P) to stabilize the loop.

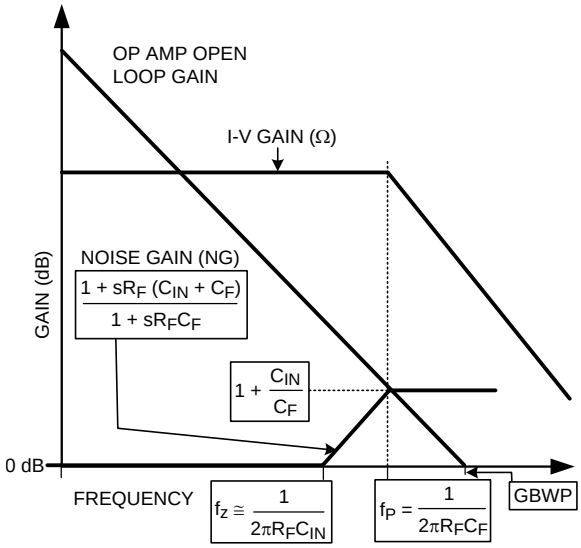


Figure 58. Transimpedance Amplifier Noise Gain and Transfer Function

8.2.2 Detailed Design Procedure

The optimum value of C_F is given by Equation 8 resulting in the I-V -3dB bandwidth shown in Equation 9, or around 124 MHz in this case, assuming GBWP = 1.5 GHz, C_{CM} (LMH6624 CM input capacitance) = 0.9 pF, and C_{DIFF} (LMH6624 DIFF input capacitance) = 2 pF. This C_F value is a "starting point" and C_F needs to be tuned for the particular application as it is often less than 1 pF and thus is easily affected by board parasitics.

Optimum C_F Value:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}} \tag{8}$$

Resulting -3dB Bandwidth:

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}} \tag{9}$$

Equation 10 provides the total input current noise density (i_{ni}) equation for the basic Transimpedance configuration and is plotted against feedback resistance (R_F) showing all contributing noise sources in Figure 59. The plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_F). This is depicted in the schematic of Figure 60 where total equivalent current noise density (i_{ni}) is shown at the input of a noiseless amplifier and noiseless feedback resistor (R_F). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_F. Noise Equation for Transimpedance Amplifier:

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}} \tag{10}$$

Typical Application (continued)

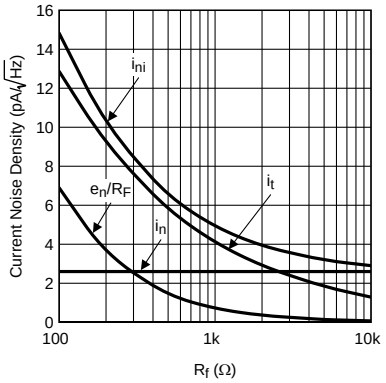


Figure 59. Current Noise Density vs. Feedback Resistance

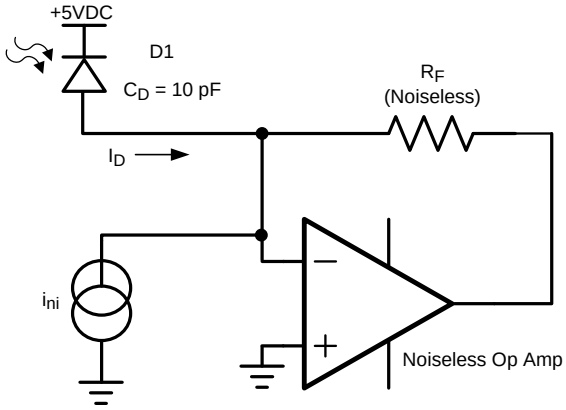


Figure 60. Transimpedance Amplifier Equivalent Input Source Mode

From Figure 61, it is clear that with the LMH6624 extremely low-noise characteristics, for R_F < 3 kΩ, the noise performance is entirely dominated by R_F thermal noise. Only above this R_F threshold, the input noise current (i_n) of LMH6624 becomes a factor and at no R_F setting does the LMH6624 input noise voltage play a significant role. This noise analysis has ignored the possible noise gain increase, due to photo-diode capacitance, at higher frequencies.

8.2.3 Application Curve

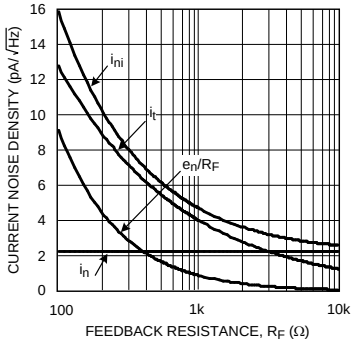


Figure 61. Current Noise Density vs. Feedback Resistance

9 Power Supply Recommendations

The LMH6624 and LMH6626 devices can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

10 Layout

10.1 Layout Guidelines

TI suggests the copper patterns on the evaluation boards shown in Figure 62 and Figure 63 as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins as shown in Figure 62. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations. See Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* (SNOA367) for more information. Use high quality chip capacitors with values in the range of 1000 pF to 0.1 µF for power supply bypassing as shown in Figure 62. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7 µF and 10 µF in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect as shown in Figure 63. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high speed and high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6624MF	SOT-23–5	LMH730216
LMH6624MA	SOIC-8	LMH730227
LMH6626MA	SOIC-8	LMH730036
LMH6626MM	VSSOP-8	LMH730123

10.2 Layout Example

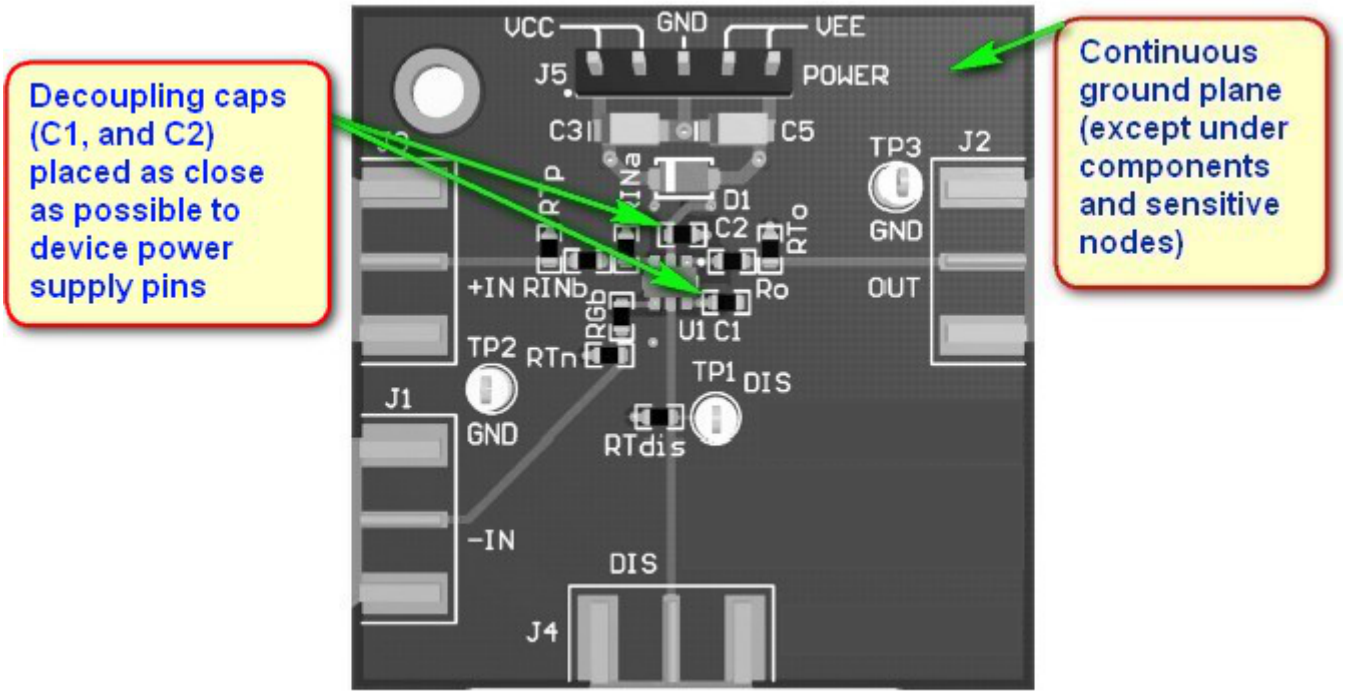


Figure 62. LMH6624 and LMH6626 EVM Board Layout Example

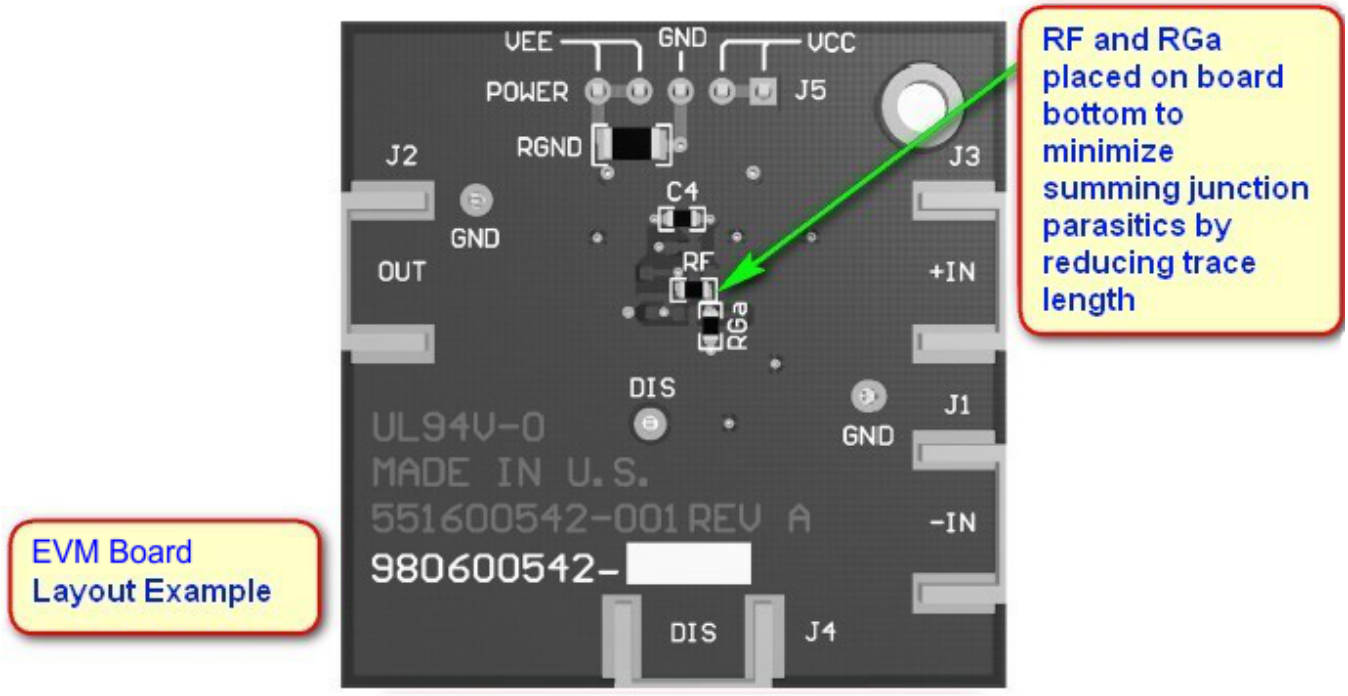


Figure 63. LMH6624 and LMH6626 EVM Board Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, Application Note OA-15 (SNOA367)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6624	Click here	Click here	Click here	Click here	Click here
LMH6626	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6624MA	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 125	LMH66 24MA	
LMH6624MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 24MA	Samples
LMH6624MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 24MA	Samples
LMH6624MF	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	A94A	
LMH6624MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A94A	Samples
LMH6624MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A94A	Samples
LMH6626MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 26MA	Samples
LMH6626MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 26MA	Samples
LMH6626MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A98A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

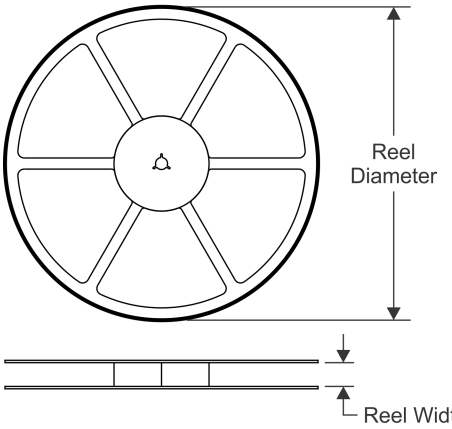
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

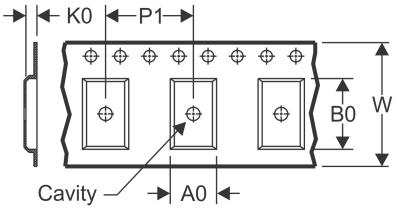
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

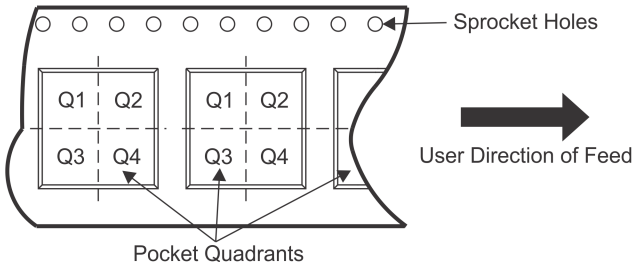


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

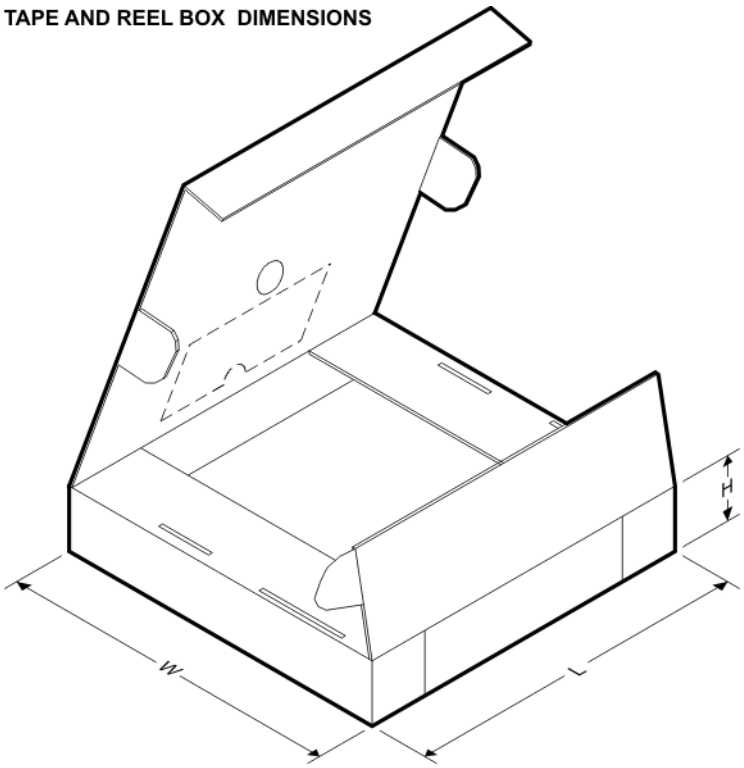
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6624MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6624MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6624MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6624MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6626MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6626MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

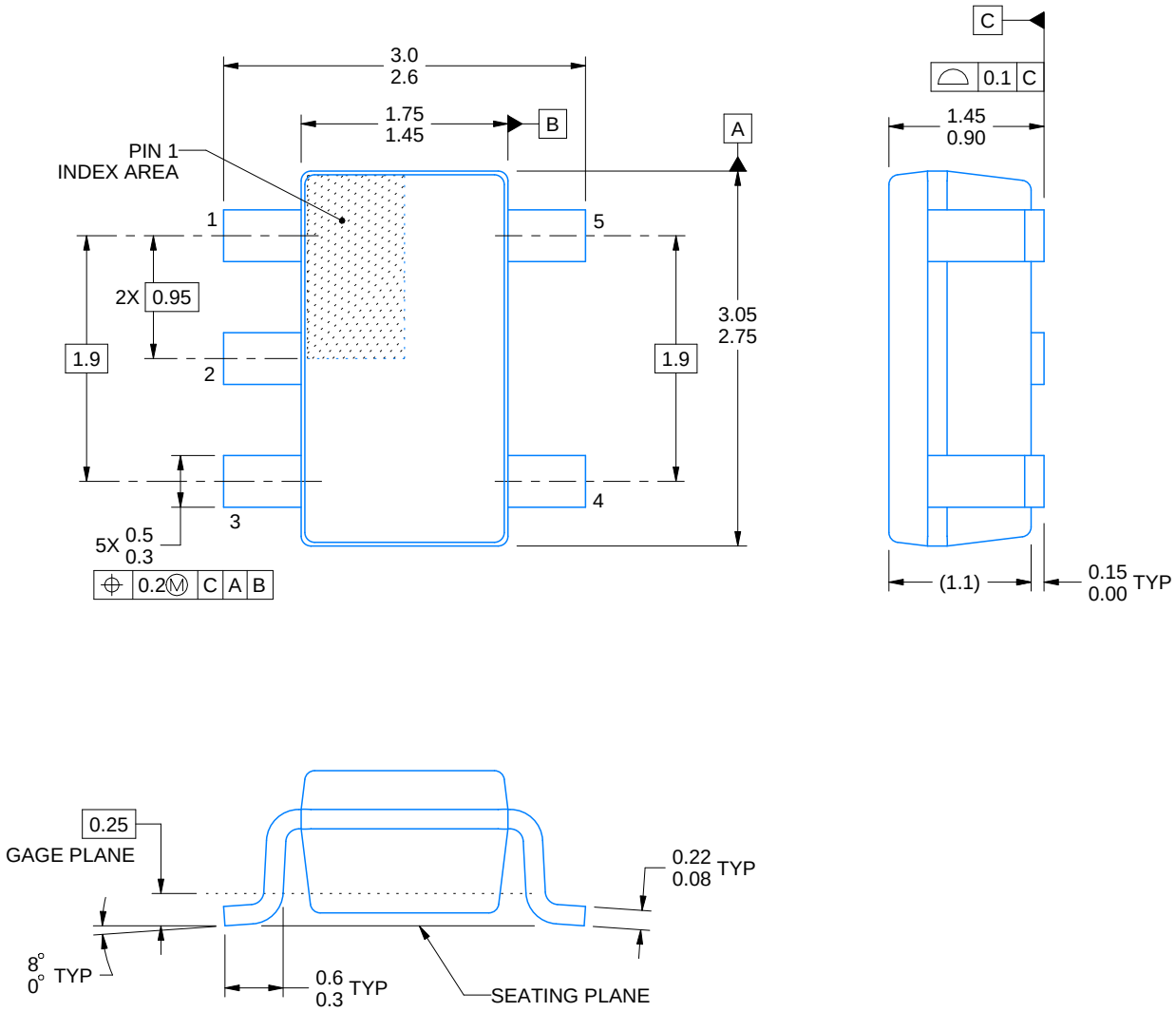
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6624MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6624MF	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6624MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6624MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6626MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6626MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

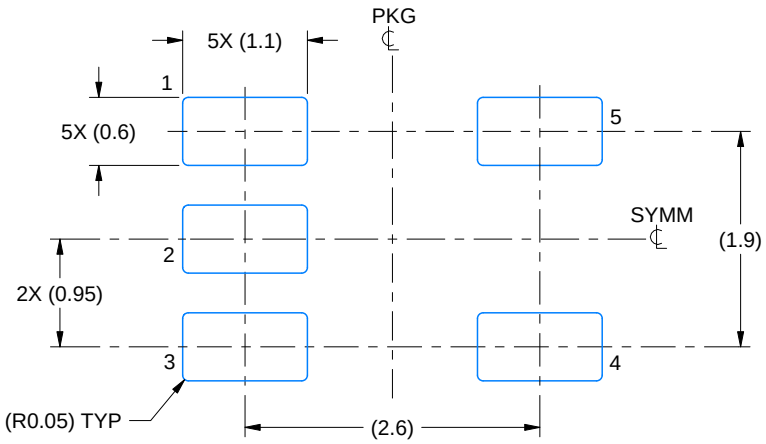
SMALL OUTLINE TRANSISTOR



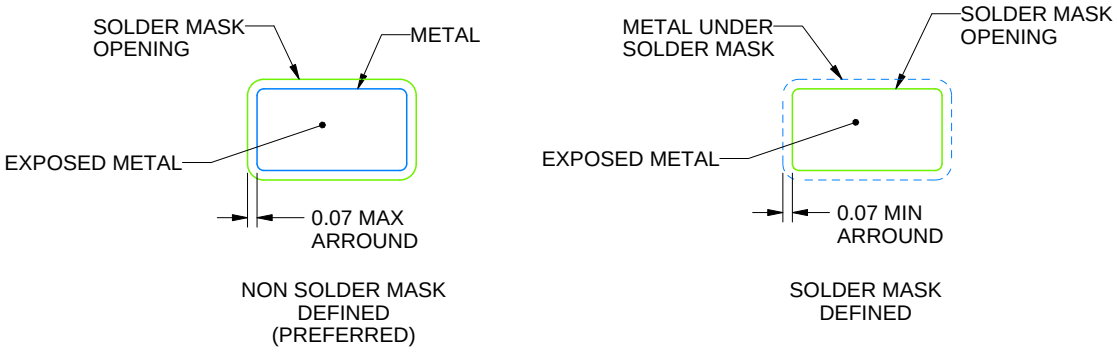
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

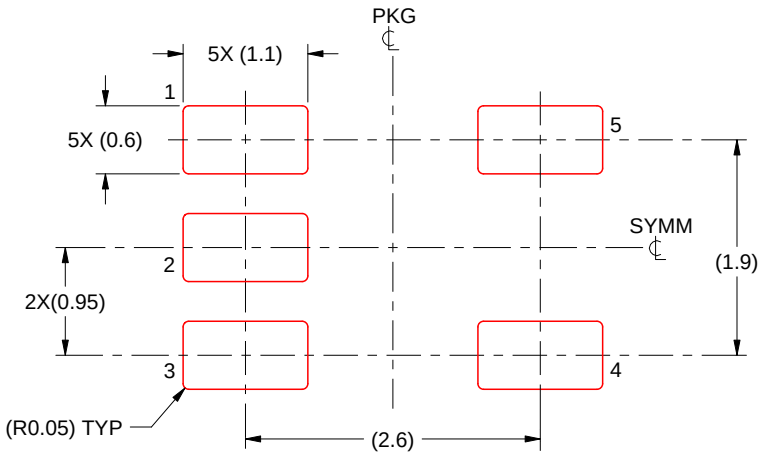


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

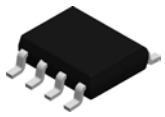


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

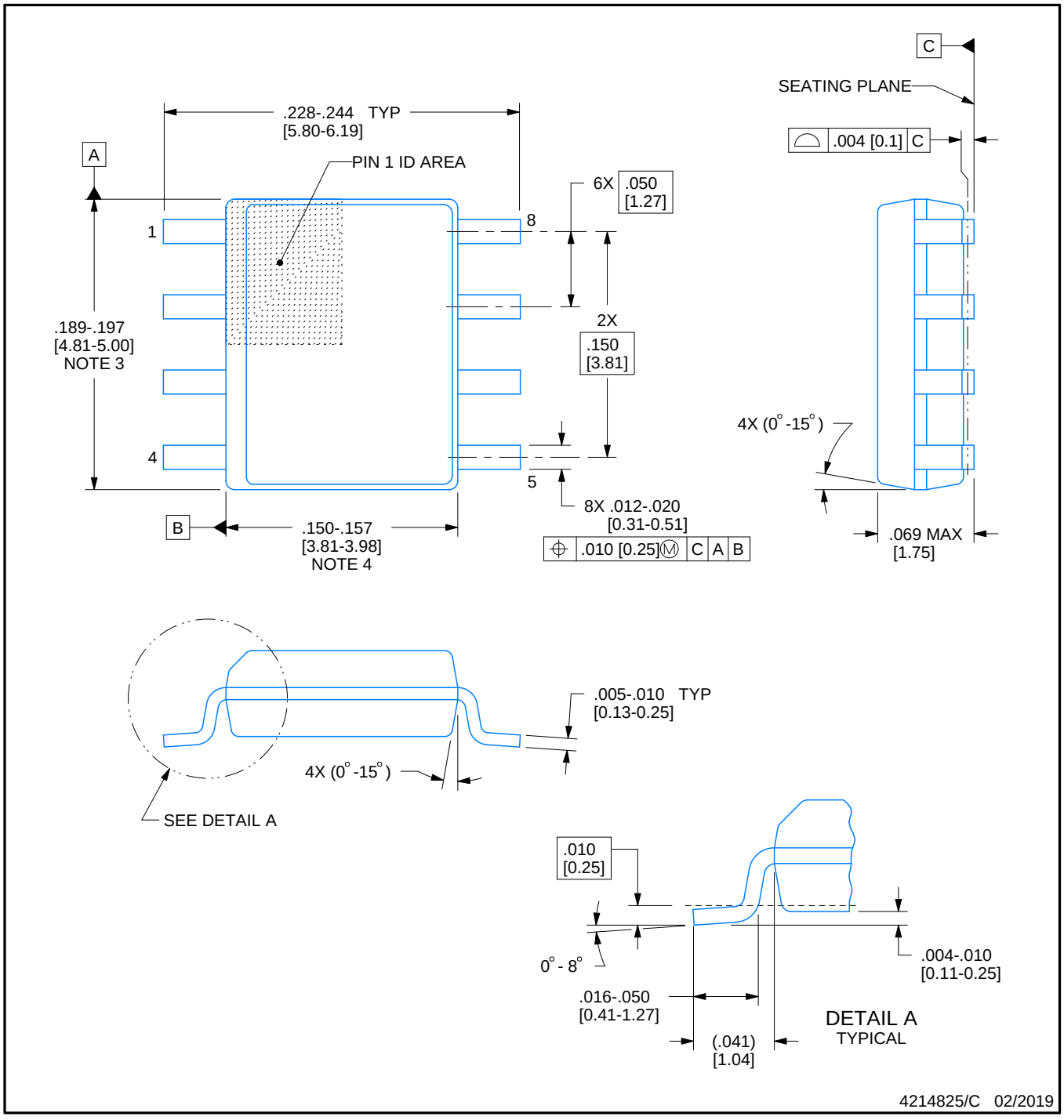


PACKAGE OUTLINE

D0008A

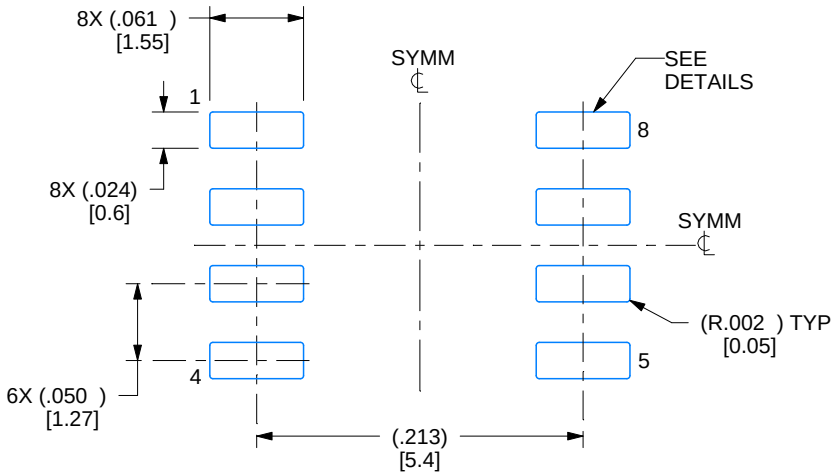
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

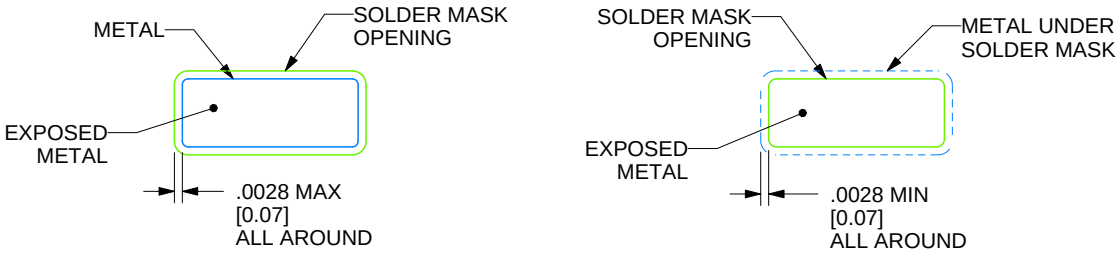


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

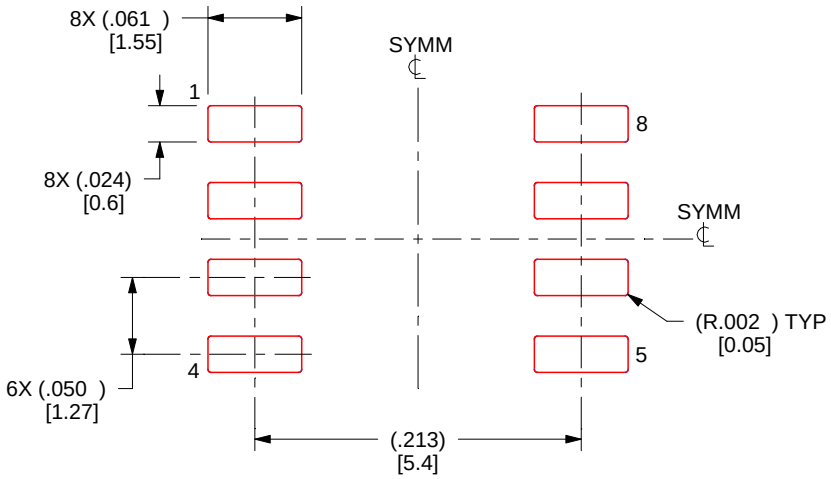
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



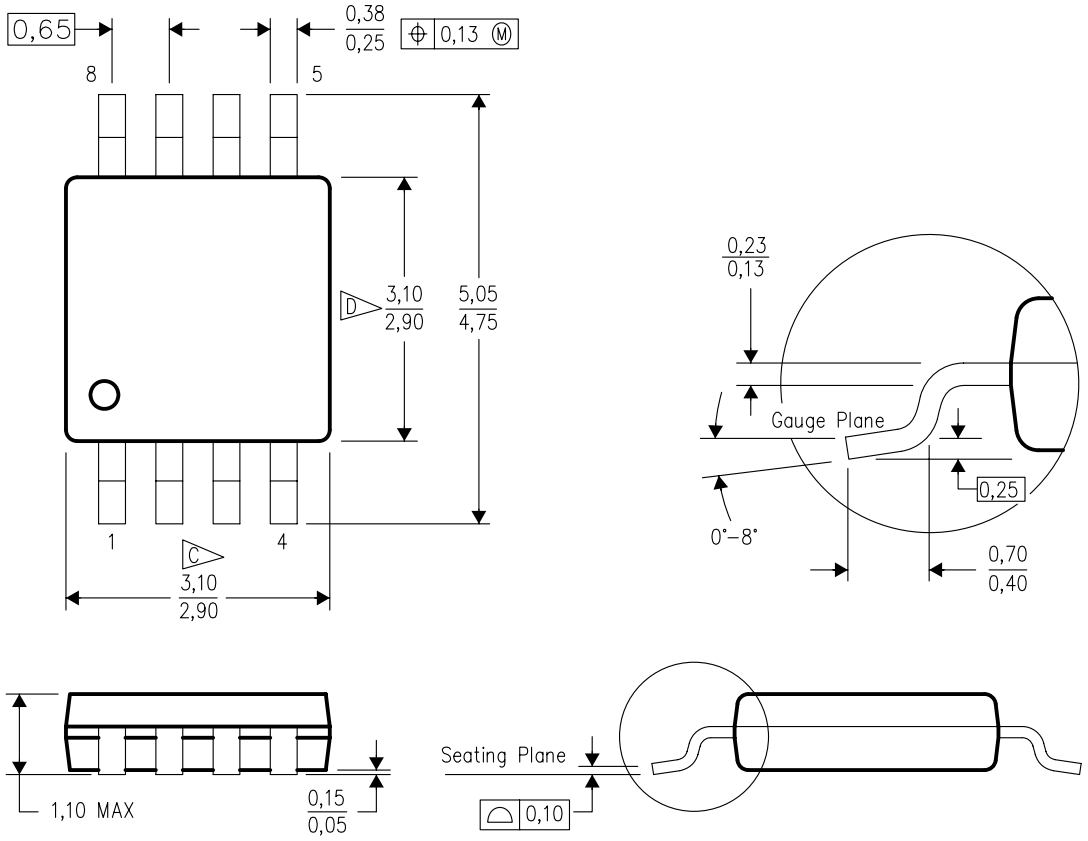
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

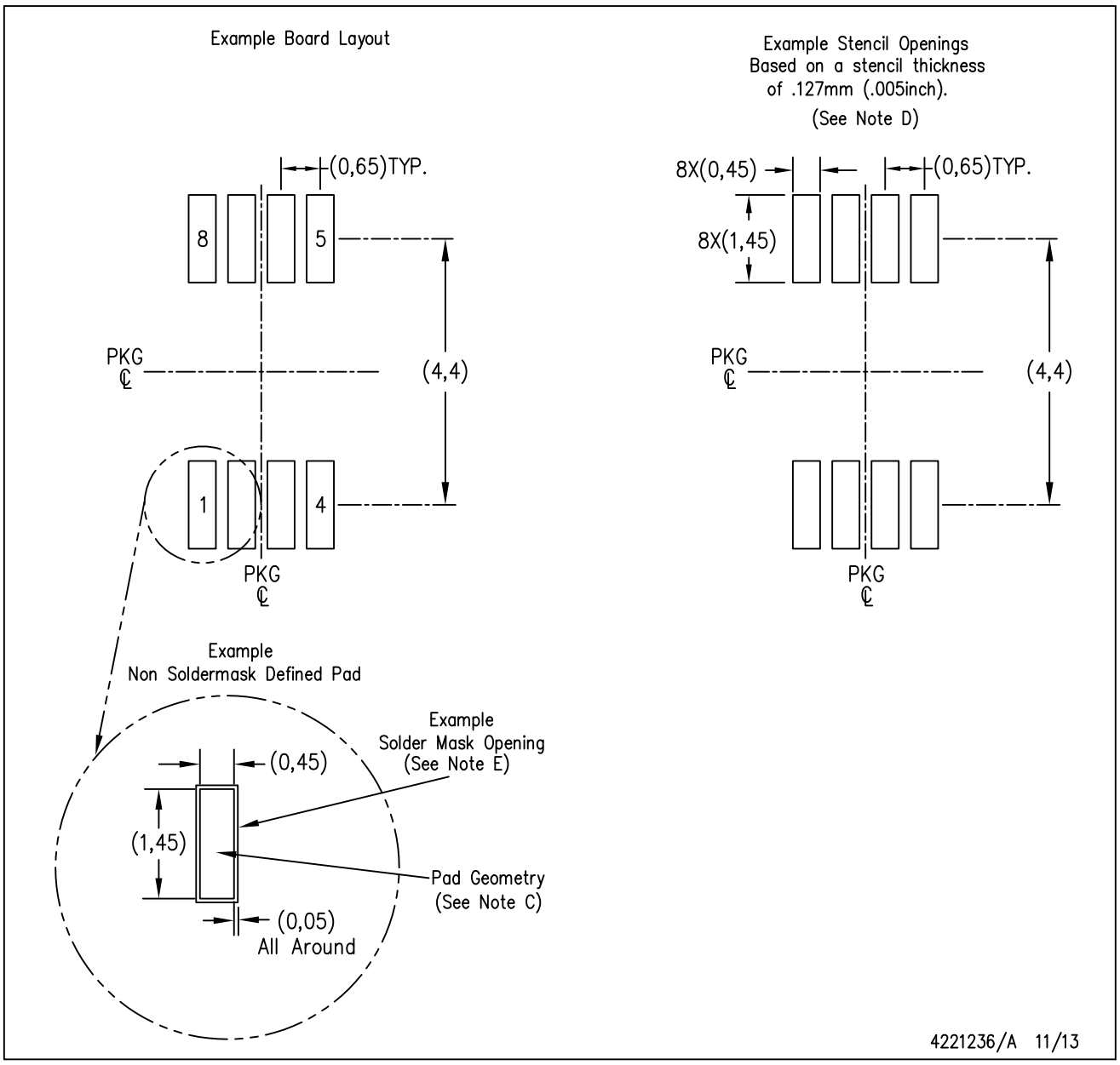
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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