

## FEATURES

- Windowed watchdog, 8 timeout options
- 26 reset threshold options
  - 2.5 V to 5 V in 100 mV increments
- 4 reset timeout options
  - 1 ms, 20 ms, 140 ms, and 1120 ms (minimum)
- Manual reset input
- Open-drain or push-pull  $\overline{\text{RESET}}$  outputs
- Low power consumption
- Specified over wide temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )
- Qualified for automotive applications
- 5-lead SOT-23 package

## APPLICATIONS

- Automotive
- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

## GENERAL DESCRIPTION

The [ADM8323/ADM8324](#) are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. An on-chip watchdog timer checks for activity within a preset timeout window. A reset signal can also be asserted by an external push-button switch through a manual reset input. The  $\overline{\text{RESET}}$  output is either push-pull ([ADM8323](#)) or open-drain ([ADM8324](#)).

A watchdog failure results in a low output on the  $\overline{\text{RESET}}$  pin. A failure can be triggered either by a fast watchdog error (watchdog pulses too close together) or by a slow watchdog error (no watchdog pulse within the timeout period). This effectively gives a window to observe the watchdog pulse. The watchdog timeout is measured from the last falling edge of the watchdog input (WDI). There are eight different watchdog windows available, as shown in Table 5.

## FUNCTIONAL BLOCK DIAGRAMS

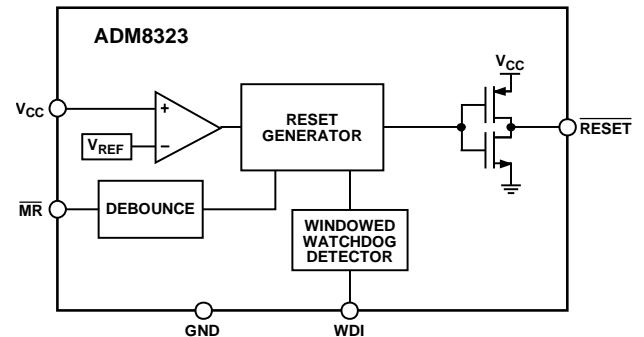


Figure 1.

11802-001

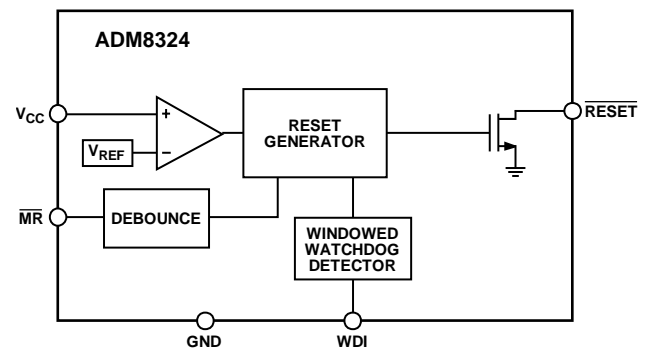


Figure 2.

11802-002

Each device is available in a choice of 26 reset threshold options from 2.5 V to 5 V in 100 mV increments. There are also four reset timeout options of 1 ms, 20 ms, 140 ms, and 1120 ms (minimum). Not all device options are available as standard models. See the Ordering Guide for details.

The [ADM8323/ADM8324](#) are available in a 5-lead SOT-23 package and typically consume only 10  $\mu\text{A}$ , making them suitable for use in low power portable applications.

**TABLE OF CONTENTS**

|  |    |   |    |
|--|----|---|----|
| Features .....                                   | 1  | Push-Pull $\overline{\text{RESET}}$ Output .....                        | 10 |
| Applications.....                                | 1  | Open-Drain $\overline{\text{RESET}}$ Output .....                       | 10 |
| Functional Block Diagrams.....                   | 1  | Manual Reset Input .....  | 10 |
| General Description .....                        | 1  | Windowed Watchdog Input.....  | 10 |
| Revision History .....                           | 2  | Applications Information .....  | 11 |
| Specifications.....                              | 3  | Watchdog Input Current .....  | 11 |
| Absolute Maximum Ratings.....                    | 5  | Negative Going $V_{CC}$ Transients.....                                 | 11 |
| ESD Caution.....                                 | 5  | Ensuring $\overline{\text{RESET}}$ Valid to $V_{CC} = 0\text{ V}$ ..... | 11 |
| Pin Configuration and Function Descriptions..... | 6  | Model Options .....   | 12 |
| Typical Performance Characteristics .....        | 7  | Outline Dimensions .....  | 13 |
| Theory of Operation .....                        | 10 | Ordering Guide .....  | 13 |
| Circuit Description.....                         | 10 | Automotive Products.....  | 14 |

**REVISION HISTORY**

**2/2018—Rev. A to Rev. B**

|   |    |
|---|----|
| Changes to General Description Section .....                          | 1  |
| Added Note 3, Table 1 .....   | 3  |
| Changed Model Options Section to Device Model Options<br>Section..... | 12 |
| Changes to Device Model Options Section .....                         | 12 |
| Deleted Table 7; Renumbered Sequentially.....                         | 13 |
| Changes to Ordering Guide .....                                       | 13 |

**3/2016—Rev. 0 to Rev. A**

|   |    |
|---|----|
| Change to Model Options Section Title ..... | 12 |
| Changes to Table 7.....                     | 13 |

**10/2013—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{CC} = (V_{TH} + 1.5\%)$  to 5.5 V,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ .

Table 1.

| Parameter  | Min                 | Typ                 | Max              | Unit                  | Test Conditions/Comments   |
|--|---------------------|---------------------|------------------|-----------------------|--|
| <b>SUPPLY</b>  |                     |                     |                  |                       |  |
| $V_{CC}$ Operating Voltage Range <sup>1</sup>                  | 0.9                 |                     | 5.5              | V                     |  |
| $V_{CC}$ that Guarantees Valid Output                          | 0.9                 |                     |                  |                       |  |
| Supply Current   |                     | 10                  | 20               | $\mu\text{A}$         | $V_{CC} = 5.5\text{ V}$ , $\text{WDI} = 0\text{ V}$                      |
|  |                     | 10                  | 18               | $\mu\text{A}$         | $V_{CC} = 3.6\text{ V}$ , $\text{WDI} = 0\text{ V}$                      |
| <b>RESET THRESHOLD VOLTAGE<sup>2,3</sup></b>                   |                     |                     |                  |                       |  |
|  | $V_{TH} - 1\%$      | $V_{TH}$            | $V_{TH} + 1\%$   | V                     | $T_A = 25^\circ\text{C}$   |
|  | $V_{TH} - 1.5\%$    | $V_{TH}$            | $V_{TH} + 1.5\%$ | V                     | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                        |
| <b>RESET THRESHOLD TEMPERATURE COEFFICIENT</b>                 |                     |                     |                  |                       |  |
|  |                     | 20                  |                  | ppm/ $^\circ\text{C}$ |  |
| <b>RESET THRESHOLD HYSTERESIS</b>                              |                     |                     |                  |                       |  |
|  |                     | $2.5 \times V_{TH}$ |                  | mV                    |  |
| <b>RESET TIMEOUT PERIOD<sup>3</sup></b>                        |                     |                     |                  |                       |  |
| Reset Timeout Option A   | 1                   | 1.4                 | 1.8              | ms                    | See Table 4  |
| Reset Timeout Option B   | 20                  | 28                  | 36               | ms                    |  |
| Reset Timeout Option C   | 140                 | 200                 | 260              | ms                    |  |
| Reset Timeout Option D   | 1120                | 1600                | 2080             | ms                    |  |
| <b><math>V_{CC}</math> TO RESET DELAY, <math>t_{RD}</math></b> |                     |                     |                  |                       |  |
|  |                     | 90                  |                  | $\mu\text{s}$         | $V_{CC}$ falling at 1 mV/ $\mu\text{s}$                                  |
| <b>PUSH-PULL OUTPUT (ADM8323)</b>                              |                     |                     |                  |                       |  |
| $\overline{\text{RESET}}$ Output Voltage                       |                     |                     | 0.2              | V                     | $V_{CC} \geq 0.9\text{ V}$ , $I_{\text{SINK}} = 25\ \mu\text{A}$         |
|  |                     |                     | 0.2              | V                     | $V_{CC} \geq 1.2\text{ V}$ , $I_{\text{SINK}} = 100\ \mu\text{A}$        |
|  |                     |                     | 0.2              | V                     | $V_{CC} \geq 2.7\text{ V}$ , $I_{\text{SINK}} = 1.2\text{ mA}$           |
|  |                     |                     | 0.3              | V                     | $V_{CC} \geq 4.5\text{ V}$ , $I_{\text{SINK}} = 3.2\text{ mA}$           |
|  | $0.9 \times V_{CC}$ |                     |                  | V                     | $V_{CC} \geq 2.7\text{ V}$ , $I_{\text{SOURCE}} = 500\ \mu\text{A}$      |
|  | $0.9 \times V_{CC}$ |                     |                  | V                     | $V_{CC} \geq 4.5\text{ V}$ , $I_{\text{SOURCE}} = 800\ \mu\text{A}$      |
| $\overline{\text{RESET}}$ Rise Time                            |                     | 50                  | 100              | ns                    | From 10% to 90% $V_{CC}$ , $C_L = 5\text{ pF}$ , $V_{CC} = 3.3\text{ V}$ |
| <b>OPEN-DRAIN OUTPUT (ADM8324)</b>                             |                     |                     |                  |                       |  |
| $\overline{\text{RESET}}$ Output Voltage                       |                     |                     | 0.2              | V                     | $V_{CC} \geq 0.9\text{ V}$ , $I_{\text{SINK}} = 25\ \mu\text{A}$         |
|  |                     |                     | 0.2              | V                     | $V_{CC} \geq 1.2\text{ V}$ , $I_{\text{SINK}} = 100\ \mu\text{A}$        |
|  |                     |                     | 0.2              | V                     | $V_{CC} \geq 2.7\text{ V}$ , $I_{\text{SINK}} = 1.2\text{ mA}$           |
|  |                     |                     | 0.3              | V                     | $V_{CC} \geq 4.5\text{ V}$ , $I_{\text{SINK}} = 3.2\text{ mA}$           |
| Open-Drain Reset Output Leakage Current                        |                     |                     | 1                | $\mu\text{A}$         |  |
| <b>WATCHDOG INPUT<sup>3</sup></b>                              |                     |                     |                  |                       |  |
| Watchdog Timeout Period (Fast), $t_{WD-FAST}$                  |                     |                     |                  |                       |  |
| Watchdog Timeout Option A                                      | 1                   |                     | 1.5              | ms                    | See Table 5  |
| Watchdog Timeout Option B                                      | 10                  |                     | 15               | ms                    |  |
| Watchdog Timeout Option C                                      | 10                  |                     | 15               | ms                    |  |
| Watchdog Timeout Option D                                      | 10                  |                     | 15               | ms                    |  |
| Watchdog Timeout Option E                                      | 10                  |                     | 15               | ms                    |  |
| Watchdog Timeout Option F                                      | 16                  |                     | 24               | ms                    |  |
| Watchdog Timeout Option G                                      | 27                  |                     | 41               | ms                    |  |
| Watchdog Timeout Option H                                      | 512                 |                     | 768              | ms                    |  |
| Watchdog Timeout Period (Slow), $t_{WD-SLOW}$                  |                     |                     |                  |                       |  |
| Watchdog Timeout Option A                                      | 10                  |                     | 15               | ms                    |  |
| Watchdog Timeout Option B                                      | 100                 |                     | 150              | ms                    |  |
| Watchdog Timeout Option C                                      | 300                 |                     | 450              | ms                    |  |
| Watchdog Timeout Option D                                      | 10                  |                     | 15               | sec                   |  |
| Watchdog Timeout Option E                                      | 60                  |                     | 90               | sec                   |  |
| Watchdog Timeout Option F                                      | 44                  |                     | 66               | ms                    |  |
| Watchdog Timeout Option G                                      | 76                  |                     | 114              | ms                    |  |
| Watchdog Timeout Option H                                      | 1.24                |                     | 1.86             | sec                   |  |

| Parameter                          | Min                 | Typ   | Max                 | Unit      | Test Conditions/Comments                                    |
|------------------------------------|---------------------|-------|---------------------|-----------|---|
| WDI Pulse Width                    | 200                 |       |                     | ns        | $V_{IL} = 0.3 \times V_{CC}$ , $V_{IH} = 0.7 \times V_{CC}$ |
| WDI Glitch Immunity                |                     | 100   |                     | ns        |   |
| WDI Input Threshold                | $0.3 \times V_{CC}$ |       | $0.7 \times V_{CC}$ | V         | $V_{WDI} = V_{CC}$<br>$V_{WDI} = 0 V$                       |
| WDI Input Current                  |                     | 0.35  | 1                   | $\mu A$   |   |
|                                    | -1                  | -0.35 |                     | $\mu A$   |   |
| <b>MANUAL RESET INPUT</b>          |                     |       |                     |           |   |
| $V_{IL}$                           |                     |       | 0.8                 | V         | $V_{CC} = 5 V$  |
| $V_{IH}$                           | 2.0                 |       |                     | V         |   |
| $\overline{MR}$ Input Pulse Width  | 1                   |       |                     | $\mu s$   |   |
| $\overline{MR}$ Glitch Rejection   |                     | 100   |                     | ns        |   |
| $\overline{MR}$ Pull-Up Resistance | 35                  | 75    | 125                 | $k\Omega$ |   |
| $\overline{MR}$ to Reset Delay     |                     | 350   |                     | ns        |   |

<sup>1</sup> The device switches from undervoltage reset to normal operation when  $1.5 V < V_{CC} < 2.5 V$ .

<sup>2</sup> The device monitors  $V_{CC}$  through an internal factory trimmed voltage divider, which programs the nominal reset threshold. Factory trimmed reset thresholds are available in approximately 100 mV increments from 2.5 V to 5 V.

<sup>3</sup> Not all device options are available as standard models. See the Ordering Guide for details.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

| Parameter                                    | Rating                        |
|--|-------------------------------|
| $V_{CC}$                                     | -0.3 V to +6 V                |
| All Other Pins                               | -0.3 V to ( $V_{CC} + 0.3$ V) |
| Output Current ( $\overline{\text{RESET}}$ ) | 20 mA                         |
| Operating Temperature Range                  | -40°C to +125°C               |
| Storage Temperature Range                    | -65°C to +150°C               |
| $\theta_{JA}$ Thermal Impedance, SOT-23      | 270°C/W                       |
| Lead Temperature                             |                               |
| Soldering (10 sec)                           | 300°C                         |
| Vapor Phase (60 sec)                         | 215°C                         |
| Infrared (15 sec)                            | 220°C                         |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

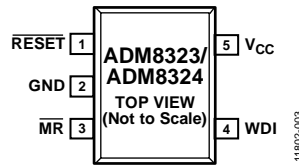


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description   |
|---------|----------|---|
| 1       | RESET    | Active Low Reset Output. Asserted whenever $V_{CC}$ is below the reset threshold, $V_{TH}$ . This pin is a push-pull output stage for the ADM8323 and an open-drain output stage for the ADM8324. |
| 2       | GND      | Ground.   |
| 3       | MR       | Manual Reset Input. This is an active low input that, when forced low for greater than the glitch filter time, generates a reset. It features a 75 k $\Omega$ internal pull-up resistor.          |
| 4       | WDI      | Watchdog Input. Generates a reset if the WDI pulse is not within the watchdog window.   |
| 5       | $V_{CC}$ | Power Supply Voltage Being Monitored.   |

# TYPICAL PERFORMANCE CHARACTERISTICS

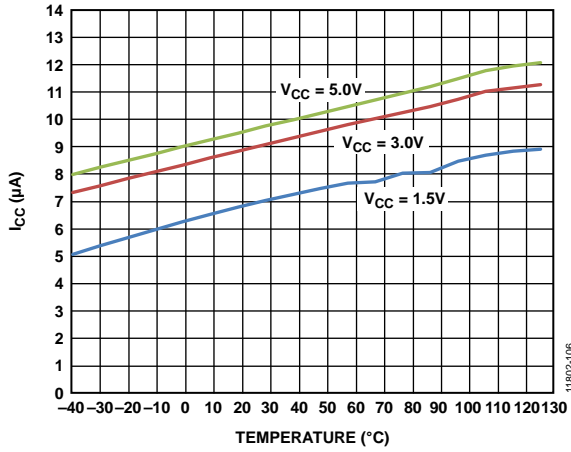


Figure 4. Supply Current ( $I_{CC}$ ) vs. Temperature

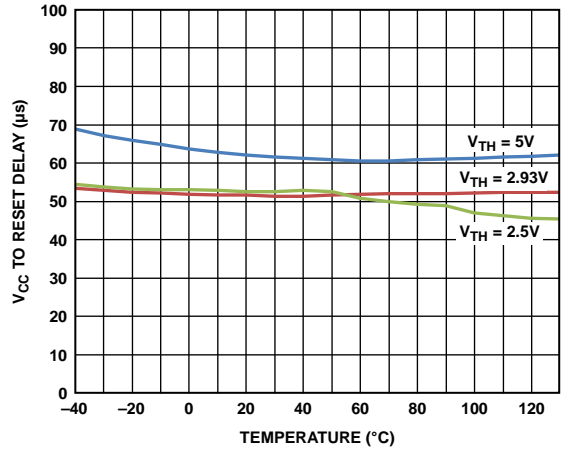


Figure 7.  $V_{CC}$  to Reset Delay vs. Temperature

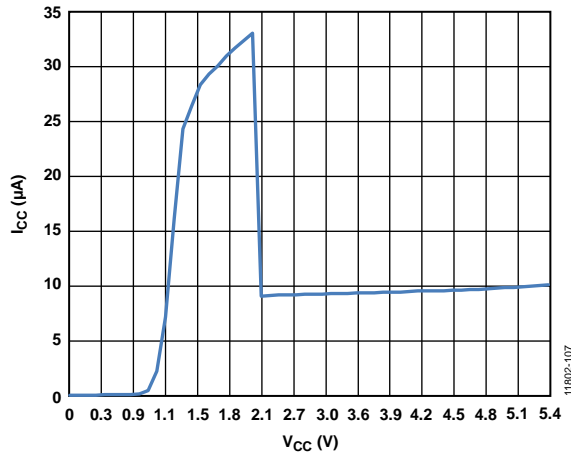


Figure 5. Supply Current ( $I_{CC}$ ) vs. Supply Voltage ( $V_{CC}$ )

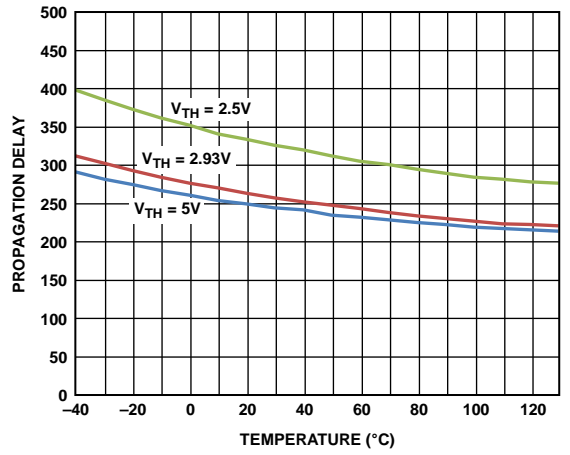


Figure 8. Manual Reset to Reset Propagation Delay vs. Temperature

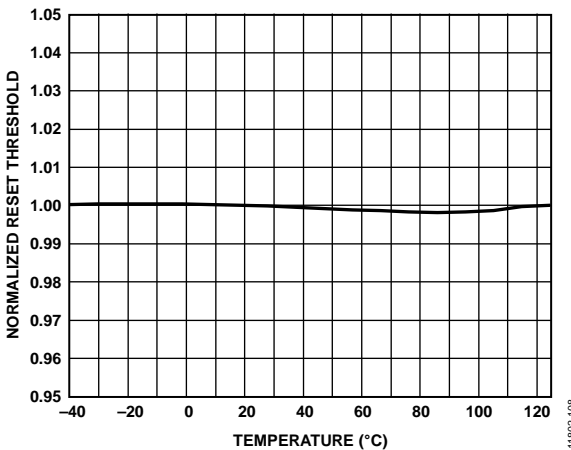


Figure 6. Normalized Reset Threshold vs. Temperature

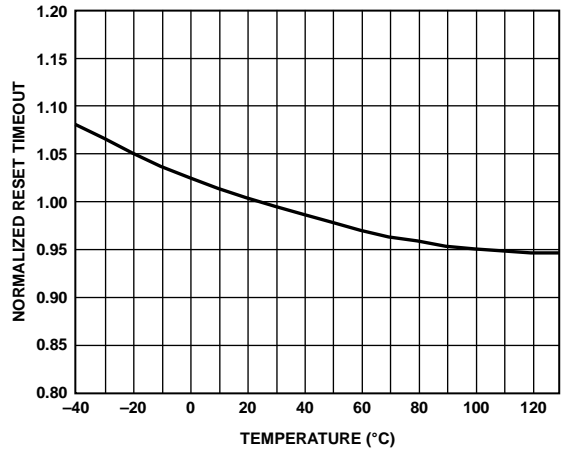


Figure 9. Normalized Reset Timeout vs. Temperature

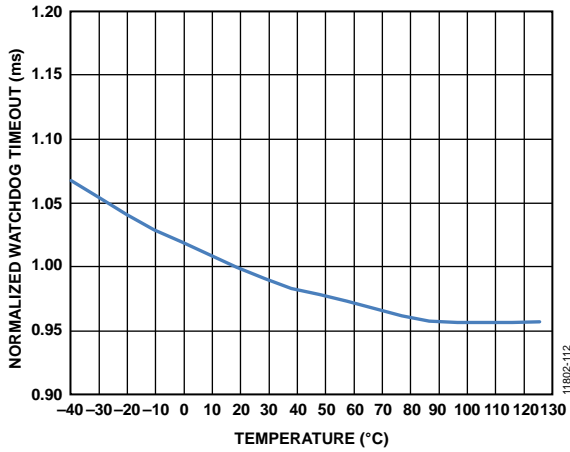


Figure 10. Normalized Watchdog Timeout vs. Temperature, Fast Timeout

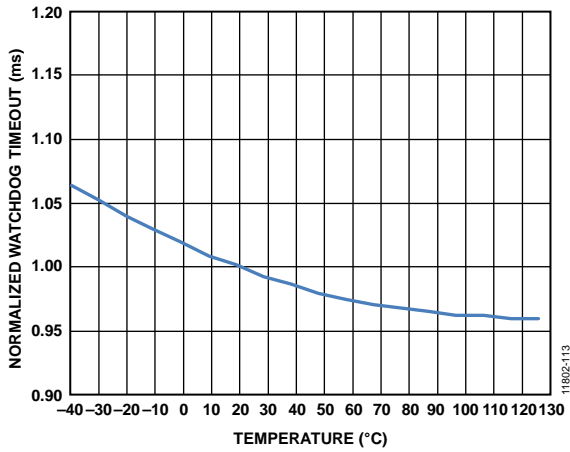


Figure 11. Normalized Watchdog Timeout vs. Temperature, Slow Timeout

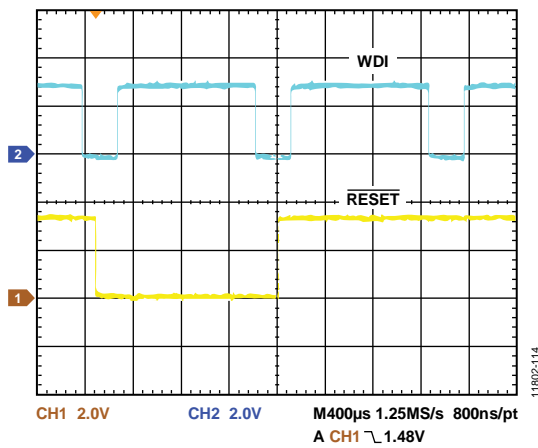


Figure 12. Fast Watchdog Timeout Period, Watchdog Timeout Option A

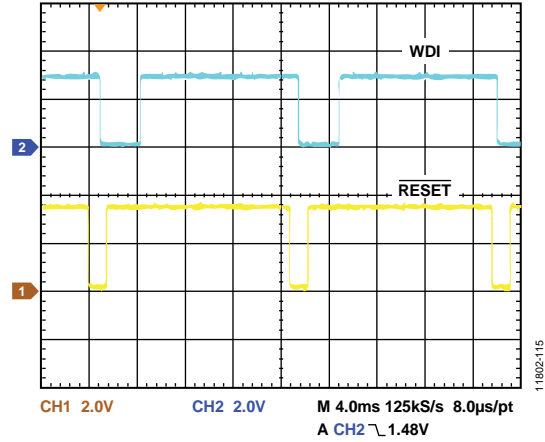


Figure 13. Slow Watchdog Timeout Period, Watchdog Timeout Option A

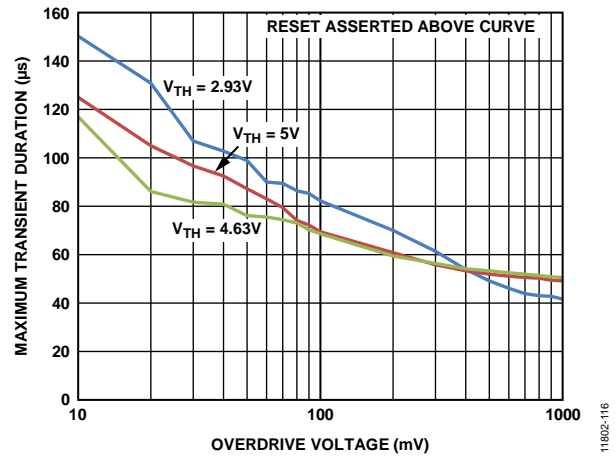


Figure 14. Maximum  $V_{CC}$  Transient Duration vs. Reset Threshold Overdrive

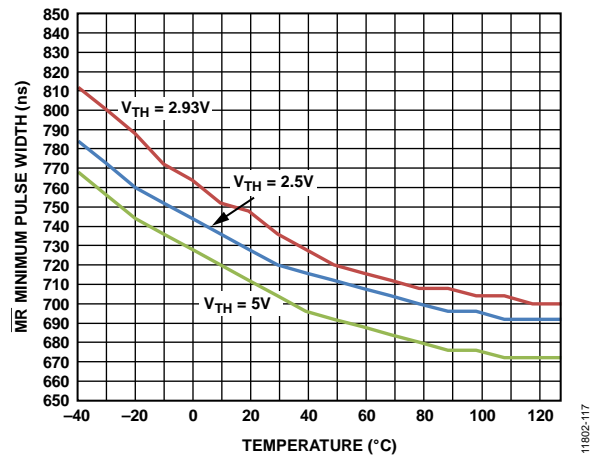


Figure 15. Manual Reset ( $\overline{MR}$ ) Minimum Pulse Width vs. Temperature



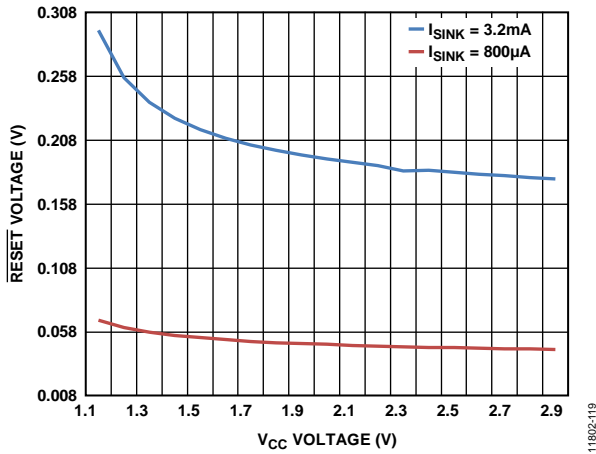


Figure 16.  $\overline{\text{RESET}}$  Open-Drain  $V_{OL}$  Voltage vs.  $V_{CC}$  Voltage ( $V_{TH} = 3\text{ V}$ )

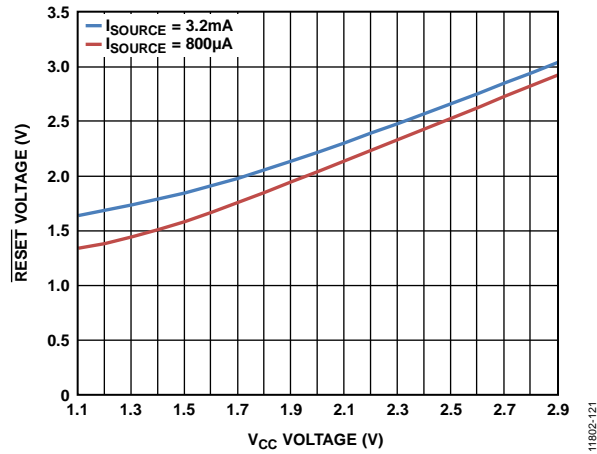


Figure 18.  $\overline{\text{RESET}}$  Push-Pull  $V_{OH}$  Voltage vs.  $V_{CC}$  Voltage ( $V_{TH} = 3\text{ V}$ )

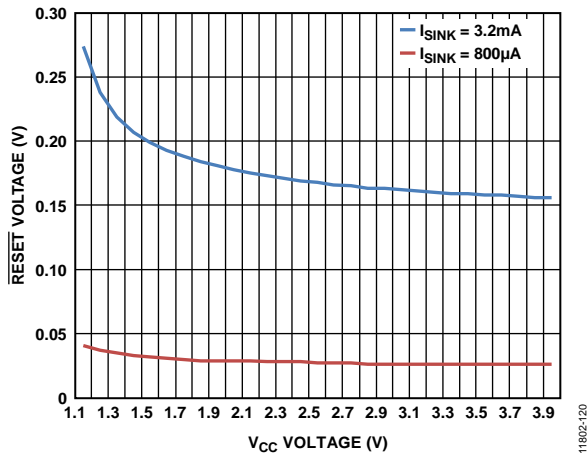


Figure 17.  $\overline{\text{RESET}}$  Push-Pull  $V_{OL}$  Voltage vs.  $V_{CC}$  Voltage ( $V_{TH} = 4\text{ V}$ )

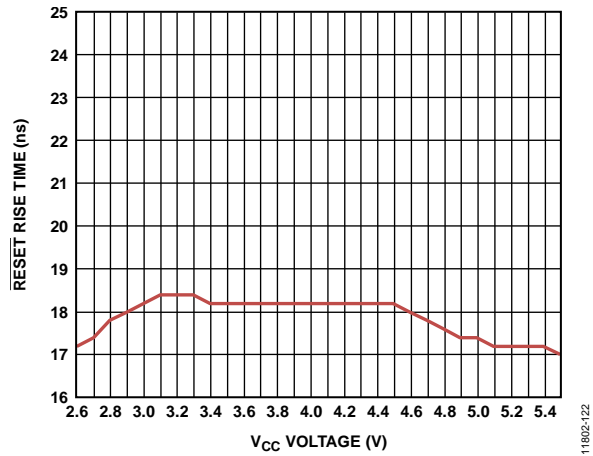


Figure 19.  $\overline{\text{RESET}}$  Push-Pull Rise Time vs.  $V_{CC}$  Voltage

## THEORY OF OPERATION

### CIRCUIT DESCRIPTION

The ADM8323/ADM8324 provide microprocessor supply voltage supervision by controlling the microprocessor reset input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a windowed watchdog timer. If the user detects a problem with system operation, a manual reset input is available to reset the microprocessor, for example, by means of an external push-button switch.

### PUSH-PULL RESET OUTPUT

The ADM8323 features an active low push-pull reset output. The reset signal is guaranteed to be valid for  $V_{CC}$  down to 0.9 V. The reset output is asserted when  $V_{CC}$  is below the reset threshold ( $V_{TH}$ ), when  $\overline{MR}$  is driven low, or when WDI is not serviced within the watchdog timeout window. Reset remains asserted for the duration of the reset active timeout period ( $t_{RP}$ ) after  $V_{CC}$  rises above the reset threshold and  $\overline{MR}$  transitions from low to high or after the watchdog timer fault occurs. Figure 20 illustrates the behavior of the reset output.

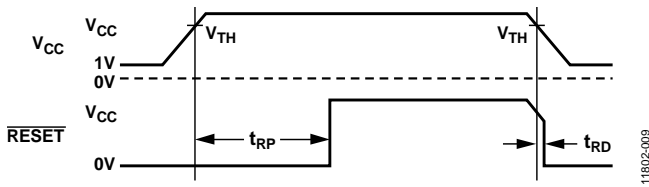


Figure 20. Reset Timing Diagram

### OPEN-DRAIN RESET OUTPUT

The ADM8324 has an active low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail no higher than  $V_{CC}$ . Use a resistor that complies with the logic low and logic high voltage level requirements of the microprocessor while supplying input current and leakage paths on the RESET line. A 10 k $\Omega$  resistor is adequate in most situations.

### MANUAL RESET INPUT

The ADM8323/ADM8324 feature a manual reset input ( $\overline{MR}$ ), which when driven low, asserts the reset output. When  $\overline{MR}$  transitions from low to high, the reset output remains asserted for the duration of the reset active timeout period before deasserting. The  $\overline{MR}$  input has a 75 k $\Omega$ , internal pull-up resistor so that the input is always high when unconnected. An external push-button switch can be connected between  $\overline{MR}$  and ground so the user can generate a reset. Debounce circuitry for this purpose is integrated on chip.

Noise immunity is provided on the  $\overline{MR}$  input, and fast, negative going transients of up to 100 ns (typical) are ignored. A 0.1  $\mu$ F capacitor between MR and ground provides additional noise immunity.

### WINDOWED WATCHDOG INPUT

The ADM8323/ADM8324 feature a windowed watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every high to low logic transition on the watchdog input pin (WDI), which detects pulses as short as 200 ns. If this watchdog pulse does not occur within the defined time window, a reset asserts. Failure of the microprocessor to toggle WDI within the watchdog window indicates a code execution error and, therefore, the generated reset pulse restarts the microprocessor in a known state.

As well as logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on  $V_{CC}$  or due to  $\overline{MR}$  being pulled low. When a reset is asserted, the watchdog timer is cleared and does not begin counting again until the reset deasserts. The windowed watchdog timer cannot be disabled.

All WDI input pulses are ignored while a reset is asserted. After the reset deasserts, the first WDI falling edge is ignored for the fast fault condition.

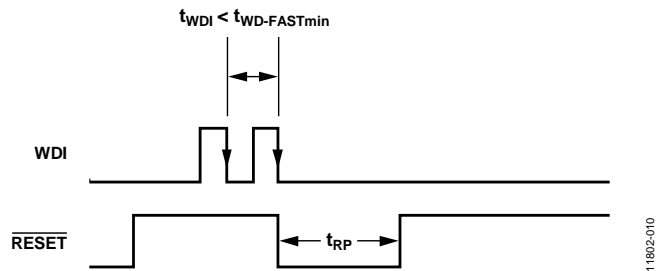


Figure 21. Watchdog Fast Timeout Fault

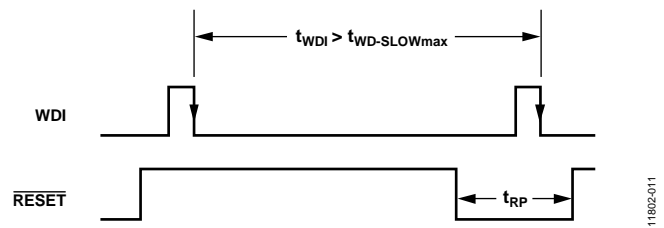


Figure 22. Watchdog Slow Timeout Fault

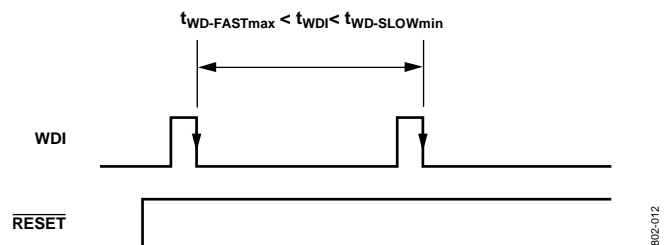


Figure 23. Normal Watchdog Operation

## APPLICATIONS INFORMATION

### WATCHDOG INPUT CURRENT

There is no way to disable the windowed watchdog functionality. Do not leave the WDI pin floating because this is not a valid mode of operation. If the WDI pin is not in a defined state at startup, this can lead to high supply current until the microprocessor is enabled and takes control of the WDI pin. A solution to this is to add a 100 k $\Omega$  pull-up or pull-down resistor on the WDI pin to hold it in a defined state until the microprocessor is enabled.

### NEGATIVE GOING $V_{CC}$ TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM8323/ADM8324 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 14 plots  $V_{CC}$  transient duration vs. reset threshold overdrive. The curves show combinations of reset threshold overdrive and duration for which a reset is not generated for 5 V, 4.63 V, and 2.93 V reset threshold devices. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 80  $\mu$ s typically does not cause a reset. However, if the transient is any larger in reset threshold overdrive or duration, a reset generates. An optional 0.1  $\mu$ F bypass capacitor mounted near  $V_{CC}$  provides additional glitch rejection.

### ENSURING $\overline{RESET}$ VALID TO $V_{CC} = 0$ V

The reset output is guaranteed valid for  $V_{CC}$  as low as 0.9 V. However, by using an external resistor with the push-pull configured reset output on the ADM8323, a valid output for  $V_{CC}$  as low as 0 V is possible. For this active low reset output, a resistor connected between  $\overline{RESET}$  and ground pulls the output low when it is unable to sink current. Use a large resistance, such as 100 k $\Omega$ , so that it does not overload the reset output when  $V_{CC}$  is above 0.9 V.

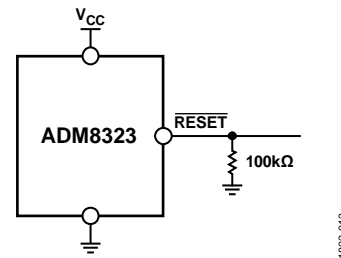


Figure 24. Ensuring  $\overline{RESET}$  Valid to  $V_{CC} = 0$  V

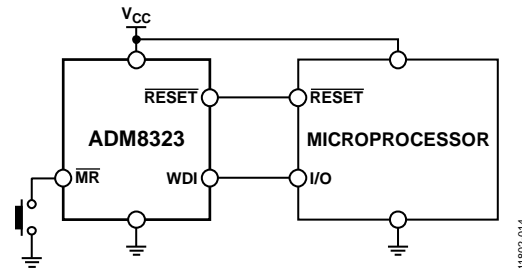


Figure 25. ADM8323 Typical Application Circuit

## DEVICE MODEL OPTIONS

The ADM8323/ADM8324 include many device options; however, not all options are released for sale. Released options are called standard models and are listed in the Ordering Guide. For the most up to date list of standard models, refer to the Analog Devices website at [www.analog.com/supervisory](http://www.analog.com/supervisory). Contact an Analog Devices sales representative for information on nonstandard models, and be aware that samples and production units have long lead times.

Table 4. Reset Timeout Options

| Suffix | Minimum | Typical | Maximum | Unit |
|--------|---------|---------|---------|------|
| A      | 1       | 1.4     | 1.8     | ms   |
| B      | 20      | 28      | 36      | ms   |
| C      | 140     | 200     | 260     | ms   |
| D      | 1120    | 1600    | 2080    | ms   |

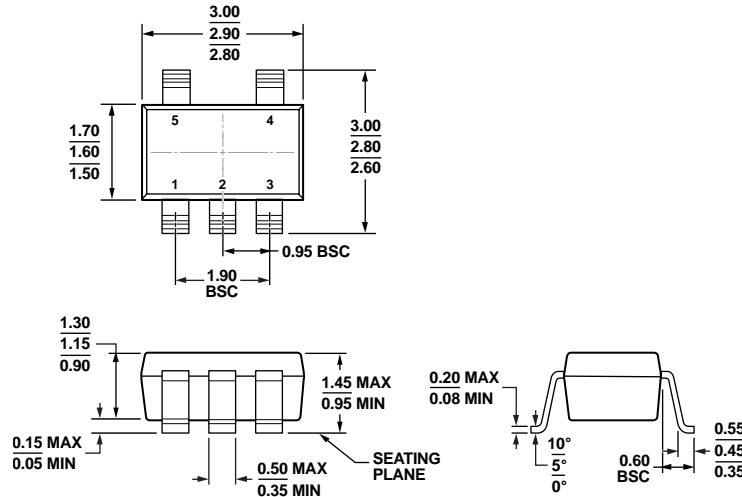
Table 5. Watchdog Timeout Options

| Suffix | Fast    |      | Slow    |      |
|--------|---------|------|---------|------|
|        | Maximum | Unit | Minimum | Unit |
| A      | 1.5     | ms   | 10      | ms   |
| B      | 15      | ms   | 100     | ms   |
| C      | 15      | ms   | 300     | ms   |
| D      | 15      | ms   | 10      | sec  |
| E      | 15      | ms   | 60      | sec  |
| F      | 24      | ms   | 44      | ms   |
| G      | 41      | ms   | 76      | ms   |
| H      | 768     | ms   | 1.24    | sec  |

Table 6. Reset Voltage Threshold Options

| Reset Threshold Number | T <sub>A</sub> = 25°C |         |         | T <sub>A</sub> = -40°C to +125°C |         | Unit |
|------------------------|-----------------------|---------|---------|----------------------------------|---------|------|
|                        | Minimum               | Typical | Maximum | Minimum                          | Maximum |      |
| 50                     | 4.950                 | 5.000   | 5.050   | 4.925                            | 5.075   | V    |
| 49                     | 4.851                 | 4.900   | 4.949   | 4.826                            | 4.974   | V    |
| 48                     | 4.752                 | 4.800   | 4.848   | 4.728                            | 4.872   | V    |
| 47                     | 4.653                 | 4.700   | 4.747   | 4.629                            | 4.771   | V    |
| 46                     | 4.584                 | 4.630   | 4.676   | 4.560                            | 4.700   | V    |
| 45                     | 4.455                 | 4.500   | 4.545   | 4.432                            | 4.568   | V    |
| 44                     | 4.346                 | 4.390   | 4.434   | 4.324                            | 4.456   | V    |
| 43                     | 4.257                 | 4.300   | 4.343   | 4.235                            | 4.365   | V    |
| 42                     | 4.158                 | 4.200   | 4.242   | 4.137                            | 4.263   | V    |
| 41                     | 4.059                 | 4.100   | 4.141   | 4.038                            | 4.162   | V    |
| 40                     | 3.960                 | 4.00    | 4.040   | 3.940                            | 4.060   | V    |
| 39                     | 3.861                 | 3.900   | 3.939   | 3.841                            | 3.959   | V    |
| 38                     | 3.762                 | 3.800   | 3.838   | 3.743                            | 3.857   | V    |
| 37                     | 3.663                 | 3.700   | 3.737   | 3.644                            | 3.756   | V    |
| 36                     | 3.564                 | 3.600   | 3.636   | 3.546                            | 3.654   | V    |
| 35                     | 3.465                 | 3.500   | 3.535   | 3.447                            | 3.553   | V    |
| 34                     | 3.366                 | 3.400   | 3.434   | 3.349                            | 3.451   | V    |
| 33                     | 3.267                 | 3.300   | 3.333   | 3.250                            | 3.350   | V    |
| 32                     | 3.168                 | 3.200   | 3.232   | 3.152                            | 3.248   | V    |
| 31                     | 3.049                 | 3.080   | 3.111   | 3.033                            | 3.127   | V    |
| 30                     | 2.970                 | 3.000   | 3.030   | 2.955                            | 3.045   | V    |
| 29                     | 2.901                 | 2.930   | 2.959   | 2.886                            | 2.974   | V    |
| 28                     | 2.772                 | 2.800   | 2.828   | 2.758                            | 2.842   | V    |
| 27                     | 2.673                 | 2.700   | 2.727   | 2.659                            | 2.741   | V    |
| 26                     | 2.604                 | 2.630   | 2.656   | 2.590                            | 2.670   | V    |
| 25                     | 2.475                 | 2.500   | 2.525   | 2.462                            | 2.538   | V    |

### OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 26. 5-Lead Small Outline Transistor Package [SOT-23] (RJ-5)

Dimensions shown in millimeters

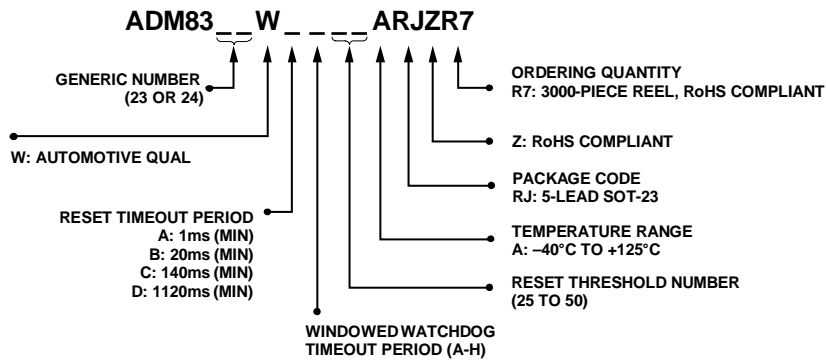


Figure 27. Ordering Code Structure

### ORDERING GUIDE

| Model <sup>1,2,3,4</sup> | Temperature Range | Reset Threshold (V) | Max Fast Timeout (ms) | Min Slow Timeout (ms) | Min Reset Timeout (ms) | Ordering Quantity | Package Description | Package Option | Marking Code |
|--------------------------|-------------------|---------------------|-----------------------|-----------------------|------------------------|-------------------|---------------------|----------------|--------------|
| ADM8323WCC29ARJZR7       | -40°C to +125°C   | 2.93                | 15                    | 300                   | 140                    | 3,000             | 5-Lead SOT-23       | RJ-5           | LNO          |
| ADM8323WCC46ARJZR7       | -40°C to +125°C   | 4.63                | 15                    | 300                   | 140                    | 3,000             | 5-Lead SOT-23       | RJ-5           | LNO          |
| ADM8324WAH29ARJZR7       | -40°C to +125°C   | 2.93                | 768                   | 1240                  | 1                      | 3,000             | 5-Lead SOT-23       | RJ-5           | LMU          |
| ADM8324WCA29ARJZR7       | -40°C to +125°C   | 2.93                | 1.5                   | 10                    | 140                    | 3,000             | 5-Lead SOT-23       | RJ-5           | LMU          |
| ADM8324WCA46ARJZR7       | -40°C to +125°C   | 4.63                | 1.5                   | 10                    | 140                    | 3,000             | 5-Lead SOT-23       | RJ-5           | LMU          |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

<sup>3</sup> The ADM8323/ADM8324 include many device options; however, not all options are released for sale. Released options are called standard models and are listed in the Ordering Guide. For the most up to date list of standard models, refer to the Analog Devices website at [www.analog.com/supervisory](http://www.analog.com/supervisory). Contact an Analog Devices sales representative for information on nonstandard models, and be aware that samples and production units have long lead times.

<sup>4</sup> If ordering nonstandard models, complete the ordering code shown in Figure 27 by inserting reset timeout, watchdog timeout, and reset threshold suffixes from Table 4 to Table 6.

**AUTOMOTIVE PRODUCTS**

The [ADM8323W/ADM8324W](#) model are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**NOTES**

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