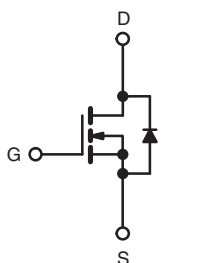
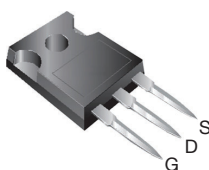


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	1000	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	2.0
Q_g (Max.) (nC)	190	
Q_{gs} (nC)	23	
Q_{gd} (nC)	110	
Configuration	Single	

TO-247AC


N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFPG50PbF SiHFPG50-E3
SnPb	IRFPG50 SiHFPG50

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	1000	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	24	
Linear Derating Factor		1.5	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	800	mJ
Repetitive Avalanche Current ^a	I_{AR}	6.0	A
Repetitive Avalanche Energy ^a	E_{AR}	19	mJ
Maximum Power Dissipation	P_D	190	W
Peak Diode Recovery dV/dt ^c	dV/dt	1.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

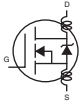

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 40\text{ mH}$, $R_g = 25\ \Omega$, $I_{AS} = 6.1\text{ A}$ (see fig. 12).
- $I_{SD} \leq 6.1\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq 600$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		1000	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	1.2	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V	
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 1000 V, V _{GS} = 0 V		-	-	100	μA	
		V _{DS} = 800 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.6 A ^b	-	-	2.0	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 100 V, I _D = 3.6 A ^b		5.4	-	-	S	
Dynamic								
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2800	-	pF	
Output Capacitance	C _{oss}			-	250	-		
Reverse Transfer Capacitance	C _{rss}			-	84	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6.1 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	190	nC	
Gate-Source Charge	Q _{gs}			-	-	23		
Gate-Drain Charge	Q _{gd}			-	-	110		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 500 V, I _D = 6.1 A, R _g = 6.2 Ω, R _D = 81 Ω, see fig. 10 ^b		-	19	-	ns	
Rise Time	t _r			-	35	-		
Turn-Off Delay Time	t _{d(off)}			-	130	-		
Fall Time	t _f			-	36	-		
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact			-	5.0	-	nH
Internal Source Inductance	L _S				-	13	-	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode			-	-	6.1	A
Pulsed Diode Forward Current ^a	I _{SM}				-	-	24	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 6.1 A, V _{GS} = 0 V ^b		-	-	1.8	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 6.1 A, dI/dt = 100 A/μs ^b		-	630	950	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.5	5.3	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

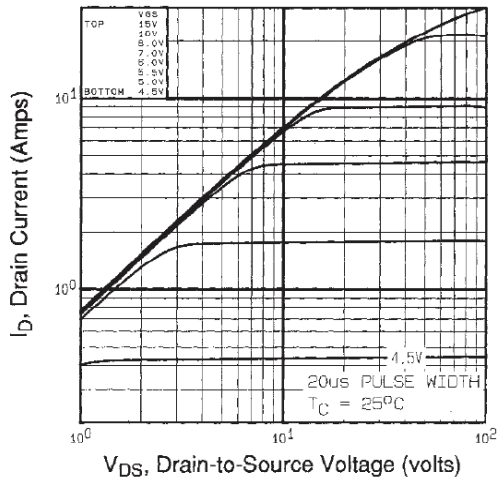


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

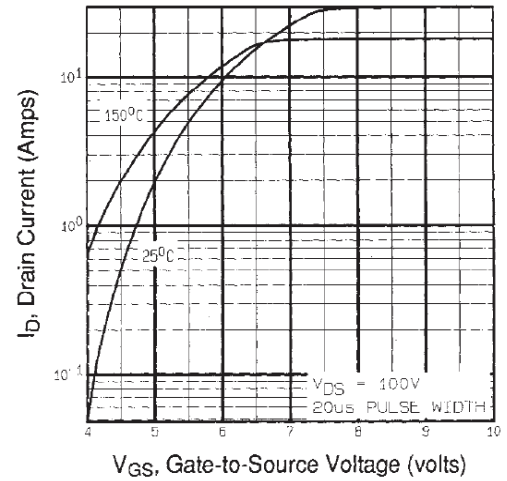


Fig. 3 - Typical Transfer Characteristics

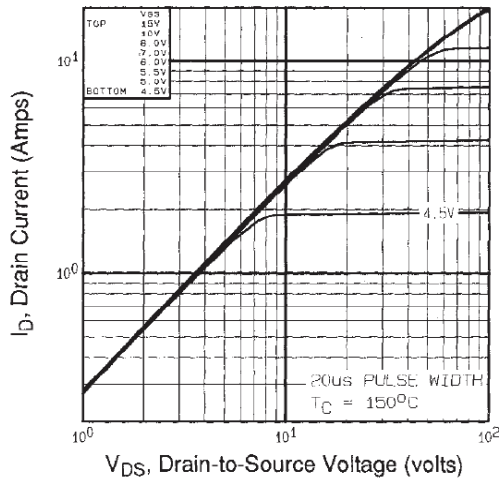


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

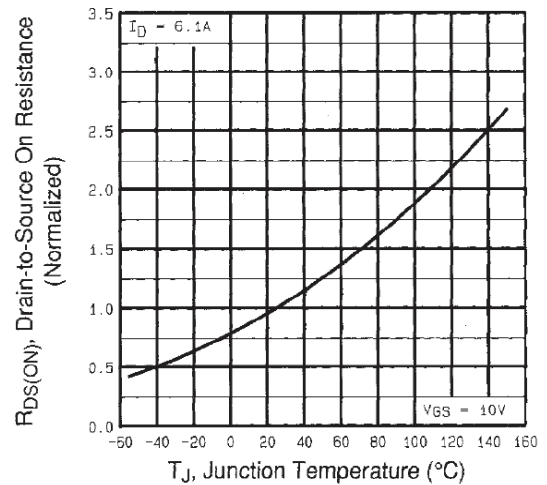


Fig. 4 - Normalized On-Resistance vs. Temperature

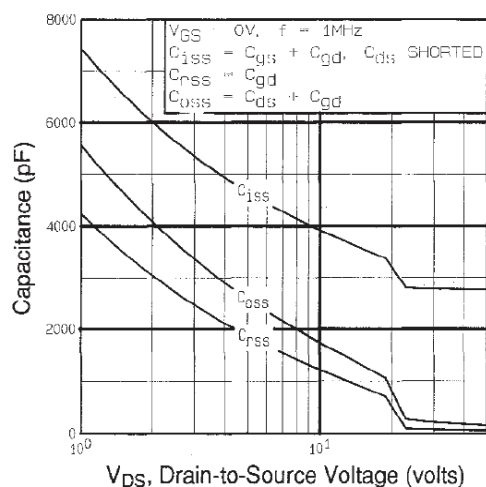


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

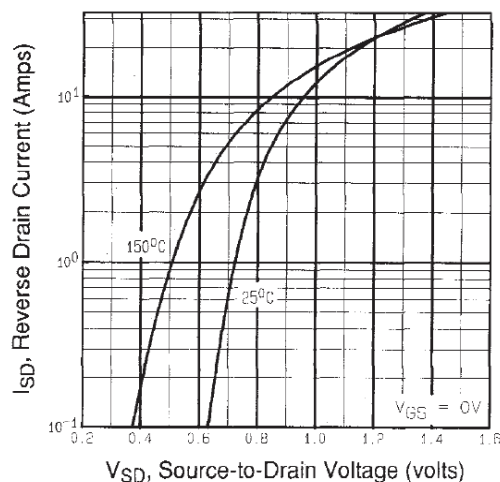


Fig. 7 - Typical Source-Drain Diode Forward Voltage

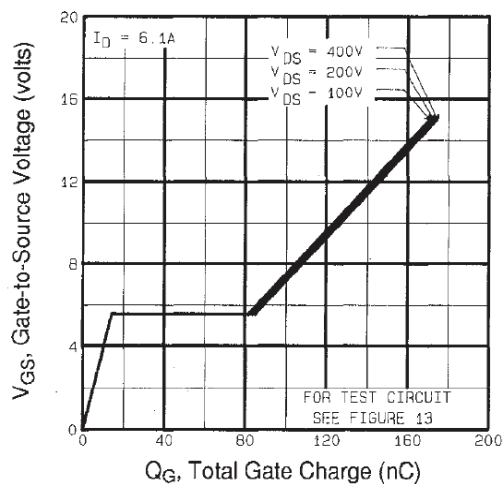


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

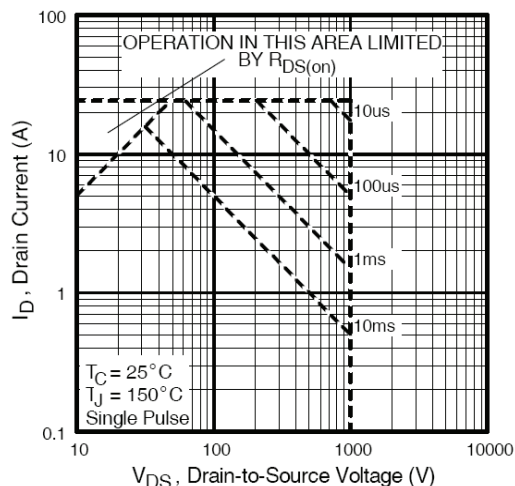


Fig. 8 - Maximum Safe Operating Area

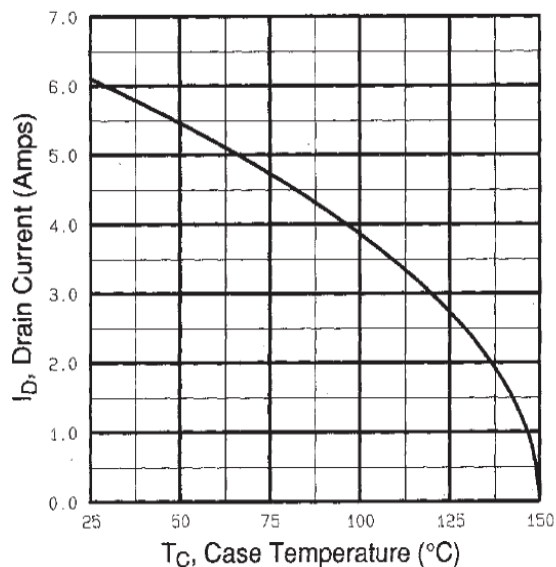


Fig. 9 - Maximum Drain Current vs. Case Temperature

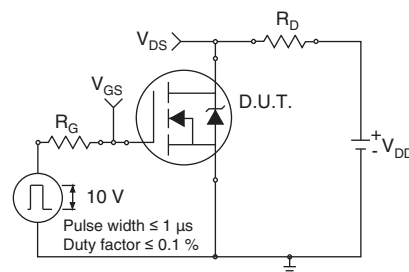


Fig. 10a - Switching Time Test Circuit

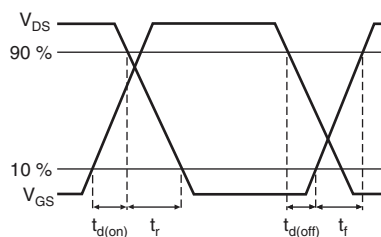


Fig. 10b - Switching Time Waveforms

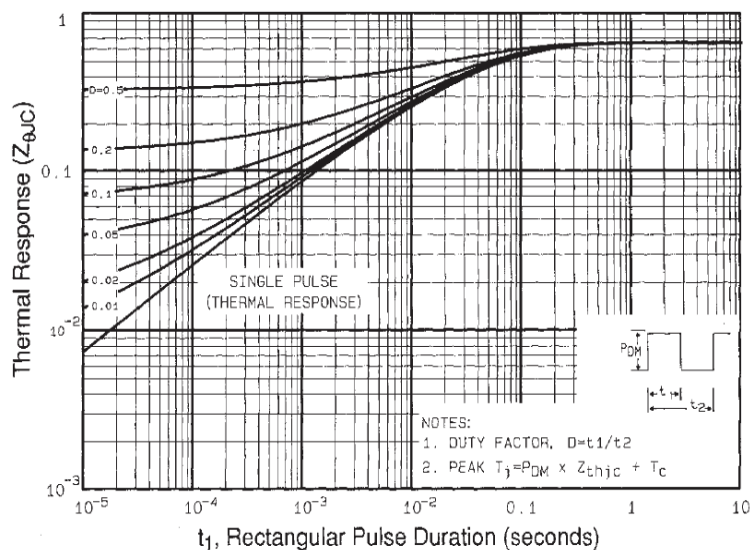


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

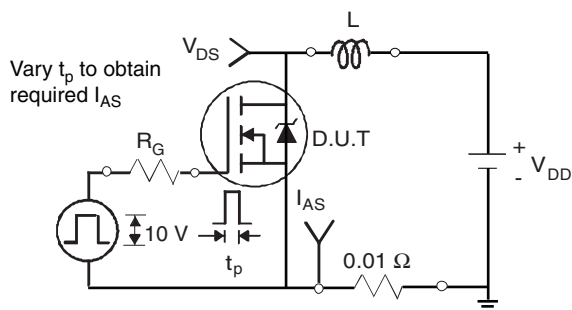


Fig. 12a - Unclamped Inductive Test Circuit

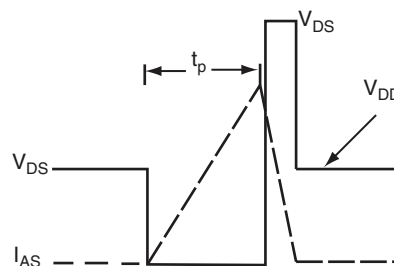


Fig. 12b - Unclamped Inductive Waveforms

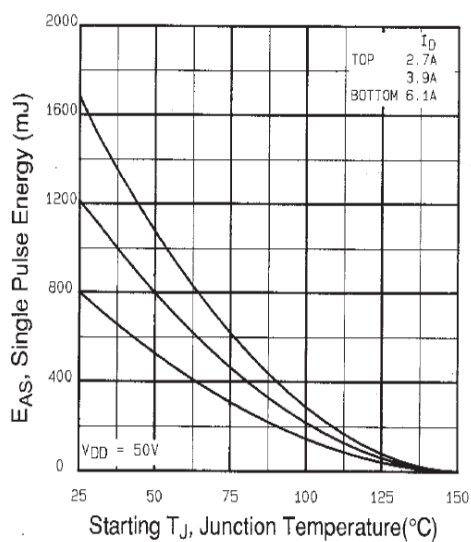


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

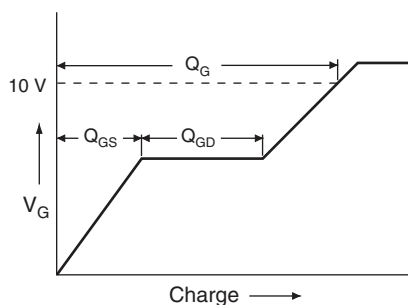


Fig. 13a - Basic Gate Charge Waveform

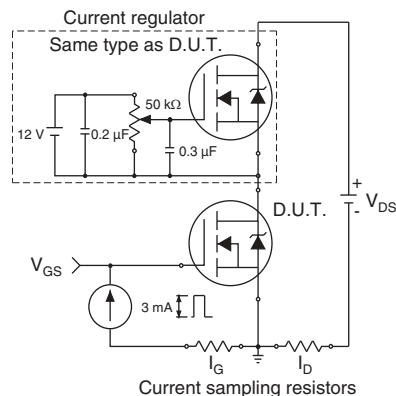
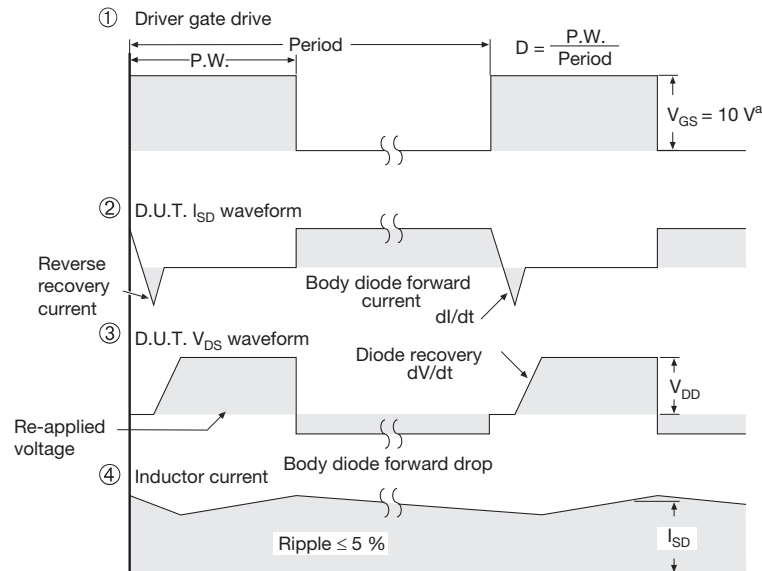
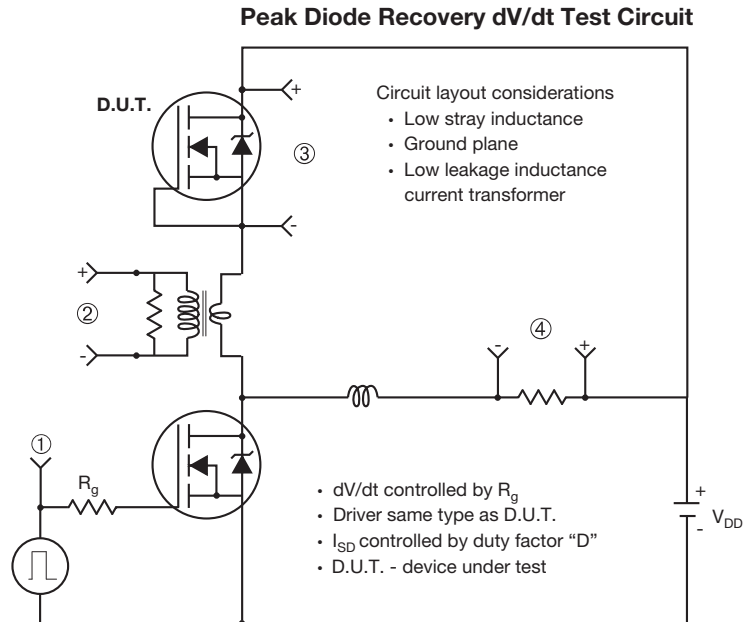


Fig. 13b - Gate Charge Test Circuit



Note

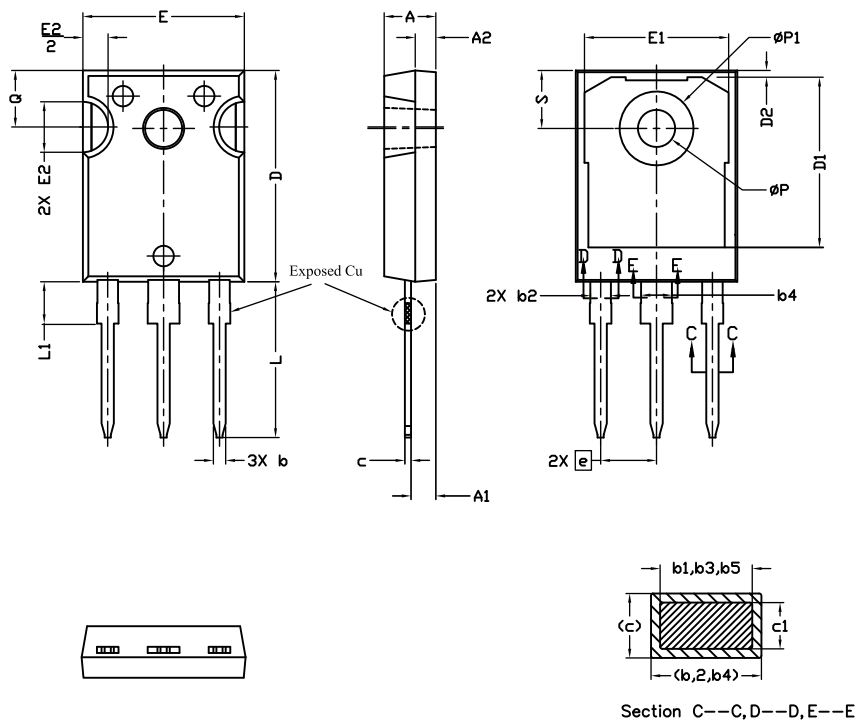
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91254.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9


Section C---C, D---D, E---E

MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

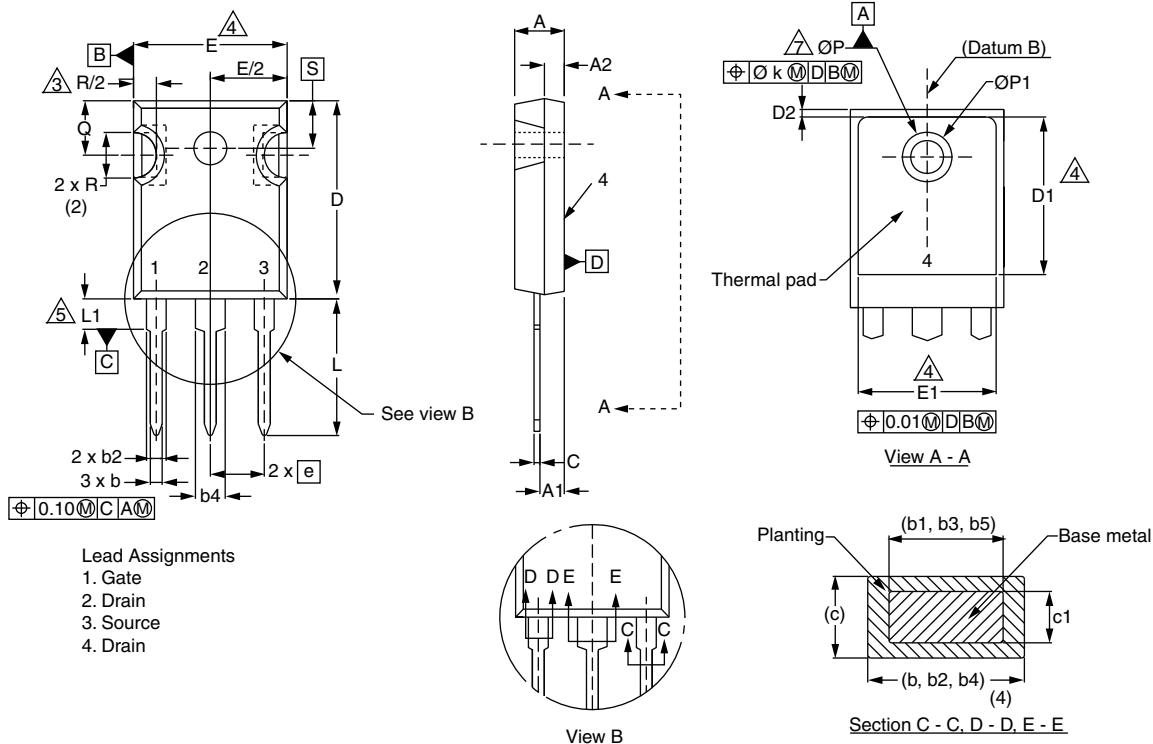
MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

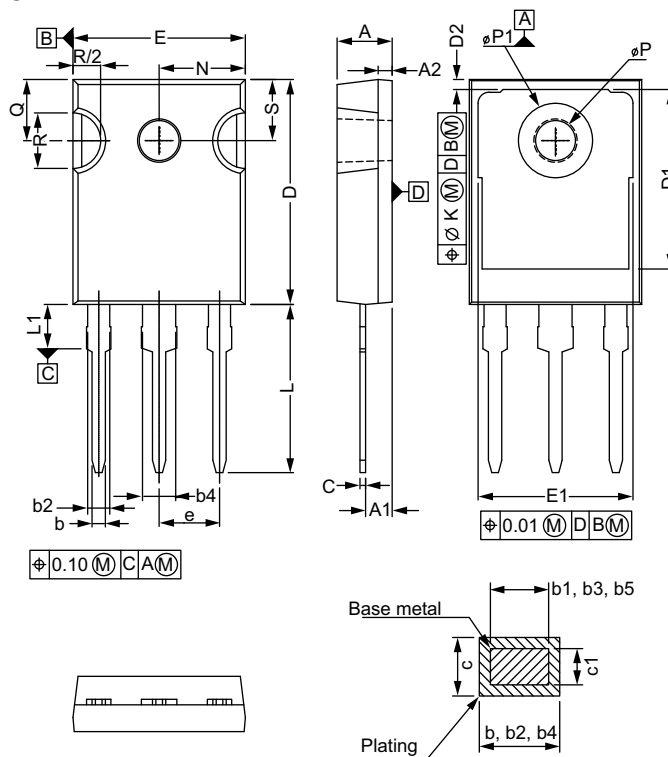
DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E20-0545-Rev. F, 19-Oct-2020
DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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