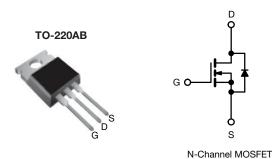


Power MOSFET



PRODUCT SUMMAI	RY	
V _{DS} (V)	40	00
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.55
Q _g max. (nC)	6	3
Q _{gs} (nC)	9.	.0
Q _{gd} (nC)	3	2
Configuration	Sin	ale

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF740PbF
Lead (Pb)-free and halogen-free	IRF740PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	400		
Gate-source voltage		V_{GS}	± 20	V		
Continuous drain current	V at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	1	10		
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	6.3	Α	
Pulsed drain current ^a			I _{DM}	40		
Linear derating factor				1.0	W/°C	
Single pulse avalanche energy ^b			E _{AS}	520	mJ	
Repetitive avalanche current a			I _{AR}	10	А	
Repetitive avalanche energy ^a	Repetitive avalanche energy ^a		E _{AR}	13	mJ	
Maximum power dissipation $T_C = 25 ^{\circ}C$		25 °C	P_{D}	125	W	
Peak diode recovery dV/dt ^c			dV/dt	4.0	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For 10 s			300		
Maria Para Laura	6 20 0 1	0.00 - 140		10	lbf ⋅ in	
Mounting torque	6-32 or M3 screw			1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 9.1 mH, R_g = 25 Ω , I_{AS} = 10 A (see fig. 12)
- c. $I_{SD} \le 10$ A, $dI/dt \le 120$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case

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THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	1.0	

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static		•				•	•
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		400	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.49	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V$	' _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _G	_{iS} = ± 20 V	-	-	± 100	nA
	I _{DSS}	$V_{DS} = 4$	V _{DS} = 400 V, V _{GS} = 0 V		-	25	μA
Zero gate voltage drain current		V _{DS} = 320 V, \	V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 6.0 \text{ A}^{\text{ b}}$	-	-	0.55	Ω
Forward transconductance	9 _{fs}	V _{DS} = 5	0 V, I _D = 6.0 A ^b	5.8	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	1400	-	
Output capacitance	C _{oss}	V _I	$_{DS} = 25 \text{ V},$	-	330	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0	MHz, see fig. 5	-	120	-	
Total gate charge	Qg		I _D = 10 A, V _{DS} = 320 V, see fig. 6 and 13 ^b	-	-	63	nC
Gate-source charge	Q _{gs}	V _{GS} = 10 V		-	-	9.0	
Gate-drain charge	Q_{gd}			-	-	32	
Turn-on delay time	t _{d(on)}			-	14	-	
Rise time	t _r	V_{DD} = 200 V, I_{D} = 10 A R_{g} = 9.1 Ω , R_{D} = 20 Ω , see fig. 10 b		-	27	-	ns
Turn-off delay time	t _{d(off)}			-	50	-	
Fall time	t _f			-	24	-	
Gate input resistance	Rg	f = 1 MHz, open drain		0.8	-	5.9	Ω
Internal drain inductance	L _D	6 mm (0.25") f	Between lead, 6 mm (0.25") from		4.5	-	-11
Internal source inductance	L _S	package and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristic	es	<u>.</u>					
Continuous source-drain diode current	I _S	showing th	MOSFET symbol showing the		-	10	A
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	40	
Body diode voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 10 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	- T _J = 25 °C, I _F = 10 A, dl/dt = 100 A/μs b		-	370	790	ns
Body diode reverse recovery charge	Q _{rr}			-	3.8	8.2	μC
Forward turn-on time	t _{on}	Intrinsic turn	-on time is negligible (turr	on is do	minated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

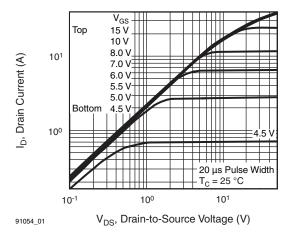


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

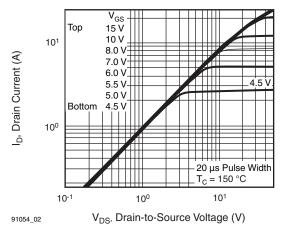


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

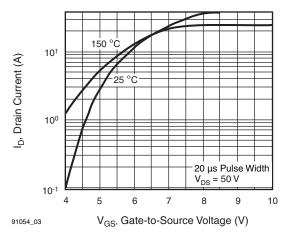


Fig. 3 - Typical Transfer Characteristics

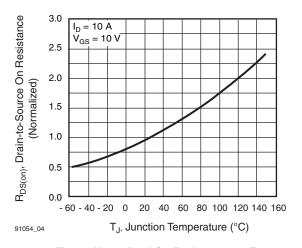


Fig. 4 - Normalized On-Resistance vs. Temperature

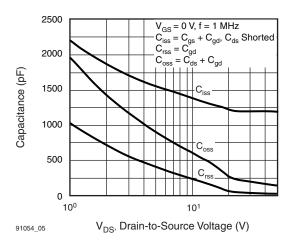


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

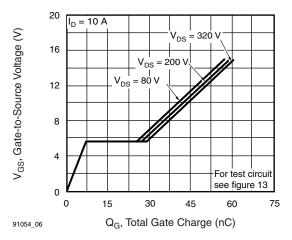


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage



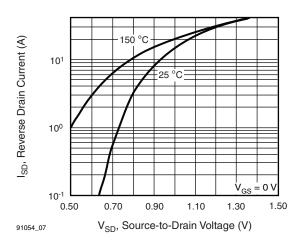


Fig. 7 - Typical Source-Drain Diode Forward Voltage

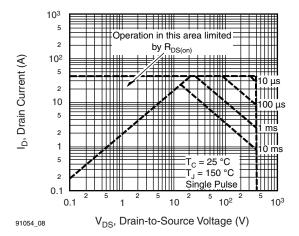


Fig. 8 - Maximum Safe Operating Area

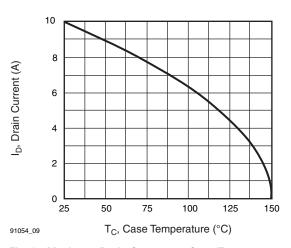


Fig. 9 - Maximum Drain Current vs. Case Temperature

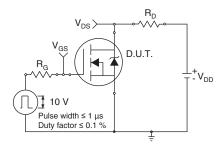


Fig. 10a - Switching Time Test Circuit

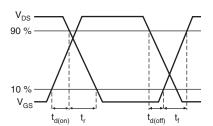


Fig. 10b - Switching Time Waveforms

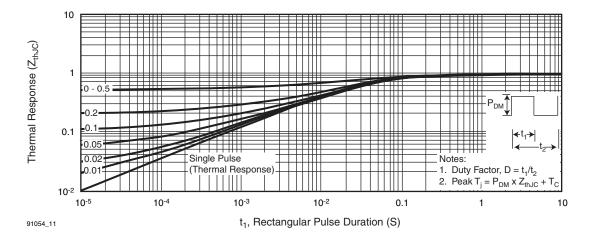
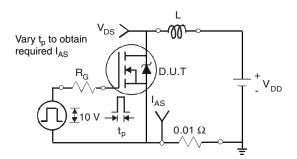
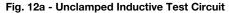




Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case





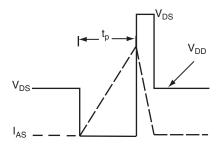


Fig. 12b - Unclamped Inductive Waveforms

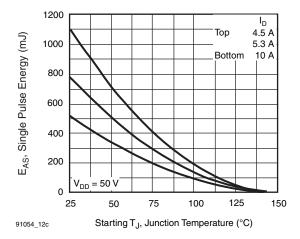


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

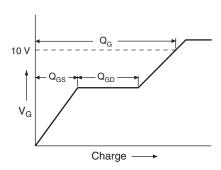


Fig. 13a - Basic Gate Charge Waveform

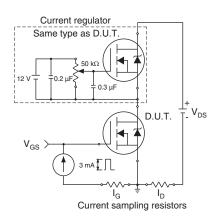
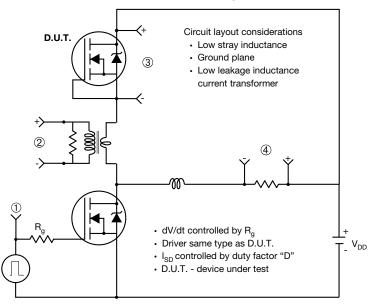


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



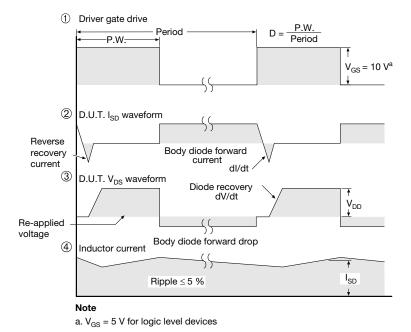


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIM	METERS	INCHE	HES
	MIN.	MAX.	MIN.	MAX.
Α	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
С	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
Е	9.96	10.52	0.392	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
ØP	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

Note

DWG: 6031

• $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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