DRV401-Q1 Sensor Signal Conditioning Device for Closed-Loop Magnetic Current Sensor

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C6
- Single-Supply: 5-V
- Power Output: H-Bridge
- Designed for Driving Inductive Loads
- Excellent DC Precision
- Wide System Bandwidth
- High-Resolution, Low-Temperature Drift
- Built-In Degauss System
- Extensive Fault Detection
- External High-Power Driver Option
- Compact Footprint

2 Applications

- Automotive
- Motor Control in Automotive Applications
- Flux Gate Current Sensing
- Generator and Alternator Monitoring and Control
- Frequency and Voltage Inverters
- Motor Drive Controllers
- System Power Consumption
- Photovoltaic Systems

3 Description

The DRV401-Q1 device is fully qualified for automotive applications and is suitable for motor control drive and battery monitoring systems.

When used with a magnetic sensor, the DRV401-Q1 monitors ac and dc currents to high accuracy.

Provided functions include: probe excitation, signal conditioning of the probe signal, signal loop amplifier, an H-bridge driver for the compensation coil, and an analog signal output stage that provides an output voltage proportional to the primary current. It offers overload and fault detection, as well as transient noise suppression.

The DRV401-Q1 device directly drives the compensation coil or connects to external power drivers. Therefore, the DRV401-Q1 combines with sensors to measure small to large currents.

To maintain the highest accuracy, the DRV401-Q1 demagnetizes (degausses) the sensor at power-up and on demand.

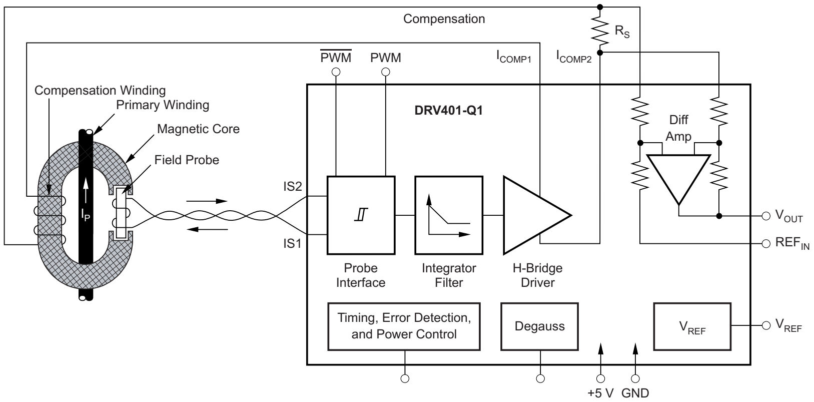
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV401-Q1	VQFN-20	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Closed-Loop Magnetic Sensing

Patents Pending



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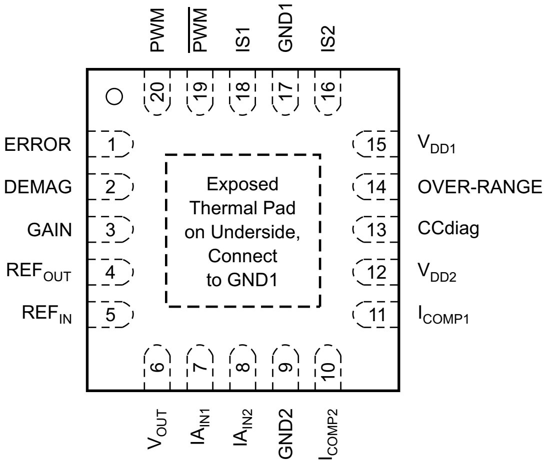
4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Pin Configuration and Functions

RGW Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CCdiag	13	I	Control input for wire-break detection: high = enable
DEMAG	2	I	Control input; See the *Demagnetization* section.
ERROR	1	O	Error flag: open-drain output. See the *Error Conditions* section.
GAIN	3	I	Control input for open-loop gain: low = normal, high = −8 dB
GND1	17	—	Ground connection
GND2	9	—	Ground connection. Connect to GND1.
IA_{IN1}	8	I	Inverting input of differential amplifier
IA_{IN2}	7	I	Noninverting input of differential amplifier
I_{COMP1}	11	O	Output 1 of compensation coil driver
I_{COMP2}	10	O	Output 2 of compensation coil driver
IS1	18	I/O	Probe connection 1
IS2	16	I/O	Probe connection 2
OVER-RANGE	14	O	Open-drain output for overrange indication: low = overrange
$\overline{PWM}$	19	O	PWM output from probe circuit (inverted)
PWM	20	O	PWM output from probe circuit
REF_{OUT}	4	O	Output for internal 2.5-V reference voltage
REF_{IN}	5	I	Input for zero reference to differential amplifier
Thermal pad	—	—	Exposed thermal pad. Connect to GND1.
V_{DD1}	15	—	Supply voltage
V_{DD2}	12	—	Supply voltage. Connect to V_{DD1}.
V_{OUT}	6	O	Output for differential amplifier

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pin	−0.5	V_{DD} + 0.5	
Differential amplifier	Signal input pin	–10	10	
Current	Signal input pin, IS1 and IS2	–75	75	mA
	Pins other than IS1 and IS2	–25	25	
	I_{COMP} short circuit	0	250	
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	Pins IA_{IN1} and IA_{IN2}	±1000	V
			All other pins	±5000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Power supply voltage, V_{DD1}, V_{DD2}	4.5	5	5.5	V
Specified temperature range	–40	25	+125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		DRV401-Q1	UNIT
		RGW (VQFN)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL AMPLIFIER						
V_{OS}	Offset voltage, RTO(1)(2)	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V Gain = 4 V/V		±0.01	±0.1	mV
dV_{OS}/dT	Offset voltage drift, RTO(2)	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C I_{COMP} = 0 mA		±0.1	±1	µV/°C
CMRR	Offset voltage vs common-mode, RTO	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V −1 V to 6 V, V_{REF} = 2.5 V		±50	±250	µV/V
PSRR	Offset voltage vs power supply, RTO	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{REF} not included		±4	±50	µV/V
SIGNAL INPUT						
	Common-mode voltage range	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	–1		(V_{DD}) + 1	V
SIGNAL OUTPUT						
	Signal overrange indication (OVER-RANGE), delay(2)	R_L = 10 kΩ to 2.5 V, V_{REFIN} = 2.5 V, T_A = –40°C to 125°C, I_{COMP} = 0 mA, V_{IN} = 1-V step. See (2)		2.5 to 3.5		µs
	Voltage output swing from negative rail(2), OVER-RANGE trip level	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V I = 2.5 mA, CMP trip level		48	85	mV
	Voltage output swing from positive rail(2), OVER-RANGE trip level	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V I = −2.5 mA, CMP trip level	V_{DD} – 85	V_{DD} – 48		mV
I_{SC}	Short-circuit current(2)	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{OUT} connected to GND		–18		mA
		R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{OUT} connected to V_{DD}		20		mA
	Gain, V_{OUT}/V_{IN_DIFF}	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C		4		V/V
	Gain error	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V		±0.02%	±0.3%	
	Gain error drift	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C I_{COMP} = 0 mA		±0.1		ppm/°C
	Linearity error	V_{REFIN} = 2.5 V R_L = 1 kΩ		10		ppm
FREQUENCY RESPONSE						
$BW_{-3\ dB}$	Bandwidth(2)	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V		2		MHz
SR	Slew rate(2)	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V CMVR = −1 V to 4 V		6.5		V/µs

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(1) Parameter value referred-to-output (RTO).
(2) θ_{JP} = junction-to-pad thermal resistance

Electrical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time, large-signal[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V dV ±2 V to 1%, no external filter		0.9		µs
	Settling time[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V dV ±0.4 V to 0.01%		14		µs
INPUT RESISTANCE						
	Differential	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	16.5	20	23.5	kΩ
	Common-mode	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	41	50	59	kΩ
	External reference input	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	41	50	59	kΩ
NOISE						
e_n	Output voltage noise density, RTO[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V f = 1 kHz, compensation loop disabled		170		nV/√Hz
COMPENSATION LOOP						
DC STABILITY						
	Offset error [3]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, deviation from 50% PWM, pin gain = L		0.03%		
	Offset error drift [2]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, deviation from 50% PWM, pin gain = L, T_A = –40°C to 125°C		7.5		ppm/°C
	Gain [2]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, pin gain = L, $\lvert V_{ICOMP1}\rvert - \lvert V_{ICOMP2}\rvert$	–200	25	200	ppm/V
PSRR	Power-supply rejection ratio	Probe f = 250 kHz, R_{LOAD} = 20 Ω		500		ppm/V
FREQUENCY RESPONSE						
	Open-loop gain	Probe f = 250 kHz, R_{LOAD} = 20 Ω, two modes, 7.8 kHz		24/32		dB
PROBE COIL LOOP						
	Input voltage clamp range	Field probe current < 50 mA	–0.7 to V_{DD} + 0.7	V		
R_{HIGH}	Internal resistor, IS1 or IS2 to V_{DD1} [2]		47	59	71	Ω
R_{LOW}	Internal resistor, IS1 or IS2 to GND1 [2]		60	75	90	Ω
	Resistance mismatch between IS1 and IS2 [2]	ppm of R_{HIGH} + R_{LOW}		300	1500	ppm
	Total input resistance	T_A = –40°C to 125°C I_{COMP} = 0 mA		134	200	Ω
	Comparator threshold current		22	28	34	mA
	Minimum probe loop half-cycle [2]		250	280	310	ns
	Probe loop minimum frequency		250			kHz
	No oscillation detect (error) suppression			35		µs
COMPENSATION COIL DRIVER, H-BRIDGE						
	Peak current [2]	$V_{ICOMP1} - V_{ICOMP2}$ = 4 V_{PP} T_A = –40°C to 125°C I_{COMP} = 0 mA		250		mA
	Voltage swing	20-Ω load	4.2			V_{PP}

(3) For VAC sensors, 0.2% of PWM offset approximately corresponds to 10-mA primary current per offset per winding.

Electrical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCM}	Output common-mode voltage			V_{DD2} / 2		V
	Wire break detect, threshold current [4]			33	57	mA
VOLTAGE REFERENCE						
	Voltage [2]	No load	2.495	2.5	2.505	V
	Voltage drift [2]	No load, T_A = – 40°C to 125°C I_{COMP} = 0 mA		±5	±50	ppm/°C
PSRR	Power-supply rejection ratio[2]			±15	±200	µV/V
	Load regulation[2]	Load to GND and V_{DD} dI = 0 mA to 5 mA		0.15		mV/mA
I_{SC}	Short-circuit current	REF_{OUT} connected to V_{DD}		20		mA
		REF_{OUT} connected to GND		–18		mA
DEMAGNETIZATION						
	Duration	At T_A = –40°C to 125°C I_{COMP} = 0 mA; see the *Demagnetization* section		106	130	ms
DIGITAL I/O						
LOGIC INPUTS (DEMAG, GAIN, and CCdiag PINS)						
	Pull-up high current (CCdiag)	CMOS-type levels, 3.5 < V_{IN} < V_{DD}		160		µA
	Pull-up low current (CCdiag)	CMOS-type levels, 0 < V_{IN} < 1.5		5		µA
	Logic input leakage current	CMOS-type levels, 0 < V_{IN} < V_{DD}		0.01		µA
	Logic level, input: L/H	CMOS-type levels		2.1/2.8		
	Hysteresis	CMOS-type levels		0.7		
OUTPUTS (ERROR AND OVER-RANGE PINS)						
	Logic level, output: L	4-mA sink		0.3		V
	Logic level, input: H			No internal pull-up		
OUTPUTS (PWM AND $\overline{\text{PWM}}$ PINS)						
	Logic level L	Push-pull type, 4-mA sink		0.2		V
	Logic level H	Push-pull type, 4-mA source		V_{DD} – 0.4		V
POWER SUPPLY						
V_{DD}	Specified voltage range	T_A = –40°C to 125°C I_{COMP} = 0 mA	4.5	5	5.5	V
V_{RST}	Power-on reset threshold			1.8		V
I_Q	Quiescent current [$I(V_{DD1})$ + $I(V_{DD2})$]	I_{COMP} = 0 mA, sensor not connected			6.8	mA
	Brownout voltage level			4		V
	Brownout indication delay			135		µs
TEMPERATURE RANGE						
T_J	Specified range		–40		125	°C
T_J	Operating range		–50		150	°C

(4) See the *Compensation Driver* subsection in the *Detailed Description* section.

6.6 Typical Characteristics

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

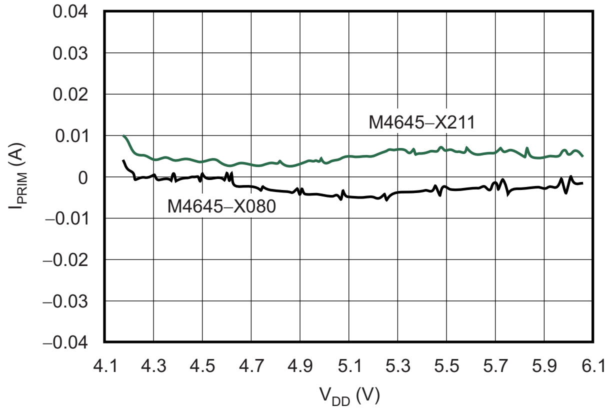
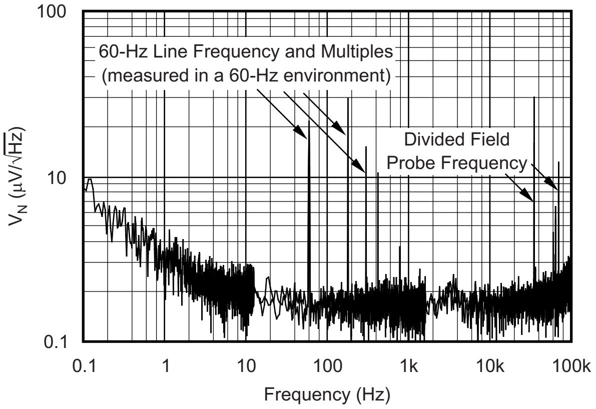


Figure 1. DRV401-Q1 Device and Sensor: Offset vs Supply Voltage



Sensor M4645−X080, R_{SHUNT} = 10 Ω, Mode = Low

Figure 2. DRV401-Q1 Device and Sensor: Output Voltage Noise Density

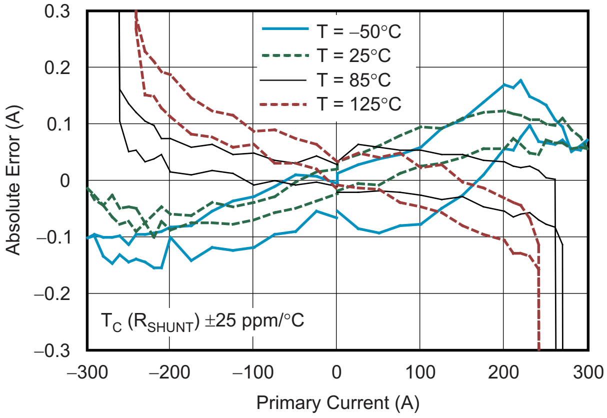
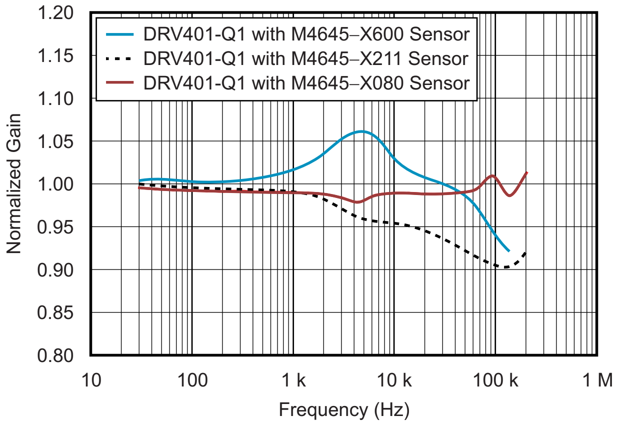
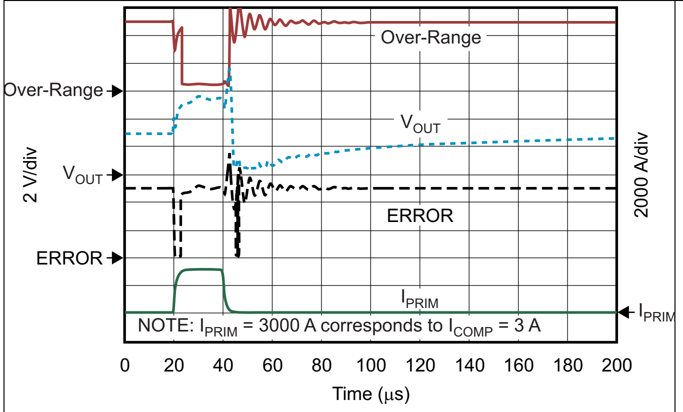


Figure 3. DRV401-Q1 Device and Sensor: Absolute Error



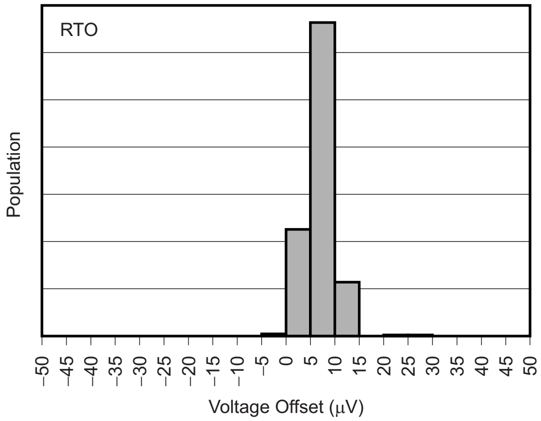
Soldered DWP−20 with 1-in^2 copper pad. Measurements by Vacuumschmelze GmbH.

Figure 4. Gain Flatness vs Frequency



Measurements by Vacuumschmelze GmbH.

Figure 5. 3-A I_{COMP} Overload Recovery



Measurements by Vacuumschmelze GmbH.

Figure 6. Differential Amplifier: Voltage Offset Production Distribution

Typical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

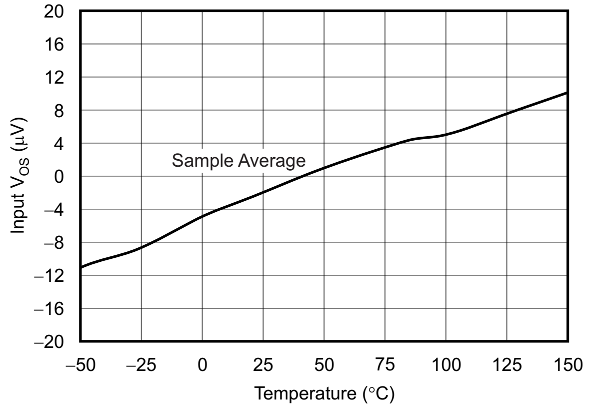


Figure 7. Differential Amplifier: Offset Voltage vs Temperature, RTO

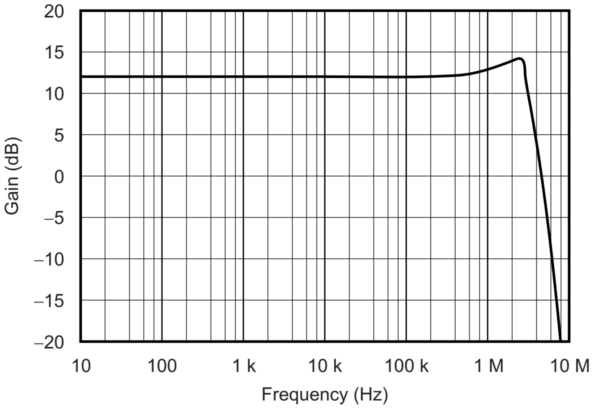


Figure 8. Differential Amplifier: Gain vs Frequency

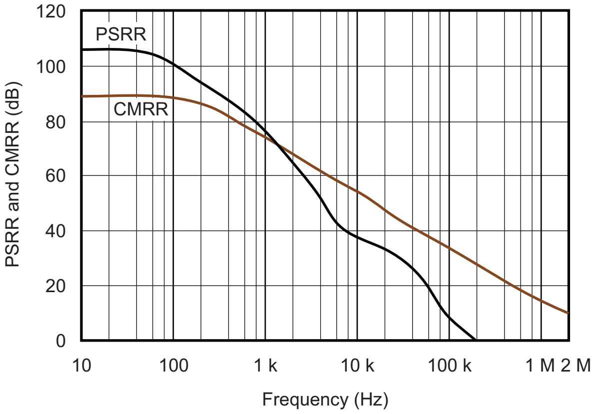


Figure 9. Differential Amplifier: PSRR and CMRR vs Frequency

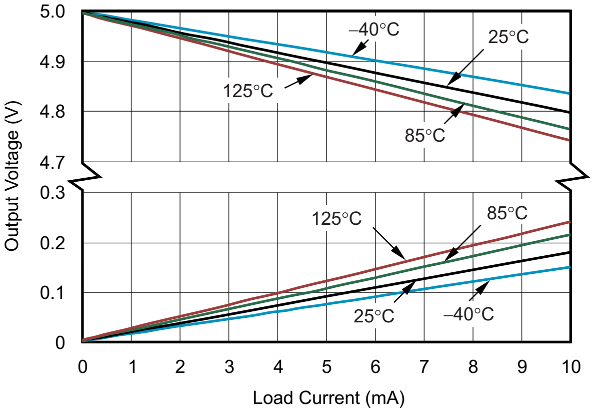


Figure 10. Differential Amplifier: Output Voltage vs Output Current

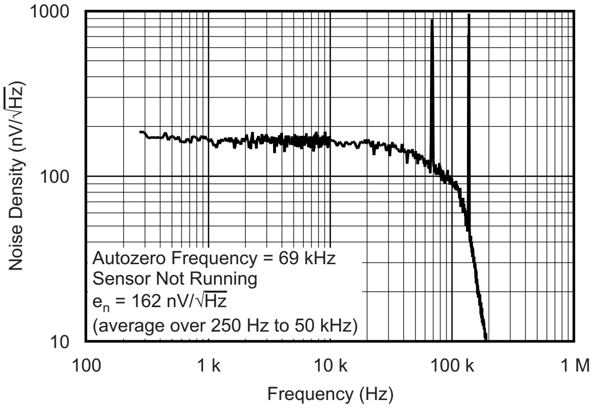


Figure 11. Differential Amplifier: Output Noise Density

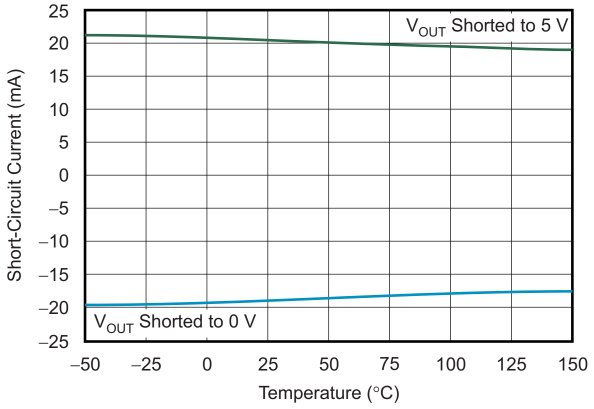


Figure 12. Differential Amplifier: Short-Circuit Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

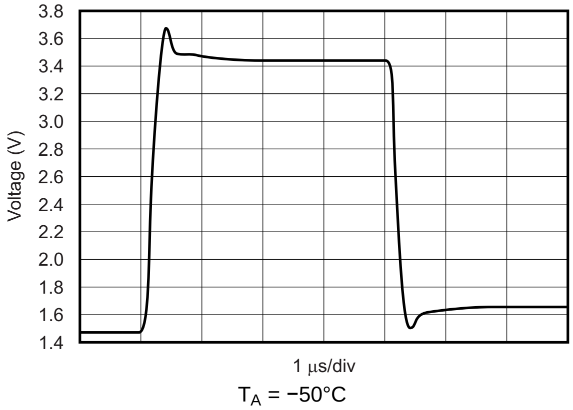


Figure 13. Differential Amplifier: Large-Signal Step Response

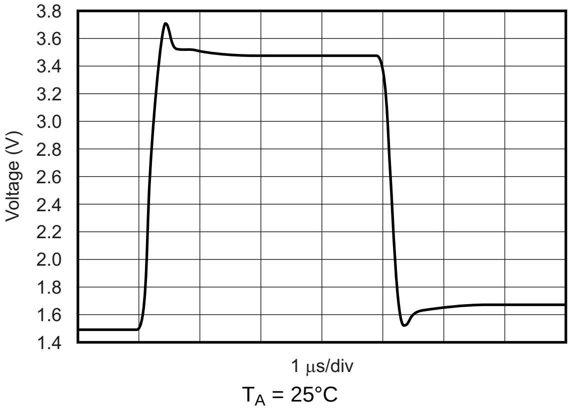


Figure 14. Differential Amplifier: Large-Signal Step Response

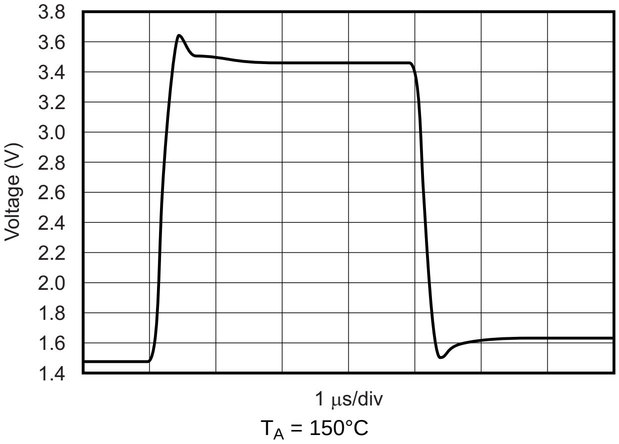


Figure 15. Differential Amplifier: Large-Signal Step Response

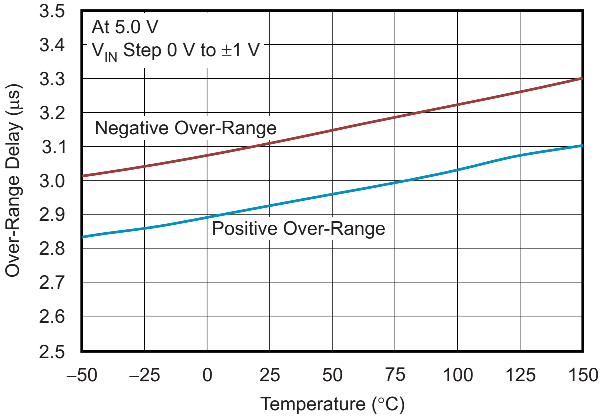


Figure 16. Differential Amplifier: Overrange Delay vs Temperature

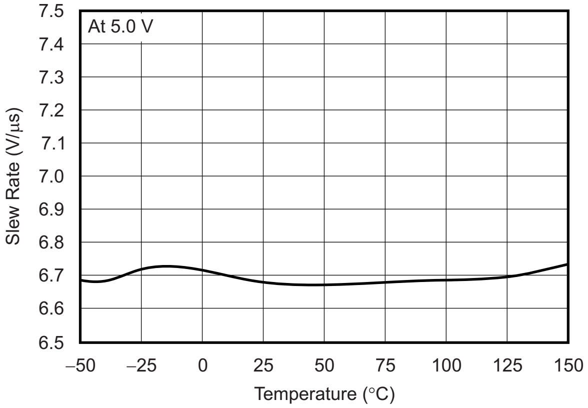


Figure 17. Differential Amplifier: Positive Slew Rate vs Temperature

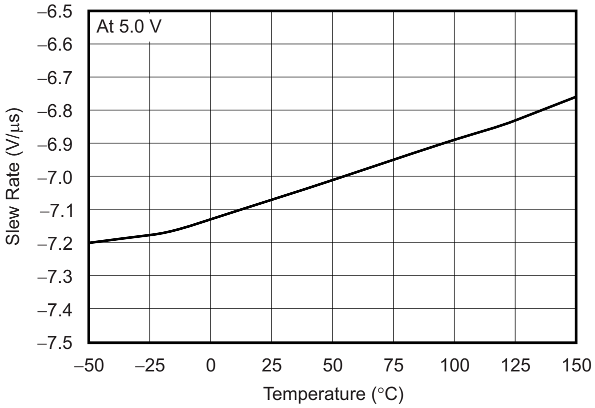


Figure 18. Differential Amplifier: Negative Slew Rate vs Temperature

Typical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

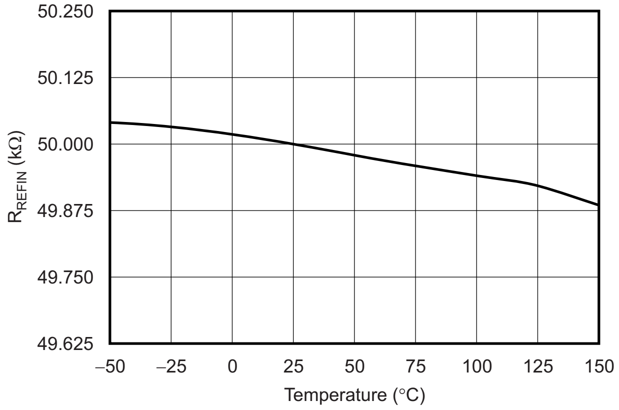


Figure 19. Differential Amplifier: REF_{IN} Resistance vs Temperature

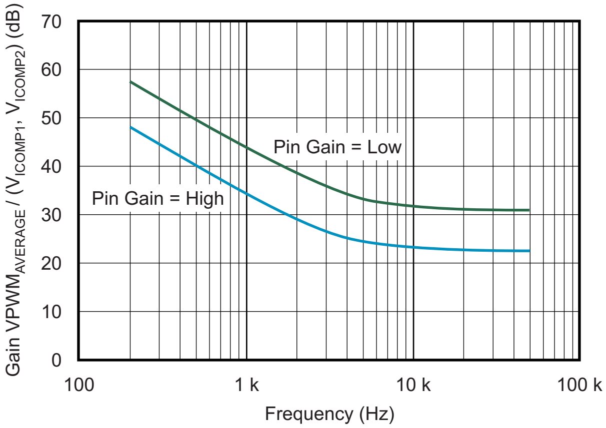


Figure 20. Compensation Loop: Small-Signal Gain

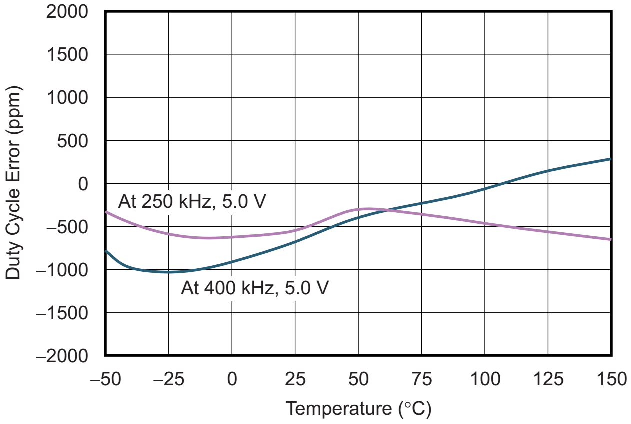


Figure 21. Compensation Loop: Duty Cycle Error vs Temperature

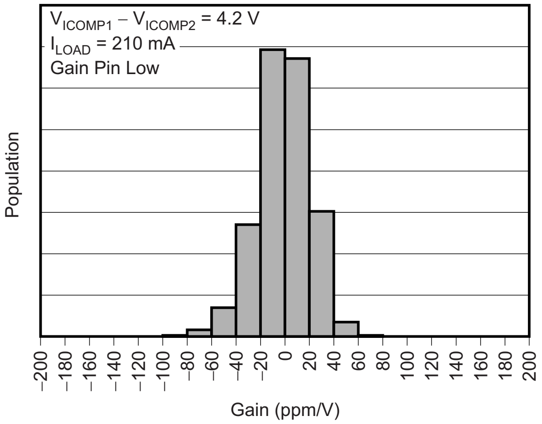


Figure 22. Compensation Loop: DC Gain: Duty Cycle Error Change

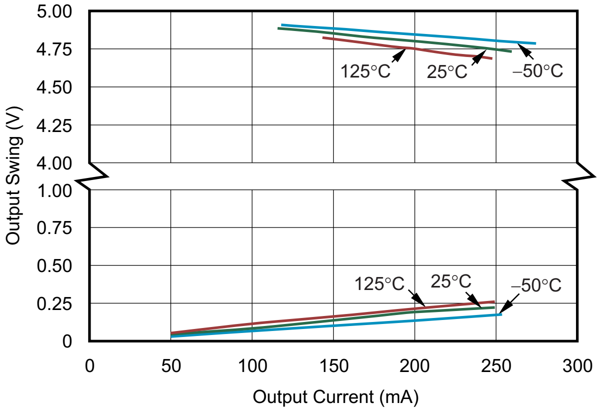


Figure 23. I_{COMP} Output Swing to Rail vs Output Current

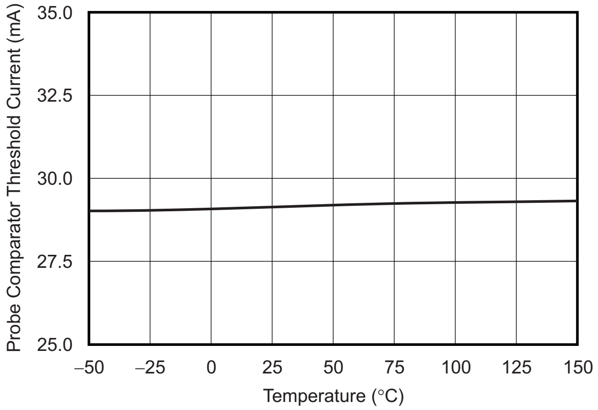


Figure 24. Probe Comparator Threshold Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

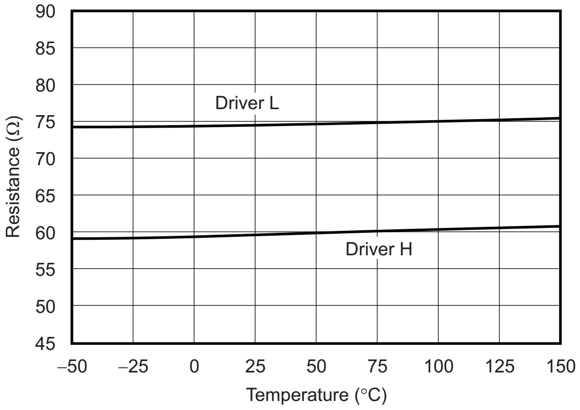


Figure 25. Probe Driver: Internal Resistor vs Temperature

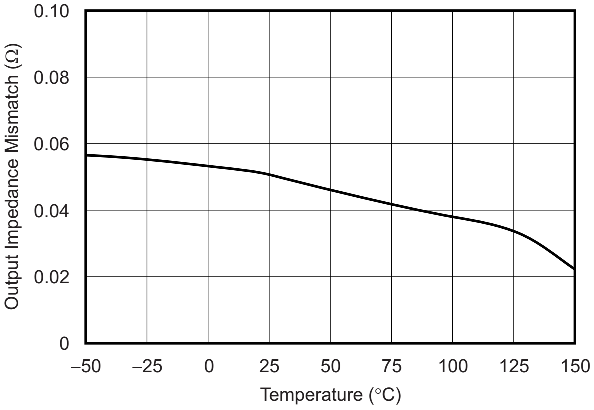


Figure 26. Output Impedance Mismatch of IS1 and IS2 vs Temperature

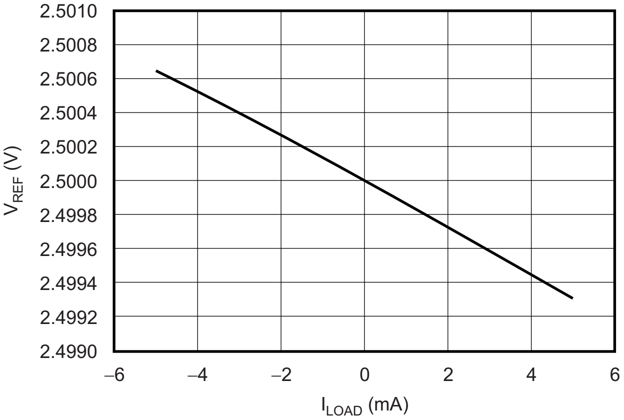


Figure 27. Voltage Reference vs Load Current

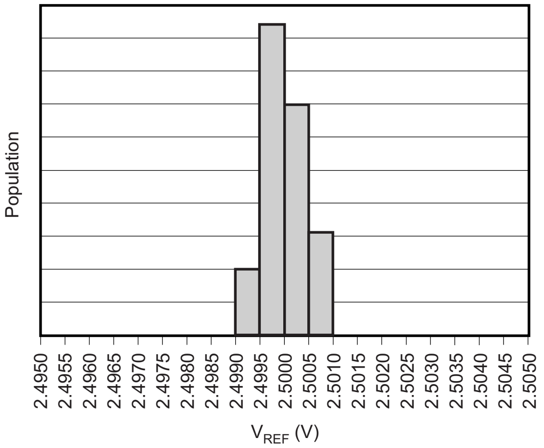


Figure 28. Voltage Reference Production Distribution

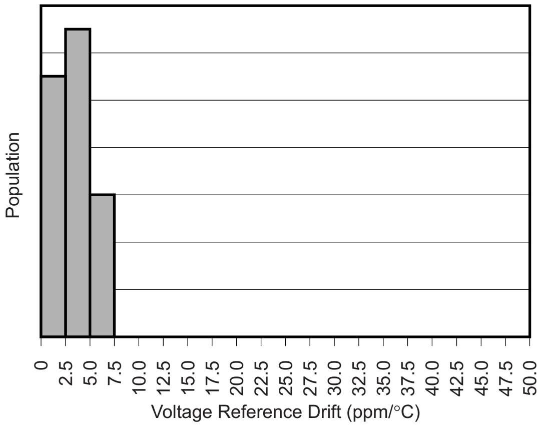


Figure 29. Voltage Reference Drift Production Distribution

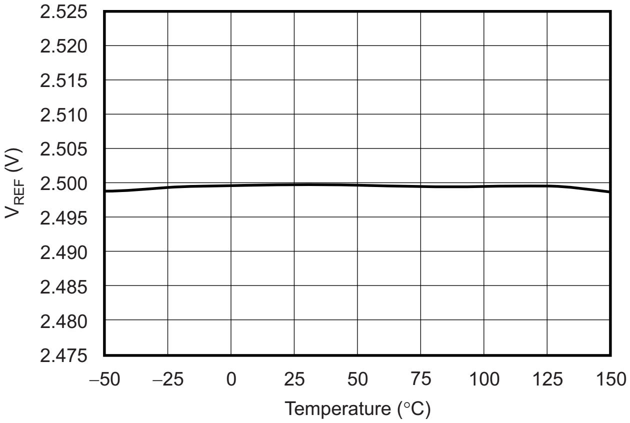


Figure 30. Voltage Reference vs Temperature

Typical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

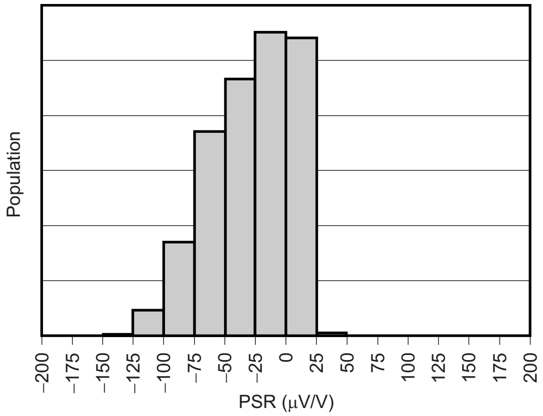


Figure 31. Voltage Reference Power-Supply Rejection Production Distribution

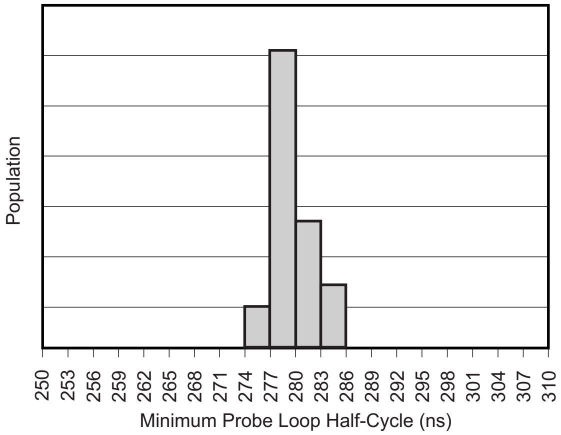


Figure 32. Oscillator Production Distribution

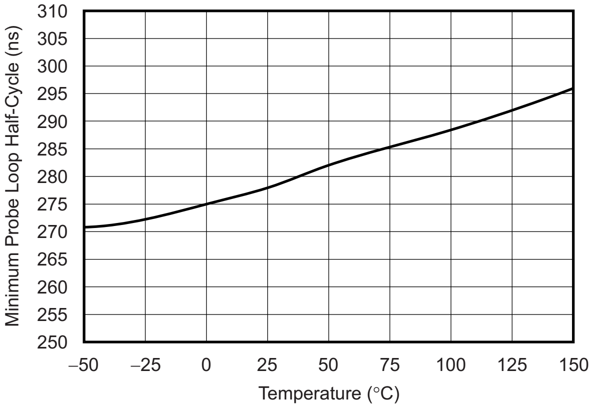


Figure 33. Oscillator vs Temperature

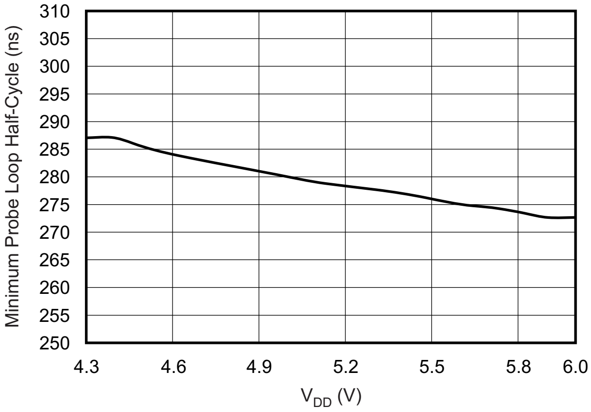


Figure 34. Oscillator vs Supply Voltage

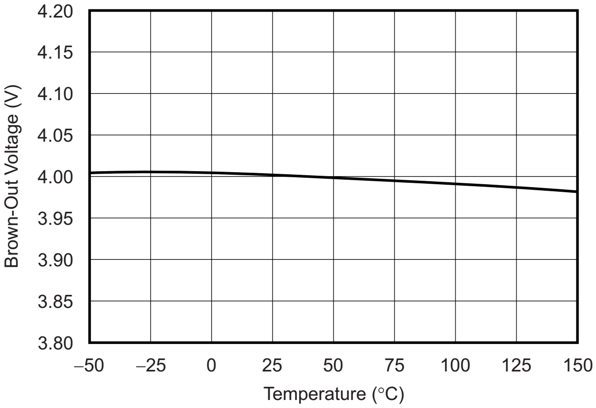


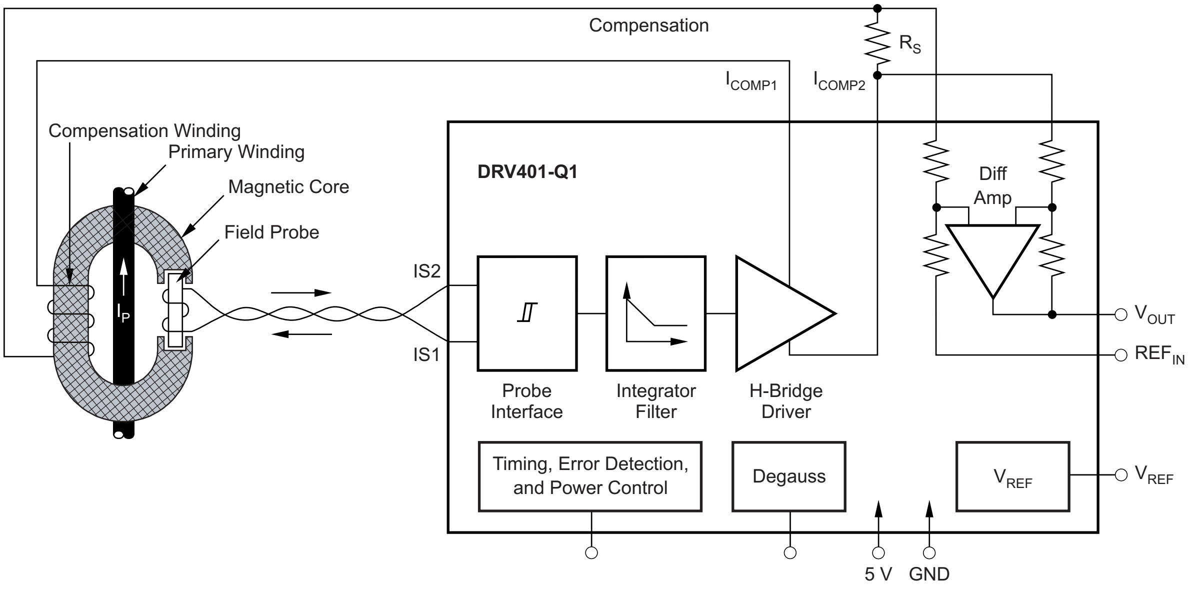
Figure 35. Brownout Voltage vs Temperature

7 Detailed Description

7.1 Overview

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method, as well as excellent galvanic isolation performance combined with high resolution, accuracy, and reliability. The DRV401-Q1 is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation.

7.2 Functional Block Diagram



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7.3 Feature Description

The DRV401-Q1 operates from a single 5-V supply. The DRV401-Q1 is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation. The DRV401-Q1 device provides magnetic field probe excitation, signal conditioning, and compensation coil driver amplification. In addition, the device detects error conditions and handles overload situations. A precise differential amplifier allows translation of the compensation current into an output voltage using a small shunt resistor. A buffered voltage reference is used for comparator, analog-to-digital converter (ADC), or bipolar zero reference voltages.

Dynamic error correction ensures high dc precision over temperature and long-term accuracy. The DRV401-Q1 uses analog signal conditioning, and the internal loop filter and integrator are switched capacitor-based circuits. Therefore, the DRV401-Q1 device allows combination with high-precision sensors for exceptional accuracy and resolution.

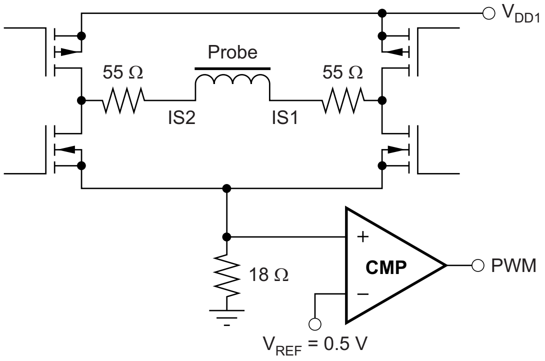
A demagnetization cycle initiates on demand or on power-up. The cycle reduces offset and restores high performance after a strong overload condition. An internal clock and counter logic generate the degauss function. The same clock controls power-up, overload detection and recovery, error, and time-out conditions.

The DRV401-Q1 device is built on a highly reliable CMOS process. Unique protection cells at critical connections enable the design to handle inductive energy.

7.3.1 Magnetic Probe (Sensor) Interface

The magnetic field probe consists of an inductor wound on a soft magnetic core. The probe is connected between pins IS1 and IS2 of the probe driver that applies approximately 5 V (the supply voltage) through resistors across the probe coil, as shown in Figure 36.

Typically, the probe core reaches saturation at a current of 28 mA, as shown in Figure 36. The comparator is connected to V_{REF} by approximately 0.5 V. A current comparator detects the saturation and inverts the excitation voltage polarity, causing the probe circuit to oscillate in a frequency range of 250 kHz to 550 kHz. The oscillating frequency is a function of the magnetic properties of the probe core and the coil.



NOTE: MOS components function as switches only.

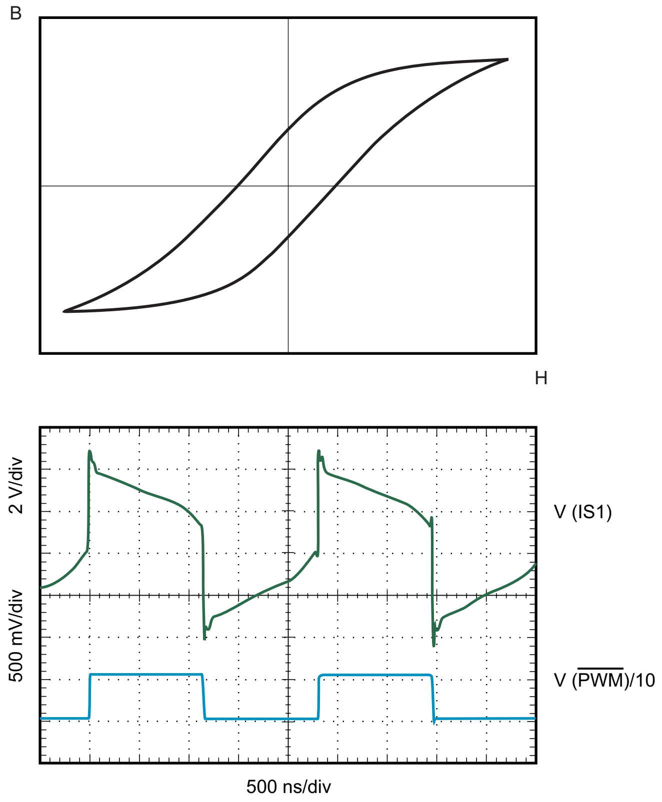
The probe is connected between S1 and S2.

Figure 36. Magnetic Probe, Hysteresis, and Duty Cycle: Simplified Probe Circuit

The current rise rate is a function of the coil inductance: dI = L × V × dT. However, the inductance of the field probe is low while the core material is in saturation (the horizontal part of the hysteresis curve) and is high at the vertical part of the hysteresis curve. The resulting inductance and the series resistance determine the output voltage and current versus time performance characteristic.

Feature Description (continued)

Without external magnetic influence, the duty cycle is exactly 50% because of the inherent symmetry of the magnetic hysteresis; the probe inductor is driven from −B saturation through the high inductance range to +B saturation and back again in a time-symmetric manner, as shown in Figure 37.

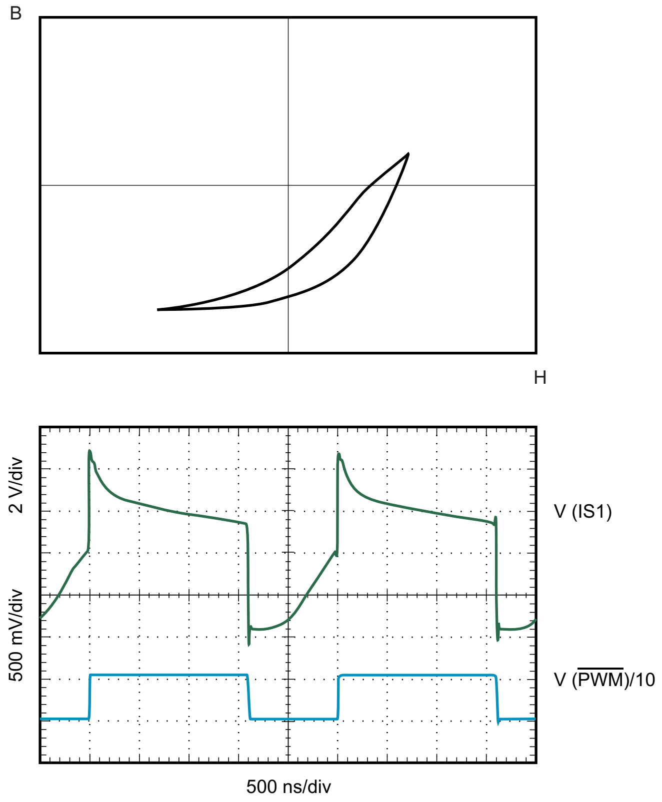


Without an external magnetic field, the hysteresis curve is symmetrical and the probe loop generates 50% duty cycle.

Figure 37. Magnetic Probe, Hysteresis, and Duty Cycle: No External Magnetic Field

Feature Description (continued)

If the core material is magnetized in one direction, a long and a short charge time result because the probe current through the inductors generates a field that subtracts or adds to the flux in the probe core, driving the probe core out of saturation or further into saturation, as shown in Figure 38. The current into the probe is limited by the voltage drops across the probe driver resistors.



An external magnetic flux (H) generated from the primary current (I_{PRIM}) shifts the hysteresis curve of the magnetic field probe in the H-axis and the probe loop generates a nonsymmetrical duty cycle.

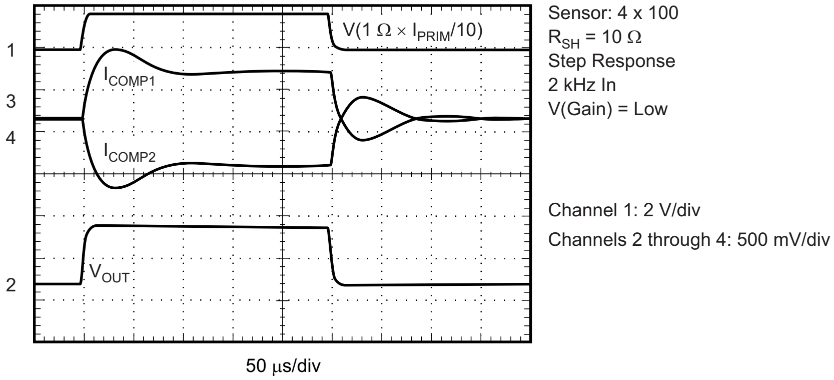
Figure 38. Magnetic Probe, Hysteresis, and Duty Cycle With External Magnetic Field

The DRV401-Q1 device continuously monitors the logic magnetic flux polarity state. In the case of distortion noise and excessive overload that can fully saturate the probe, the overload control circuit recovers the probe loop. During an overload condition, the probe oscillation frequency increases to approximately 1.6 MHz until limited by the internal timing control.

In an overload condition, the compensation current (I_{COMP}) driver cannot deliver enough current into the sensor secondary winding, so the magnetic flux in the sensor main core becomes uncompensated.

Feature Description (continued)

The transition from normal operation to overload happens slowly because the inherent sensor transformer characteristics induce the initial primary current step, as shown in Figure 39. As the transformer-induced secondary current starts to decay, the compensation feedback driver increases the output voltage to maintain the sensor core flux compensation at zero.



A current pulse of 0 A to 18 A (channel 1) generates the two I_{COMP} signals (channel 3 and channel 4). Channel 2 shows the resulting output signal (V_{OUT}). This test uses the M4645-X030 sensor with no bandwidth limitation, and a 20-sample average.

Figure 39. Primary Current Step Response

When the system compensation loop reaches the driving limit, the rising magnetic flux causes one of the probe pulse-width modulator (PWM) half-periods to become shorter. The minimum half-period of the probe oscillation is limited by the internal timing to 280 ns, based on the properties of the VAC magnetic sensors. After three consecutive cycles of the same half-period being shorter than 280 ns, the DRV401-Q1 device enters overload-latch mode. The device stores the I_{COMP} driver output signal polarity and continues producing the skewed-duty cycle PWM signal. This action prevents the loss of compensation signal polarity information during strong overloads. In this case, both PWM half-periods are short and approximately equal, because the field probe stays completely in one of the saturated regions.

The overload-latch condition is removed after the primary current goes low enough for the I_{COMP} driver to compensate, and both half-periods of the probe driver oscillation become longer than 280 ns (the field probe comes out of the saturated region).

Peak voltages and currents generate during normal operations and overload conditions. Both probe connection pins are internally protected against coupled energy from the magnetic core. Wiring between probe and device inputs must be short and guarded against interference, as shown in the *Layout Guidelines* section.

For reliable operation, error detection circuits monitor the probe operation:

1. If the probe driver comparator (CMP) output stays low longer than 32 µs, the ERROR flag asserts active, and the compensation current (I_{COMP}) is set to zero.
2. If the probe driver period is less than 275 ns on three consecutive pulses, the ERROR flag asserts active.

See the *Error Conditions* section for more details.

7.3.2 PWM Processing

The PWM and $\overline{\text{PWM}}$ outputs represent the probe output signal as a differential PWM signal. The signal drives external circuitry and is used for synchronous ripple reduction. The PWM signal from the probe excitation and sense stage is internally connected to a high-performance, switched-capacitor integrator followed by an integrating-differentiating filter. The filter converts the PWM signal into a filtered delta signal and prepares the PWM signal to drive the analog compensation coil driver. The gain roll-off frequency of the filter stage provides high dc gain and loop stability. If additional gain is added from external circuitry, the internal gain is reduced by 8 dB, which asserts the GAIN pin high, as shown in the *External Compensation Coil Driver* section.

Feature Description (continued)

7.3.3 Compensation Driver

The compensation coil driver provides the driving current for the compensation coil. A fully-differential driver stage offers high signal voltages to overcome the wire resistance of the coil with a 5-V supply. The compensation coil is connected between I_{COMP1} and I_{COMP2}, generating an analog voltage across the coil (shown in Figure 39) that turns into current from the wire resistance (and eventually from the inductance). The compensation current represents the primary current transformed by the turns ratio. A shunt resistor is connected in this loop and the high-precision difference amplifier translates the voltage from the shunt to an output voltage.

Both compensation driver outputs provide low impedance over a wide frequency range to ensure smooth transitions between the closed-loop compensation frequency range and the high-frequency range, where the primary winding directly couples the primary current into the compensation coil at a rate set by the winding ratio.

The two compensation driver outputs are designed with protection circuitry to handle inductive energy. However, additional external protection diodes may be necessary for high-current sensors.

For reliable operation, a wire break in the compensation circuit can be detected. If the feedback loop is broken, the integrating filter drives the I_{COMP1} and I_{COMP2} outputs to the opposite rails. With one of these pins coming within 300 mV to ground, a comparator tests for a minimum current flowing between I_{COMP1} and I_{COMP2}. If the current stays below the threshold current level for a minimum of 100 μs, the ERROR pin is asserted active (low). The threshold current level for the test is less than 57 mA at 25°C and 65 mA at −40°C if the I_{COMP} pins are fully railed, as shown in the *Typical Characteristics* section.

For sensors with high winding resistance (compensation coil resistance + R_{SHUNT}) or that are connected to an external compensation driver, this function must be disabled by pulling the CCdiag pin low, as shown in Equation 1:

$$R_{MAX} = \frac{V_{OUT}}{65\text{ mA}}$$

where:

- V_{OUT} equals the peak voltage between I_{COMP1} and I_{COMP2} at a 65-mA drive current; and
- R_{MAX} equals the sum of the coil and the shunt resistance (1)

7.3.4 External Compensation Coil Driver

An external driver for the compensation coil connects to the I_{COMP1} and I_{COMP2} outputs. To prevent a wire break indication, CCdiag must be asserted low.

An external driver provides a higher drive voltage and more drive current. The driver moves the power dissipation to the external transistors, thereby allowing a higher winding resistance in the compensation coil and more current. Figure 40 shows a block diagram of an external compensation coil driver. To drive the buffer, one or both of the I_{COMP} outputs may be used. Note, however, that the additional voltage gain can cause instability of the loop. Therefore, the internal gain may be reduced by approximately 8 dB by asserting the GAIN pin high. R_{SHUNT} is connected to GND to allow for a single-ended external compensation driver. The differential amplifier continues to sense the voltage, and is used for the gain and over-range comparator or ERROR flag.

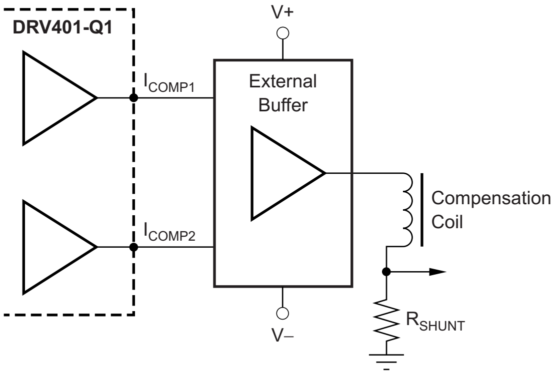


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Figure 40. DRV401-Q1 with External Compensation Coil Driver and R_{SHUNT} Connected to GND

Feature Description (continued)

7.3.5 Shunt Sense Amplifier

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal SiCr resistors.

7.3.6 Over-Range Comparator

High peak current can overload the differential amplifier connected to the shunt. The OVER-RANGE pin, an open-drain output, indicates an over-voltage condition for the differential amplifier by pulling low. The output of this flag is suppressed for 3 µs, preventing unwanted triggering from transients and noise. This pin returns to high when the overload condition is removed (an external pull-up is required to return the pin high).

This ERROR flag provides a warning about a signal clipping condition, but is also a window comparator output for actively shutting off circuits in the system. The value of the shunt resistor defines the operating window for the current. The value of the shunt resistor sets the ratio between the nominal signal and the trip level of the over-range flag. The trip current of this window comparator is calculated using the following example:

> With a 5-V supply, the output voltage swing is approximately ±2.45 V (load and supply voltage-dependent).
>
> The gain of 4 V/V allows an input swing of ±0.6125 V.
>
> Thus, the clipping current is $I_{MAX} = 0.6125\ V / R_{SHUNT}$.

See Figure 10.

The over-range condition is internally detected when the amplifier exceeds the linear operating range, not merely as a set voltage level. Therefore, the error or the over-range comparator level is reliably indicated in fault conditions such as output shorts, low load or low supply conditions. The flag is activated when the output cannot drive the voltage higher. The configuration is a safety improvement over a voltage level comparator.

NOTE

The internal resistance of the compensation coil may prevent high compensation current from flowing because of I_{COMP} driver overload. Therefore, the differential amplifier may not overload with this current. However, a fast rate of change of the primary current would be transmitted through transformer action and safely trigger the overload flag.

7.3.7 Voltage Reference

The precision 2.5-V reference circuit offers low drift (typically 10 ppm/K), used for internal biasing, and connects to the REF_{OUT} pin. The circuit is intended as the reference point of the output signal to allow a bipolar signal around it. The output is buffered for low impedance and tolerates sink and source currents of ±5 mA. Capacitive loads may be directly connected, but generate ringing on fast load transients. A small series resistor of a few ohms improves the response, especially for a capacitive load in the range of 1 µF. Figure 41 illustrates this circuit configuration and the transient load regulation with 1-nF direct load.

The reference source is part of the integrated circuit and referenced to GND2. Large current pulses driving the compensation coil generates a voltage drop in the GND connection that may add on to the reference voltage. Therefore, a low impedance GND layout is critical to handle the currents and the high bandwidth of the device.

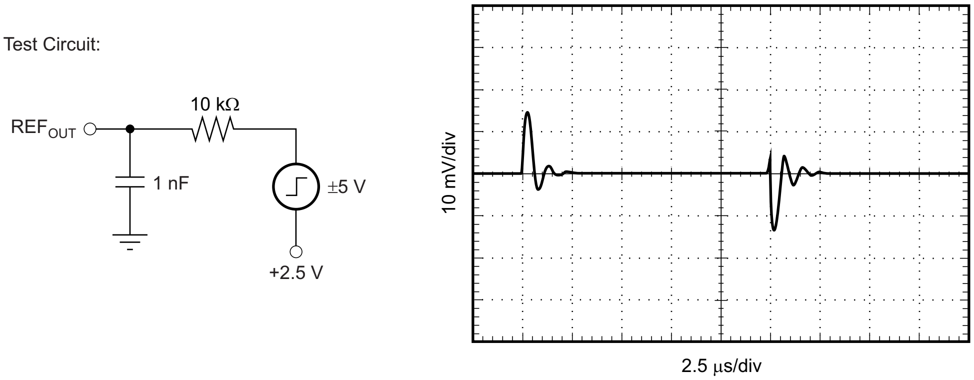


Figure 41. Pulse Response: Test Circuit and Scope Shot of Reference

7.3.8 Demagnetization

Iron cores are not immune to residual (remanence) magnetism. The residual remanence produces a signal offset error, especially after strong current overload, which goes along with high magnetic field density. Therefore, the DRV401-Q1 device includes a signal generator for a demagnetization cycle. The digital control pin, DEMAG, starts the cycle on demand after the pin is held high for at least 25.6 µs. Shorter pulses are ignored. The cycle lasts for approximately 110 ms. During this time, the ERROR flag is asserted low to indicate that the output is not valid. When DEMAG is high during power-on, a demagnetization cycle immediately initiates (12 µs) after power-on (V_{DD} > 4 V). Holding DEMAG low avoids this cycle at power-up. See the *Power-On and Brownout* section for more information.

The probe circuit is in normal operation and oscillates during the demagnetization cycle. The PWM and $\overline{\text{PWM}}$ outputs are active accordingly.

A demagnetization cycle can be aborted by pulling DEMAG low, filtered by 25 µs to ignore glitches, as shown in Figure 46. In a typical circuit, the DEMAG pin may be connected to the positive supply, which enables a degauss cycle every time the unit is powered on.

The degauss cycle is based on an internal clock and counter logic. The maximum current is limited by the resistance of the connected coil in series with the shunt resistor. The DEMAG logic input requires a 5-V, CMOS-compatible signal.

7.3.9 Power-On and Brownout

Power-on is detected with the supply voltage going higher than 4 V at V_{DD1}. When DEMAG is high, a degauss cycle is started, as shown in Figure 46 through Figure 49. During this time the ERROR flag remains low, indicating the *not ready* condition. Maintaining DEMAG low prevents this cycle, and the DRV401-Q1 device starts operation approximately 32 µs after power-up. If no probe error conditions are detected within four full cycles (that is, the probe half-periods are shorter than 32 µs and longer than 280 ns), the compensation driver starts and the ERROR pin indicates the ready condition by going high, typically about 42 µs after power-up.

NOTE

An external pull-up resistor is required to pull the ERROR pin high.

Both supply pins (V_{DD1} and V_{DD2}) must not differ by more than 100 mV for proper device operation. They are normally connected together or separately filtered as shown in *Layout*.

The DRV401-Q1 device tests for low supply voltage with a brownout voltage level of 4 V; proper power conditions must be supplied. Good power-supply and low equivalent series resistance (ESR) bypass capacitors are required to maintain the supply voltage during the large current pulses that the DRV401-Q1 device drives.
A critical voltage level is derived from the proper operation of the probe driver. The probe interface relies on a peak current flowing through the probe to trip the comparator. The probe resistance plus the internal resistance of the driver (see *Probe Coil Loop, Internal Resistor* parameters in the *Electrical Characteristics* table) sets the lower limit for the acceptable supply voltage. Voltage drops lasting less than 31 µs are ignored. The probe error detection activates the ERROR pin when proper oscillation fails for more than 32 µs.

A low supply voltage condition, or brownout, is detected at 4 V. Short and light voltage drops of less than 100 µs are ignored, provided the probe circuit continues to operate. If the probe no longer operates, the ERROR pin goes active. Signal overload recovery is only provided if the probe loop was not discontinued.

A supply drop lasting longer than 100 µs generates power-on reset. A voltage dip down to 1.8 V (for V_{DD1}) initiates a power-on reset.

7.3.10 Error Conditions

In addition to the overrange flag that indicates signal clipping in the output amplifier (differential amplifier), a system error flag is provided. The ERROR flag indicates conditions when the output voltage does not represent the primary current. The ERROR flag is active during a demagnetization cycle, power-fail, or brownout. The ERROR flag becomes active with an open or short-circuit in the probe loop. When the error condition is no longer present and the circuit returns to normal operation, the flag resets.

The ERROR and overrange flags are open-drain logic outputs. The flags connect together for a wired-*OR* and require an external pull-up resistor for proper operation.

The following conditions result in ERROR flag activation (ERROR asserts low):

1. The probe comparator stays low for more than 32 µs. This condition occurs if the probe coil connection is open or if the supply voltage dips to the level where the required saturation current cannot be reached. During the 32-µs timeout, the I_{COMP} driver remains active but goes inactive thereafter. In case of recovery, ERROR is low and the I_{COMP} driver remains in reset for another 3.3 ms.
2. The probe driver pulse-width is less than 280 ns for three consecutive periods. This condition indicates a shorted field probe coil or a fully-saturated sensor at start-up. If this condition persists longer than 25 µs and then recovers, the ERROR flag remains low and I_{COMP} is in reset for another 3.3 ms. If the condition lasts less than 25 µs, the ERROR flag recovers immediately and the I_{COMP} driver is not interrupted.
3. During demagnetization, if the cycle is aborted early by pulling DEMAG low, the ERROR flag stays low for another 3.3 ms (I_{COMP} is disabled during this time).
4. An open compensation coil is detected (longer than 100 µs). This condition indicates that not enough current is flowing in the I_{COMP} driver output; this condition may be the result of a high-resistance compensation coil or the connection of an external driver. Detection of this condition can be disabled by setting the CCdiag pin low.

NOTE

The probe driver, the PWM signal filter, and the I_{COMP} driver continue to function in normal mode. Only the ERROR flag is asserted in the case when an open compensation coil is detected.

---

5. At power-on after V_{DD1} crosses the 4-V threshold, the ERROR flag is low for approximately 42 μs.
6. A supply voltage low (brownout) condition lasts longer than 100 μs. Recovery is the same as power-up, with or without a demagnetization cycle.

7.3.11 Protection Recommendations

The I_{AIN1} and I_{AIN2} inputs require external protection to limit the voltage swing beyond 10 V of the supply voltage. The driver outputs I_{COMP1} and I_{COMP2} handles high current pulses protected by internal clamp circuits to the supply voltage. If repeated overcurrents of large magnitudes are expected, connect external Schottky diodes to the supply rails. This external protection prevents current flowing into the die.

The IS1 and IS2 probe connections are protected with diode clamps to the supply rails. In normal applications, no external protection is required. The maximum current must be limited to ±75 mA.

All other pins offer standard protection. See the *Absolute Maximum Ratings* table for more information.

7.4 Device Functional Modes

The DRV401-Q1 has a single functional mode and is operational when the power supply voltages, V_{DD1} and V_{DD2}, are between 4.5 V and 5.5 V. For unusual operating conditions where a brownout condition may occur the DRV401-Q1 may perform a power-on reset. See the *Power-On and Brownout* section for a complete description of operation during a brownout.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Functional Principle of Closed-Loop Current Sensors with Magnetic Probe Using the DRV401-Q1 Device

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method and an excellent galvanic isolation performance combined with high resolution, accuracy, and reliability.

At dc and in low-frequency ranges, the magnetic field induced from the current in the primary winding is compensated by a current flowing through a compensation winding. A magnetic field probe, located in the magnetic core loop, detects the magnetic flux. This probe delivers the signal to the amplifier that drives the current through the compensation coil, bringing the magnetic flux back to zero. This compensation current is proportional to the primary current, relative to the winding ratio.

In higher-frequency ranges, the compensation winding acts as the secondary winding in the current transformer, while the H-bridge compensation driver is rolled off and provides low output impedance.

A difference amplifier senses the voltage across a small shunt resistor that is connected to the compensation loop. This difference amplifier generates the output voltage that is referenced to REF_{IN} and is proportional to the primary current. The *Functional Block Diagram* shows the DRV401-Q1 device used as a compensation current sensor.

Application Information (continued)

8.1.2 Basic Connection

The circuit shown in Figure 42 offers an example of a fully-connected current sensor system.

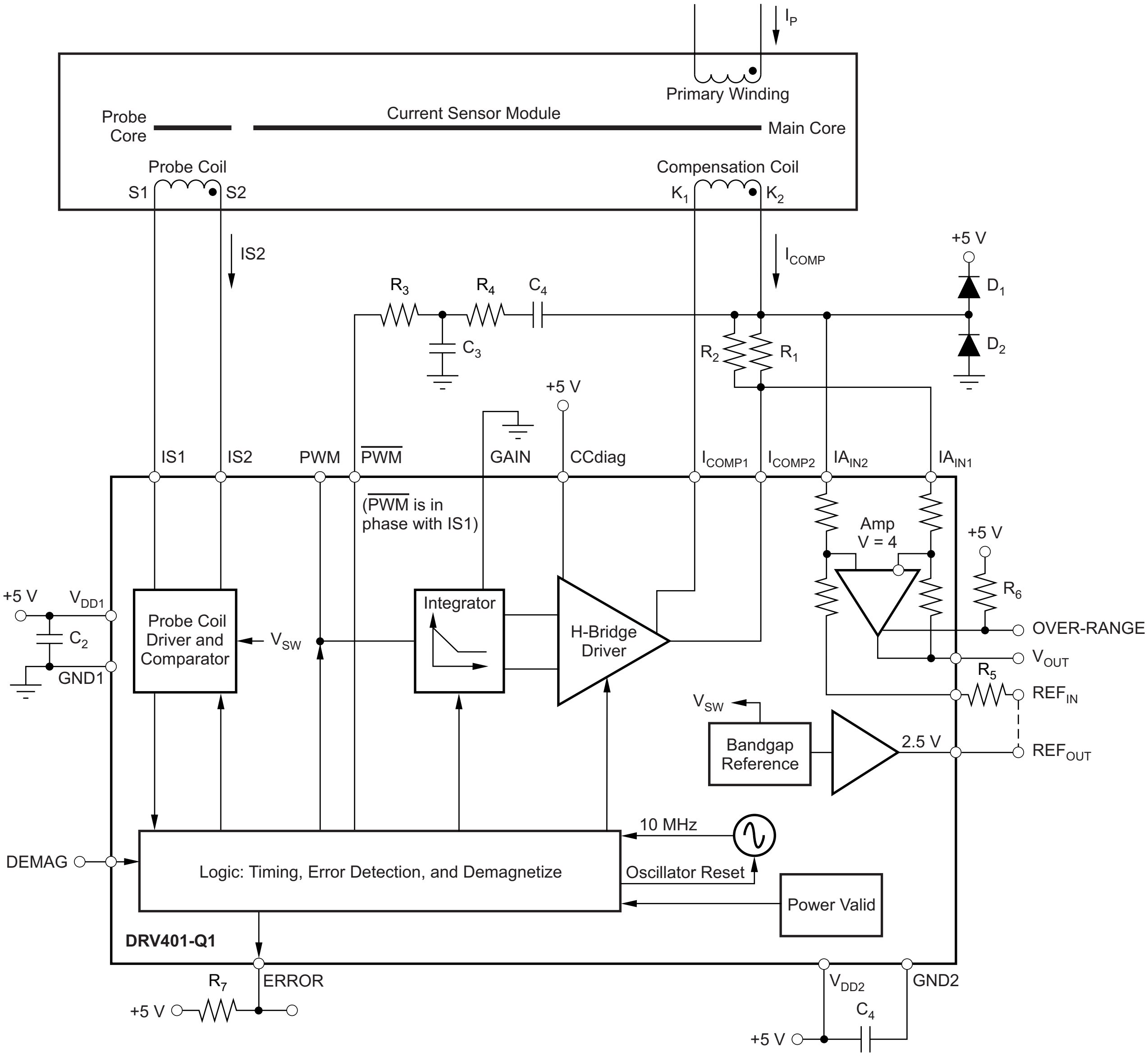


Figure 42. Basic Connection Circuit

The connection example in Figure 42 illustrates the few external components required for optimal performance. Each component is described in the following list:

- **I_P** is the primary current to be measured; **K_1** and **K_2** connect to the compensation coil. **S1** and **S2** connect to the magnetic field probe. The dots indicate the winding direction on the sensor main core.
- **R_1** and **R_2** form the shunt resistor R_{SHUNT}. This resistance is split into two to allow for adjustments to the required R_{SHUNT} value. The accuracy and temperature stability of these resistors are part of the final system performance.
- **R_3** and **R_4**, together with **C_3** and **C_4**, form a network that reduces the remaining probe oscillator ripple in the output signal. The component values depend on the sensor type and are tailored for best results. This network is not required for normal operation.

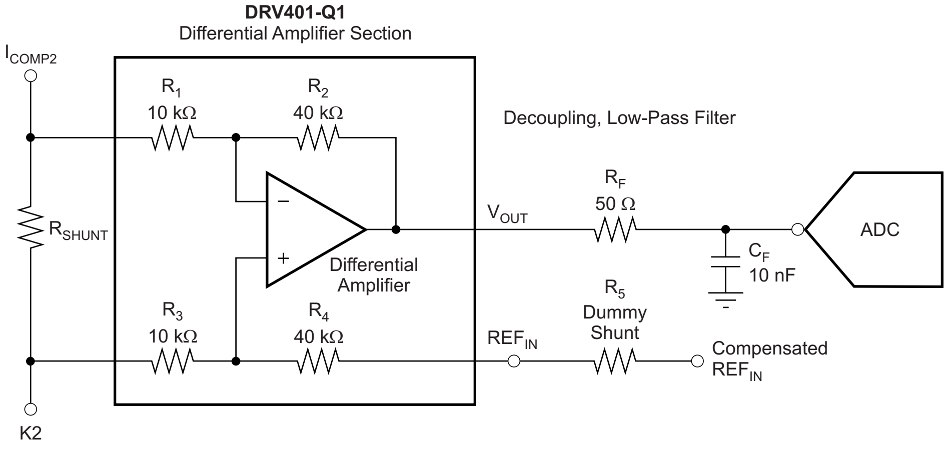
Application Information (continued)

- **R_5** is the dummy shunt (R_D) resistor used to restore the symmetry of both differential amplifier inputs. $R_5 = 4 \times R_{SHUNT}$, but the accuracy is less important.
- **R_6** and **R_7** are pull-up resistors connected to the logic outputs.
- **C_1** and **C_2** are decoupling capacitors. Use low ESR-type capacitors connected close to the pins. Use low-impedance printed circuit board (PCB) traces, either avoiding vias (plated-through holes) or using multiple vias. A combination of a large (> 1-µF) and a small (< 4.7-nF) capacitor are suggested. When selecting capacitors, make sure to consider the large pulse currents handled from the DRV401-Q1 device.
- **D_1** and **D_2** are protection diodes for the differential amplifier input. They are only needed if the voltage drop at R_{SHUNT} exceeds 10 V at the maximum possible peak current.

8.2 Typical Application

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal SiCr resistors.

Both inputs of the differential amplifier are normally connected to the current shunt resistor. The resistor adds to the internal (10-kΩ) resistor, slightly reducing the gain in this leg. For best common-mode rejection (CMR), a dummy shunt resistor (R_5) is placed in series with the REF_{IN} pin to restore matching of both resistor dividers, as shown in Figure 43.



R_5 is a dummy shunt resistor equal to $4 \times R_{SHUNT}$ to compensate for R_{SHUNT} and provide optimal CMR.

Figure 43. Internal Difference Amplifier with an Example of a Decoupling Filter

8.2.1 Design Requirements

- Operate from a single 5-V power supply.
- Measure the compensation coil current with a gain = 4 V/V.
- Maximize the gain accuracy.
- Minimize the common-mode error.

Typical Application (continued)

8.2.2 Detailed Design Procedure

For gains of 4 V/V, Equation 2 shows the calculation:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3} \quad (2)$$

With $R_2 / R_1 = R_4 / R_3 = 4$; $R_5 = R_{SHUNT} \times 4$.

Typically, the gain error resulting from the resistance of R_{SHUNT} is negligible; for 70 dB of common-mode rejection, however, the match of both divider ratios must be better than 1/3000.

The amplifier output may drive close to the supply rails, and is designed to drive the input of a successive-approximation resistance (SAR)-type ADC; adding an RC low-pass filter stage between the DRV401-Q1 device and the ADC is recommended. This filter limits the signal bandwidth and decouples the high-frequency component of the converter input sampling noise from the amplifier output. For R_F and C_F values, see the specific converter recommendations in the specific product data sheet. Empirical evaluation may be necessary to obtain optimum results.

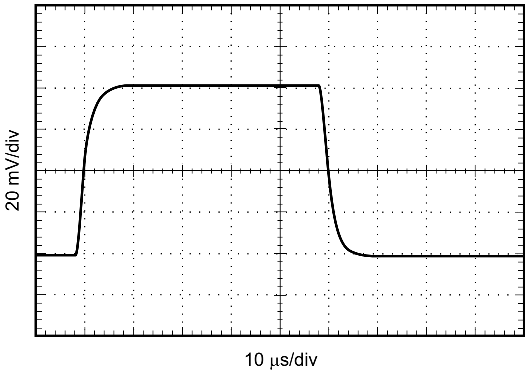
The output drives 100 pF directly and shows 50% overshoot with approximately 1-nF capacitance. Adding R_F allows much larger capacitive loads, as shown in Figure 44 and Figure 45.

NOTE

Note that with an R_F value of only 20 Ω, the load capacitor must be smaller than 1 nF or larger than 33 nF to avoid overshoot; with an R_F value of 50 Ω, this transient area is avoided.

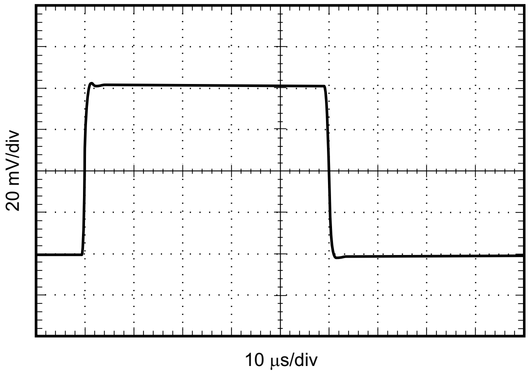
The reference input (REF_{IN}) is the reference node for the exact output signal (V_{OUT}). Connecting REF_{IN} to the reference output (REF_{OUT}) results in a live zero reference voltage of 2.5 V. Using the same reference for REF_{IN} and the ADC avoids mismatch errors that exist between two reference sources.

8.2.3 Application Curves



R_5 = 20 Ω, C_D = 100 nF

Figure 44. Figure 44 Performance (V_{OUT})

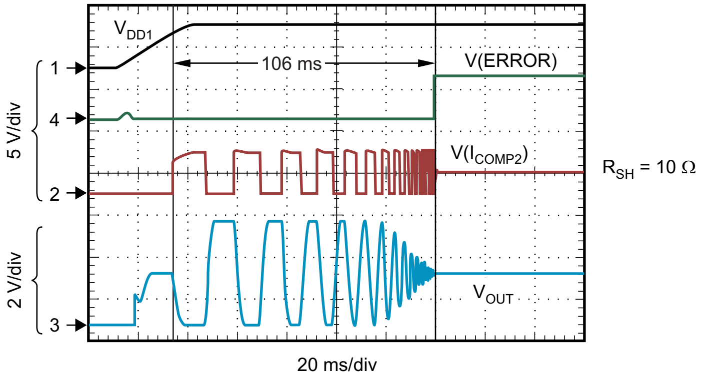


R_5 = 50 Ω, C_D = 10 nF

Figure 45. Figure 45 Performance (V_{OUT})

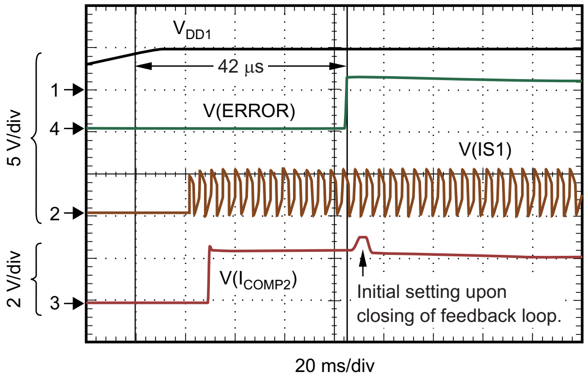
9 Power Supply Recommendations

The DRV401-Q operates from a single power supply, nominally 5 V, and must remain between 4.5 V and 5.5 V for normal operation. See Figure 46, Figure 47, Figure 48, and Figure 49 for device power-on behavior.



With power-up, the V_{OUT} across the compensation coil centers around half the supply and then starts the cycle after the 4-V threshold is exceeded. The ERROR flag resets to H after the cycle is completed.

Figure 46. Demagnetization and Power-On Timing: Demagnetization Cycle on Power-Up



The probe oscillation V(IS1) starts just before ERROR resets—15 µs after the supply voltage crosses the 4-V threshold.

Figure 47. Demagnetization and Power-On Timing: Power-Up Without Demagnetization

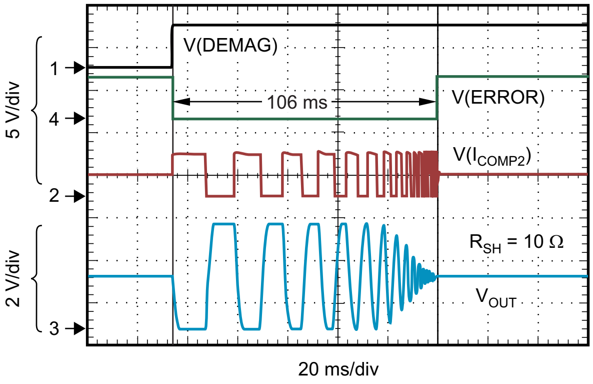
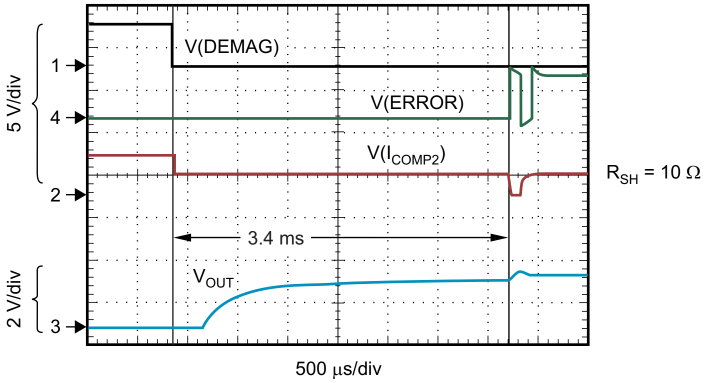


Figure 48. Demagnetization and Power-On Timing: Demagnetization Cycle On Command



The ERROR flag resets to H (as shown) and the output settles back to normal operation.

Figure 49. Demagnetization and Power-On Timing: Abort of Demagnetization Cycle

10 Layout

10.1 Layout Guidelines

The typical device configuration is shown in Figure 42. The DRV401-Q1 operates with relatively large currents and fast current pulses, and offers wide-bandwidth performance. The device is often exposed to large distortion energy from the primary signal and the operating environment. Therefore, the wiring layout must provide shielding and low-impedance connections between critical points.

Use low-ESR capacitors for power-supply decoupling. Use a combination of a small capacitor and a large capacitor with a 1-µF or larger value. Use low-impedance tracks to connect the capacitors to the pins.

Both grounds must be connected to a local ground plane. Both supplies can be connected together; however, best results are achieved with separate decoupling (to the local GND plane) and ferrite beads in series with the main supply. The ferrite beads decouple the DRV401-Q1 device, reducing interaction with other circuits powered from the same supply voltage source.

The reference output is referred to GND2. A low-impedance, star-type connection is required to avoid the driver current and the probe current modulating the voltage drop on the ground track.

The connection wires of the difference amplifier to the shunt must be low resistance and of equal length. For best accuracy, avoid current in this connection. Consider using a Kelvin Contact-type connection. The required resistance value may be set using two resistors.

Wires and PCB traces for S1 and S2 must be close or twisted. I_{COMP1} and I_{COMP2} must be wired close together. To avoid capacitive coupling, run a ground shield between the S1/S2 and I_{COMP} wire pair or keep them distant from each other.

The compensation driver outputs (I_{COMP}) are low frequency only. However, the primary signal (with high-frequency content present) is coupled into the compensation winding, the shunt, and the difference amplifier. TI recommends a careful layout.

The REF_{OUT} and V_{OUT} output drives some capacitive loads, but avoid large direct capacitive loads; these loads increase internal pulse currents. Given the wide bandwidth of the differential amplifier, isolate any large capacitive load with a small series resistor. A small capacitor (in the pF range) improves the transient response on a high resistive load.

The exposed thermal pad on the bottom of the package must be soldered to GND because the thermal pad is internally connected to the substrate, which must be connected to the most negative potential. Solder the exposed pad to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example

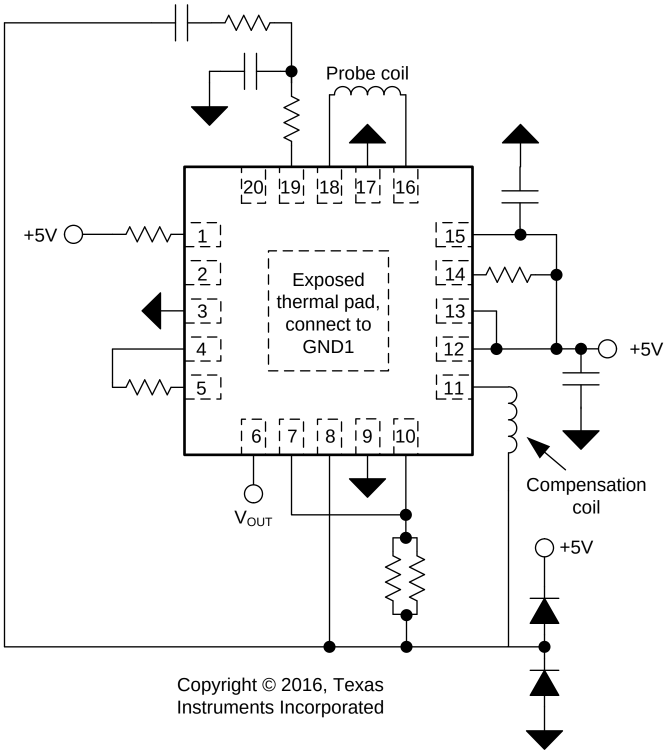


Figure 50. DRV401-Q1 Layout Example (RGW Package)

10.3 Power Dissipation

Using the thermally-enhanced VQFN package dramatically reduces the thermal impedance from junction to case. This package is constructed using a down-set lead frame that the die is mounted on. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The two outputs (I_{COMP1} and I_{COMP2}) are linear outputs. Therefore, the power dissipation on each output is proportional to the current multiplied by the internal voltage drop on the active transistor. For I_{COMP1} and I_{COMP2}, this internal voltage drop is the voltage drop to V_{DD2} or GND, according to the current-conducting side of the output.

Output short-circuits are particularly critical for the driver because the full supply voltage can be seen across the conducting transistor, and the current is not limited by anything other than the current density limitation of the FET. Permanent damage to the device may occur.

The DRV401-Q1 does not include temperature protection or thermal shutdown.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the DRV401-Q1 device, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *PowerPAD Thermally-Enhanced Package* (SLMA002)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *QFN/SON PCB Attachment* (SLUA271)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help

Community Resources (continued)

solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Thermal Pad

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. Table 1 shows the thermal resistance (θ_{JA}) for the package with the exposed thermal pad soldered to a normal PCB, as described in *PowerPAD Thermally-Enhanced Package* (SLMA002). Refer to EIA/JEDEC Specifications JESD51-0 to 7, *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017). These documents are available for download at www.ti.com.

Table 1. θ_{JA} and θ_{JP} Estimations According to EIA/JED51-7(1)

PARAMETER	VQFN
θ_{JP}	9
θ_{JA} with still air	40
θ_{JA} with forced airflow (150 lfm)	38

(1) θ_{JA} = junction-to-ambient thermal resistance.

TI recommends measuring the temperature as close as possible to the thermal pad. The relatively low thermal impedance, θ_{JP}, of less than 10°C/W (with some additional °C/W to the temperature test point on the PCB) allows good estimation of the junction temperature in the application.

The thermal pad on the PCB must contain nine or more vias for the VQFN package.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions must be tested in the actual operating environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below 125°C.

NOTE

All thermal models have an accuracy ≈ 20%.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV401AQRGWRQ1	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV 401Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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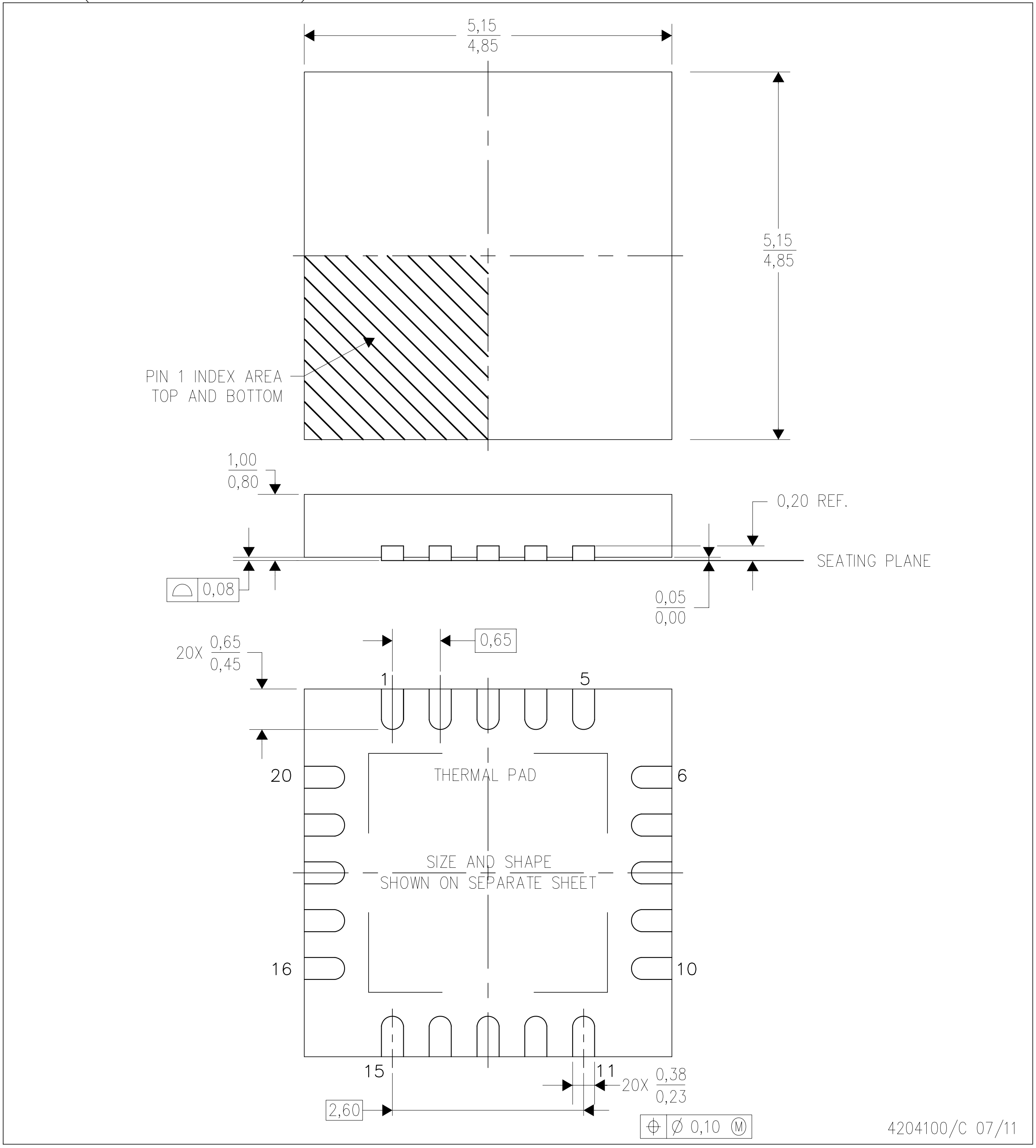
OTHER QUALIFIED VERSIONS OF DRV401-Q1 :

- Catalog: DRV401
- Enhanced Product: DRV401-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

RGW (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flat pack, No–leads (QFN) package configuration
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

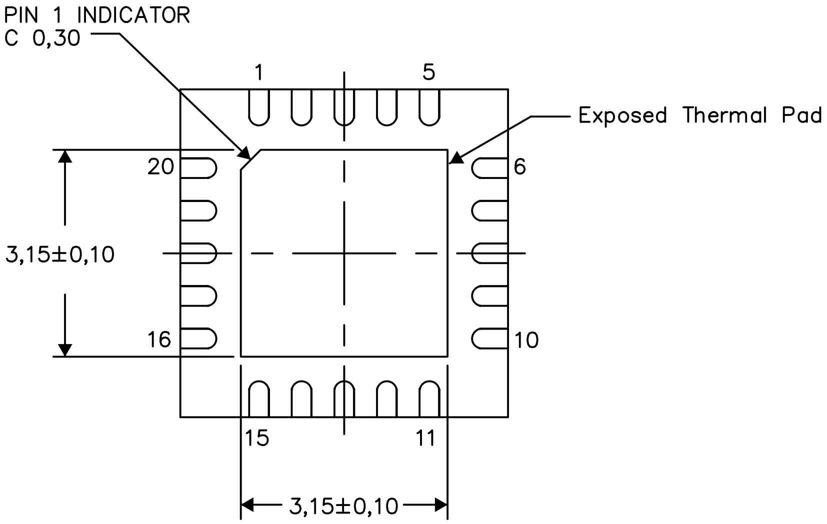
RGW (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



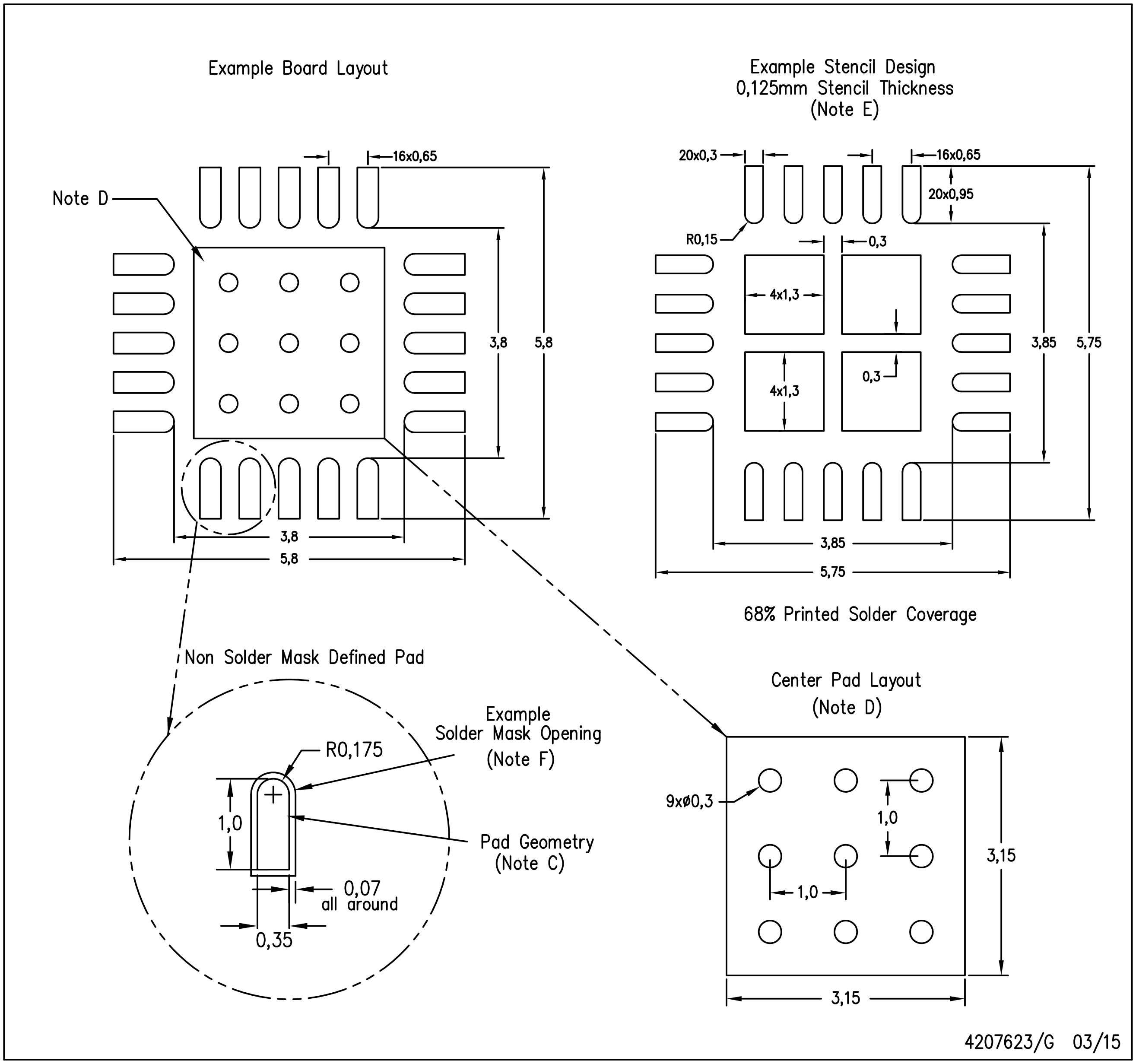
Bottom View

Exposed Thermal Pad Dimensions

4206352-2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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