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EZ-PD™ CCG3

USB Type-C Port Controller

General Description

EZ-PD™ CCG3 is a highly integrated USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG3 provides a complete USB Type-C and USB-Power Delivery port control solution for notebooks, dongles, monitors, docking stations and power adapters. CCG3 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex® -M0 processor with 128-KB flash, 8-KB SRAM, 20 GPIOs, full-speed USB device controller, a Crypto engine for authentication, a 20V-tolerant regulator, and a pair of FETs to switch a 5V (VCONN) supply, which powers cables. CCG3 also integrates two pairs of gate drivers to control external VBUS FETs and system level ESD protection. CCG3 is available in 40-QFN, 32-QFN, and 42-WLCSP packages.

Features

Type-C and USB-PD Support

- Integrated USB Power Delivery 3.0 support
- Integrated USB-PD BMC transceiver
- Integrated VCONN FETs
- Configurable resistors R_A, R_P, and R_D
- Dead Battery Detection support
- Integrated fast role swap and extended data messaging
- Supports one USB Type-C port
- Integrated Hardware based overcurrent protection (OCP) and overvoltage protection (OVP)

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 128-KB Flash
- 8-KB SRAM

Integrated Digital Blocks

- Hardware Crypto block enables Authentication
- Full-Speed USB Device Controller supporting Billboard Device Class
- Integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 2.7 V to 21.5 V operation
- 2x Integrated dual-output gate drivers for external VBUS FET switch control
- Independent supply voltage pin for GPIO that allows 1.71 V to 5.5 V signaling on the I/Os
- Reset: 30 µA, Deep Sleep: 30 µA, Sleep: 3.5 mA

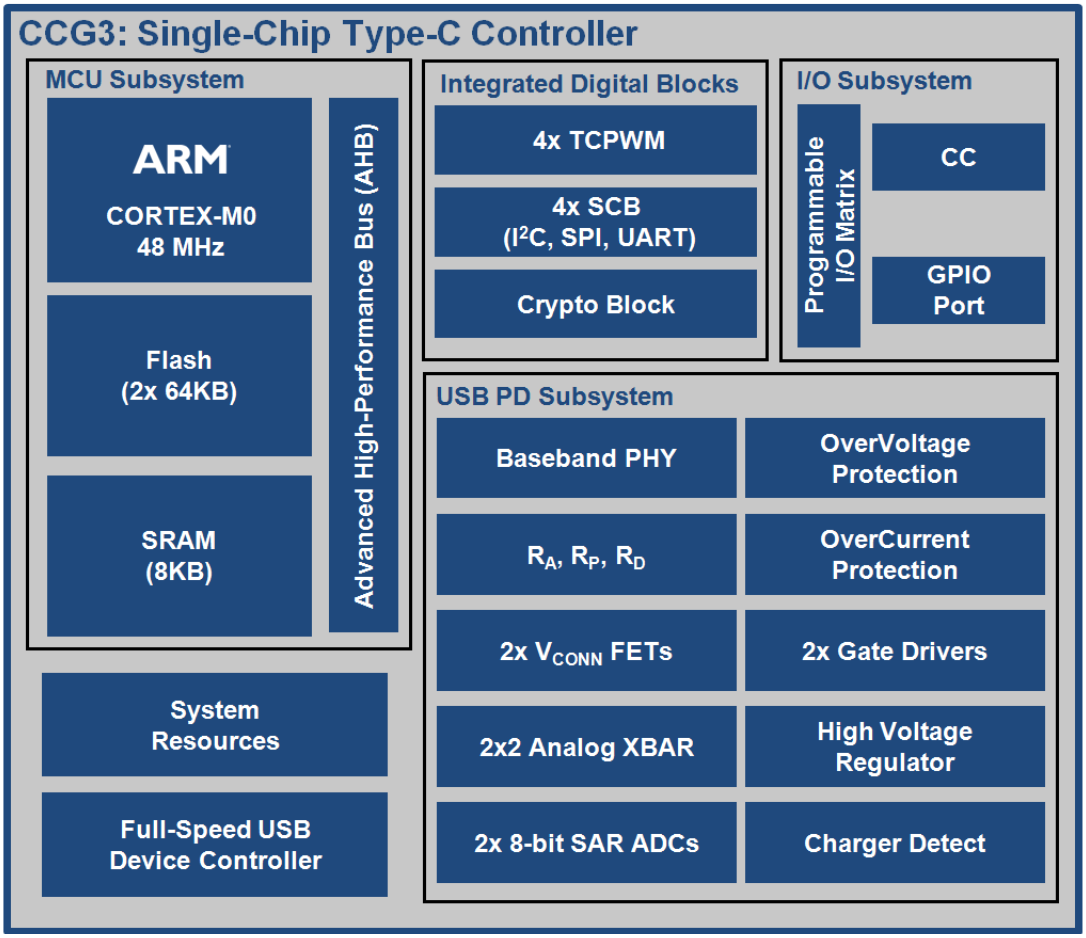
System-Level ESD Protection

- On CC, SBU, DPLUS, DMINUS and VBUS pins
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

Packages

- 40-pin QFN, 32-pin QFN, and 42-ball CSP for Notebooks/Accessories
- Supports industrial temperature range (–40 °C to +105 °C)

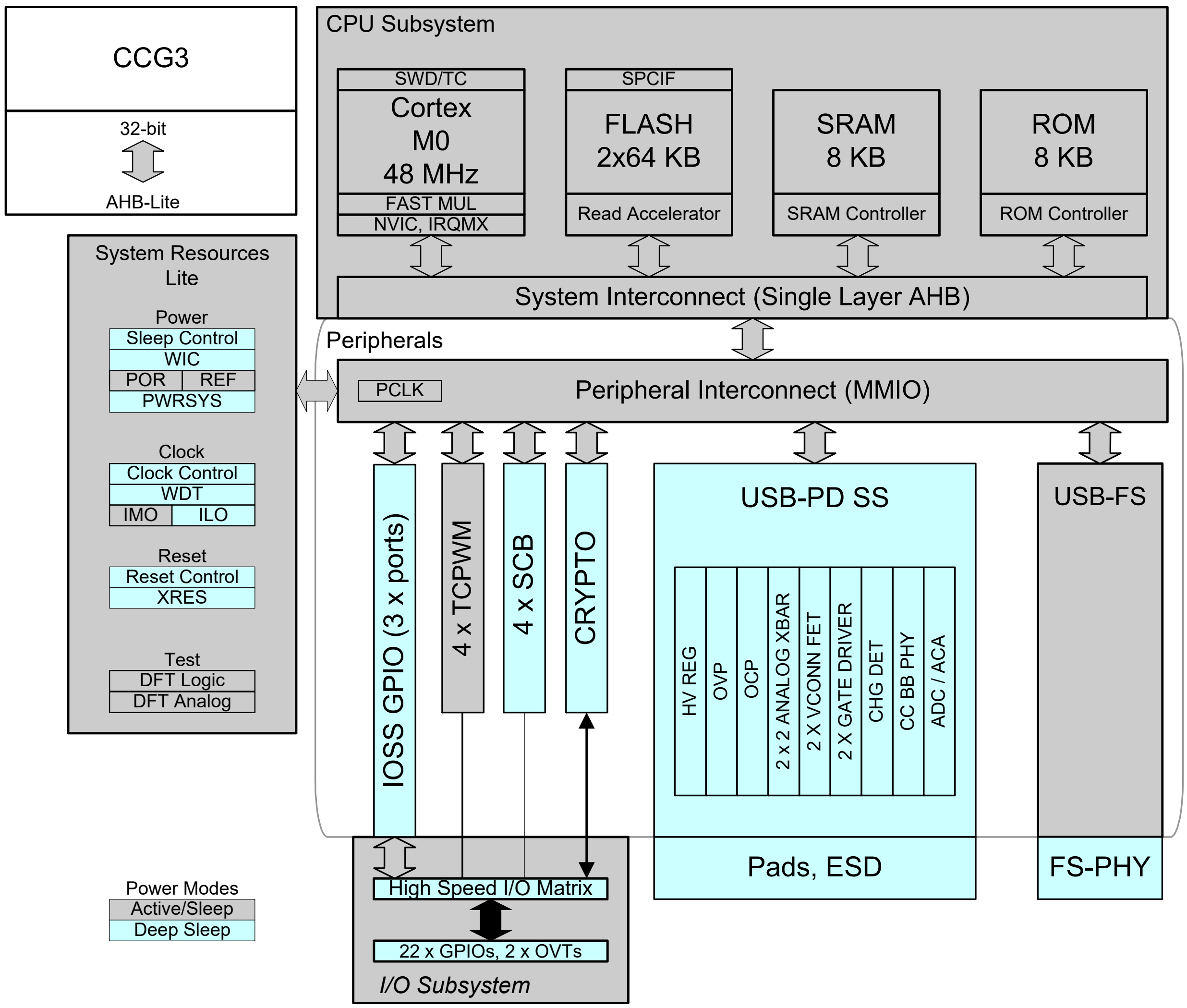
Logic Block Diagram



Contents

EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram[1]



Note
1. See Acronyms section for more details.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for Advanced Encryption Standard (AES) block cipher, Secure Hash Algorithm (SHA-1 and SHA-2), Cyclic Redundancy Check (CRC), and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD subsystem contains all of the blocks related to USB Type-C and Power Delivery. The subsystem consists of the following:

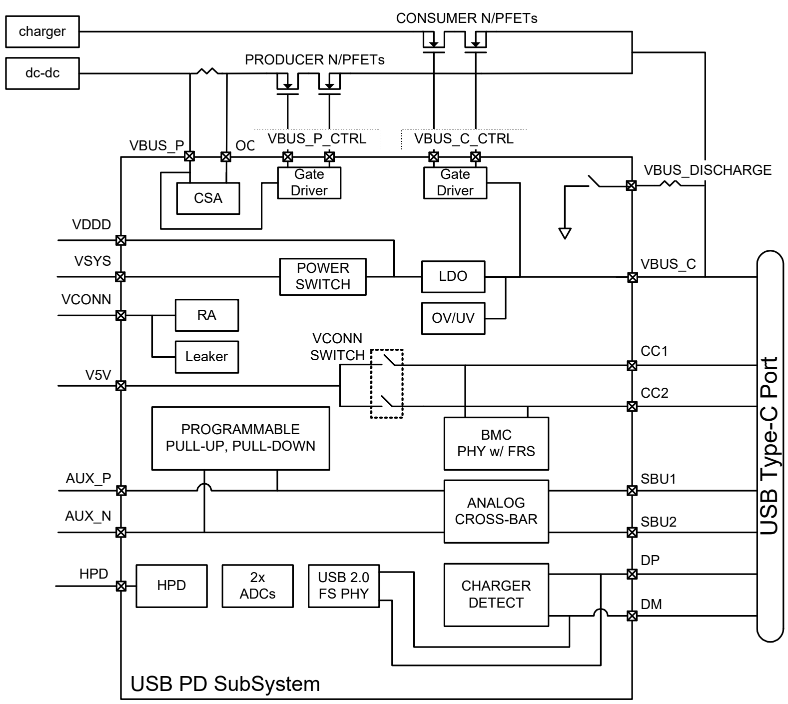
- Biphase Marked Coding (BMC) PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN R_A Termination and Leakers
- Analog Crossbar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable pull-up and pull-down termination on the AUX_P/AUX_N pins
- Hot Plug Detect (HPD) processor
- VBUS_C regulator (20V LDO)
- Power switch between VSYS supply and VBUS_C regulator output
- VBUS_C overvoltage (OV) and undervoltage (UV) detectors
- Current sense amplifier (CSA) for overcurrent detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0 V to 3.3 V regulator
- Charger Detection/Emulation for USB BC1.2 and other proprietary protocols
- Two instances of 8-bit SAR ADCs
- 8-kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

The EZ-PD CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2-V analog front end (AFE). This subsystem integrates the required terminations to identify the role of the CCG3 device, including R_P and R_D for UFP/DFP roles and R_A for EMCA/VCONN powered accessories. The programmable VCONN leakers are included to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The analog crossbar enables connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The Overvoltage/Undervoltage (OV/UV) block monitors the VBUS_C supply for programmable overvoltage and undervoltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an overcurrent condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed overvoltage and overcurrent conditions. The VBUS_C discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB-PD subsystem also contains two 8-bit Successive Approximation Register (SAR) ADCs for analog to digital conversions. The voltage reference for the ADCs is generated from the VDDD supply. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global Analog Multiplex Busses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

Figure 2. USB-PD Subsystem



Full-Speed USB Subsystem

The FSUSB subsystem contains a full-speed USB device controller as described in the Integrated Billboard Device section.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG3 has four SCBs, which can be configured to implement an I^{2}C, SPI, or UART interface. The hardware I^{2}C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^{2}C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^{2}C that creates a mailbox address range in the memory of EZ-PD CCG3 and effectively reduce I^{2}C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^{2}C peripherals are compatible with the I^{2}C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^{2}C-bus specification and user manual (UM10204).

The I^{2}C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Power Systems Overview

Figure 3 shows an overview of the CCG3 power system requirement. CCG3 shall be able to operate from two possible external supply sources VBUS (4.0 V–21.5 V) or VSYS (2.7 V–5.5 V). The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3-V level. The chip's internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers majority of the core using regulators. Besides Reset mode, CCG3 has three different power modes: Active, Sleep and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VDDD and VCCD pins, both the output of regulators are brought out for connecting a 1-μF capacitor for the regulator stability only. These pins are not supported as power supplies. When CCG3 is powered from VSYS that is greater than 3.3 V, the dedicated USB regulator allows USB operation.

Figure 3. EZ-PD CCG3 Power System Block Diagram

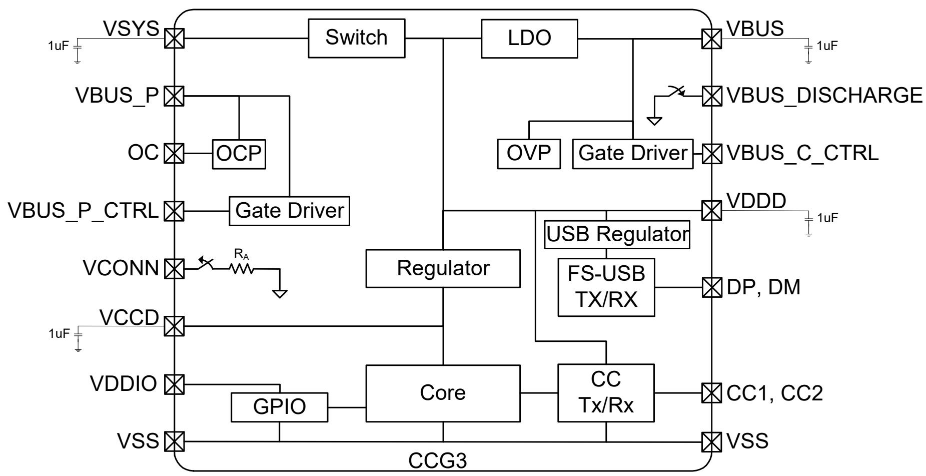


Table 1. CCG3 Power Modes

Mode	Description
RESET	Power is Valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is Valid and CPU is executing instructions.
SLEEP	Power is Valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

Pinouts

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN, and 40-QFN Devices

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
A5	1	1	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
A6	1	2	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
B6	2	3	CC2	USB PD connector detect/Configuration Channel 2
C5	N/A	N/A	CC2	USB PD connector detect/Configuration Channel 2
D4	3	4	V5V	Input Supply Voltage for VCONN FETs V5V = 5.0V – 5.5V to supply VCONN > 4.75V @ 1.5W V5V = 3.5V – 5.5V to supply VCONN > 3.00V @ 1W
C6	4	5	CC1	USB PD connector detect/Configuration Channel 1
D6	N/A	N/A	CC1	USB PD connector detect/Configuration Channel 1
E6	N/A	6	VCONN	VCONN Input - provides R_A termination for cable applications
F6	5	7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
D5	N/A	8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
E5	6	9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL
G6	7	10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
E4	N/A	11	AUX_P / P1.6	DisplayPort AUX_P signal / GPIO / UART_1_TX / SPI_1_MISO
F5	8	12	SBU1 / P1.4	USB Type-C SBU1 signal / GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
G5	9	13	SBU2 / P1.5	USB Type-C SBU2 signal / GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
G4	N/A	14	AUX_N / P1.7	DisplayPort AUX_N signal / GPIO / UART_1_RX / SPI_1_SEL
F4	10	15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
G3	11	16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
G2	13	17	VDDD	VDDD supply Input / Output (2.7 V–5.5 V)
F3	14	18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
F2	15	19	VCCD	1.8-V regulator output for filter capacitor
G1	16	20	VSYS	System power supply (2.7 V–5.5 V)
F1	17	21	DPLUS	USB 2.0 DP
E1	18	22	DMINUS	USB 2.0 DM
E2	19	23	P2.4	GPIO
D3	20	24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
D2	N/A	25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
D1	21	26	XRES	External Reset Input. Internally pulled-up to VDDIO.
C3	22	27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN, and 40-QFN Devices *(continued)*

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
C2	23	28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1
C1	24	29	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
C4	24	30	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
B1	25	31	VBUS	VBUS Input
A1	26	32	VBUS_DISCHARGE	VBUS Discharge Control output
E3	12, 27	33	VSS	Ground Supply (GND)
	EPAD	EPAD	VSS	
A2	28	34	P3.2	GPIO / TCPWM0
B2	N/A	35	P3.3	GPIO / TCPWM1
B3	29	36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI/ I2C_2_SDA / TCPWM2
A3	30	37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK/ I2C_2_SCL / TCPWM3
B4	N/A	38	P3.6	GPIO
A4	31	39	OC	Overcurrent sensor input
B5	32	40	VBUS_P	VBUS producer input

Figure 4. Pinout of 40-QFN Package (Top View)

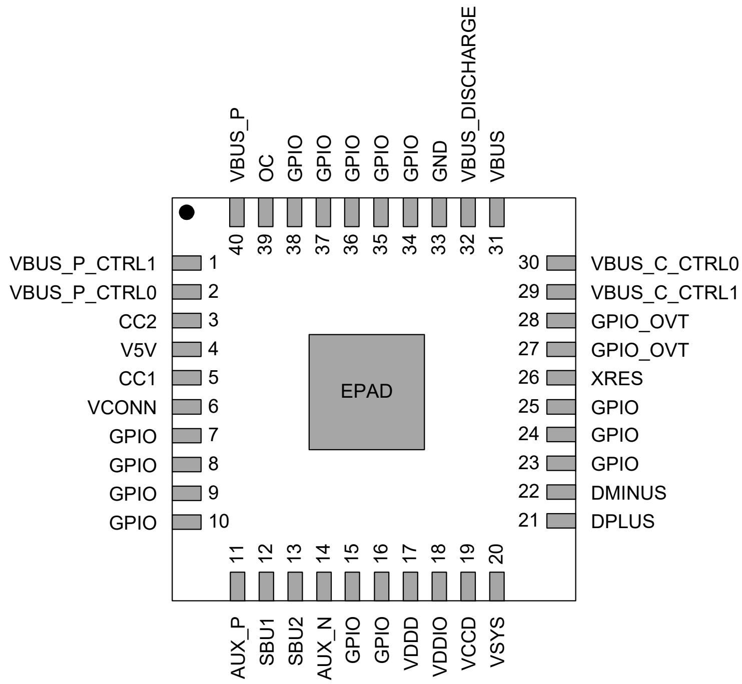


Figure 5. Pinout of 32-QFN Package (Top View)

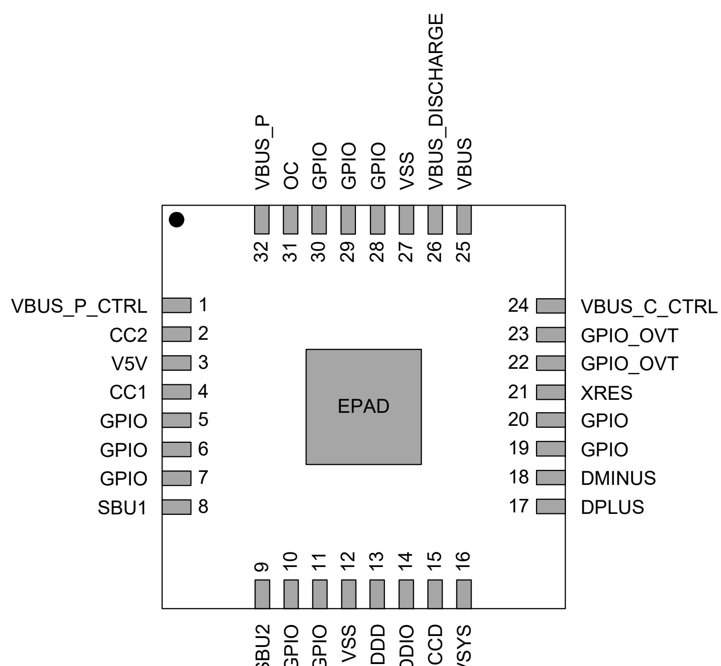


Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View

	6	5	4	3	2	1
A	VBUS_P_CTRL0	VBUS_P_CTRL1	OC	GPIO P3.5	GPIO P3.2	VBUS_DISCHARGE
B	CC2	VBUS_P	GPIO P3.6	GPIO P3.4	GPIO P3.3	VBUS
C	CC1	CC2	VBUS_C_CTRL0	GPIO_OVT P0.0	GPIO_OVT P0.1	VBUS_C_CTRL1
D	CC1	GPIO P1.1	V5V	GPIO P2.5	GPIO P2.6	XRES
E	VCONN	GPIO P1.2	AUX_P	VSS	GPIO P2.4	DMINUS
F	GPIO P1.0	SBU1	GPIO P2.0	VDDIO	VCCD	DPLUS
G	GPIO P1.3	SBU2	AUX_N	GPIO P2.1	VDDD	VSYS

Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

CCG3 Programming and Bootloading

There are two ways to program application firmware into a CCG3 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, USB, I^2C)

Generally, the CCG3 devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3 device's application firmware can be updated via the appropriate bootloader interface.

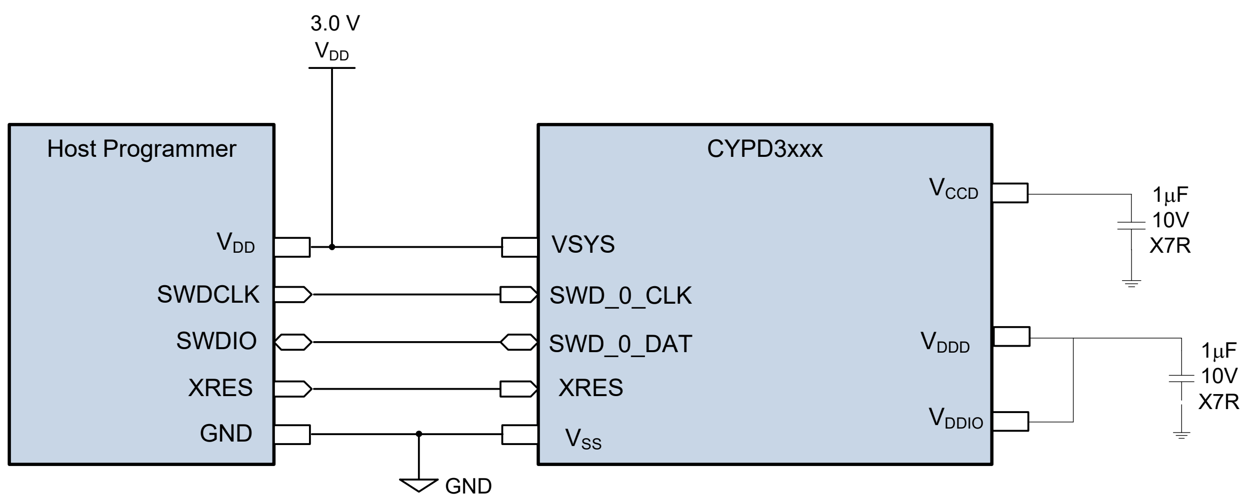
Programming the Device Flash over SWD Interface

The CCG3 family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 7, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VSYS pin of CCG3 device. If the CCG3 device is powered using an on-board power supply, it can be programmed using the "Reset Programming" option. For more details, refer to the CYPD3XXX Programming Specifications.

The CYPD3105 device for Thunderbolt cable applications is pre-programmed with a micro-bootloader that allows users to program the flash using the alternate SWD pins (SBU1 for SWD_1_CLK and SBU2 for SWD_1_DAT) that can be connected to the SBU interface of a Type-C connector. Note that this interface can be used to program the flash only once. Subsequent re-programming of this device can be done through the primary SWD interface (SWD_0_CLK and SWD_0_DAT pins). Irrespective of which SWD interface is used for programming the device, once the device is programmed with the hex file provided by Cypress for thunderbolt cable application, subsequent updates to the application firmware can be done over the CC line. Refer to Application Firmware Update over Specific Interfaces (I2C, CC, USB) for more details.

Figure 7. Connecting the Programmer to CYPD3xxx Device



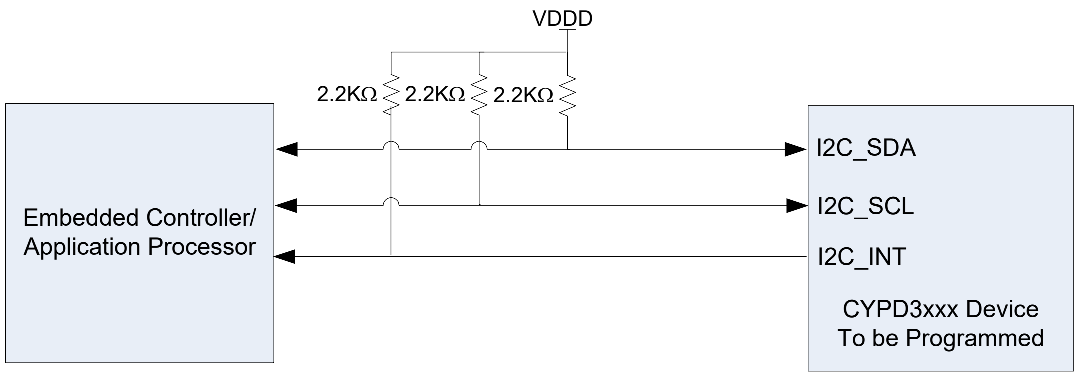
Application Firmware Update over Specific Interfaces (I^2C, CC, USB)

The application firmware can be updated over three different interfaces depending on the default firmware programmed into the CCG3 device. Refer to Table 38 for more details on default firmware that various part numbers of the CCG3 family of devices are pre-programmed with (note that some of the devices have bootloader only and some have bootloader plus application firmware). The application firmware provided by Cypress for all CCG3 applications have dual images. This allows fail-safe update of the alternate image while executing from the current image. For more information, refer to the EZ-PD Configuration Utility User Manual.

Application Firmware Update over I^2C Interface

This method primarily applies to CYPD3122, CYPD3125, and CYPD3126 devices of the CCG3 family. In these applications, the CCG3 device interfaces to an on-board application processor or an embedded controller over I^2C interface. Refer to Figure 8 for more details. Cypress provides pseudo-code for the host processor for updating the CCG3 device firmware.

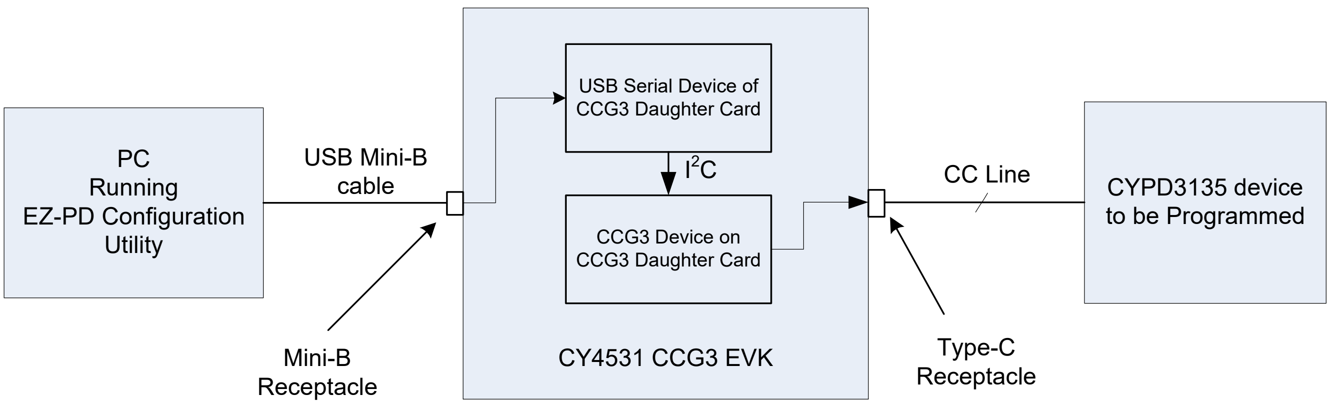
Figure 8. Application Firmware Update over I²C Interface



Application Firmware Update over CC Line

This method primarily applies to the CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4531 CCG3 EVK is connected to the system containing the CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

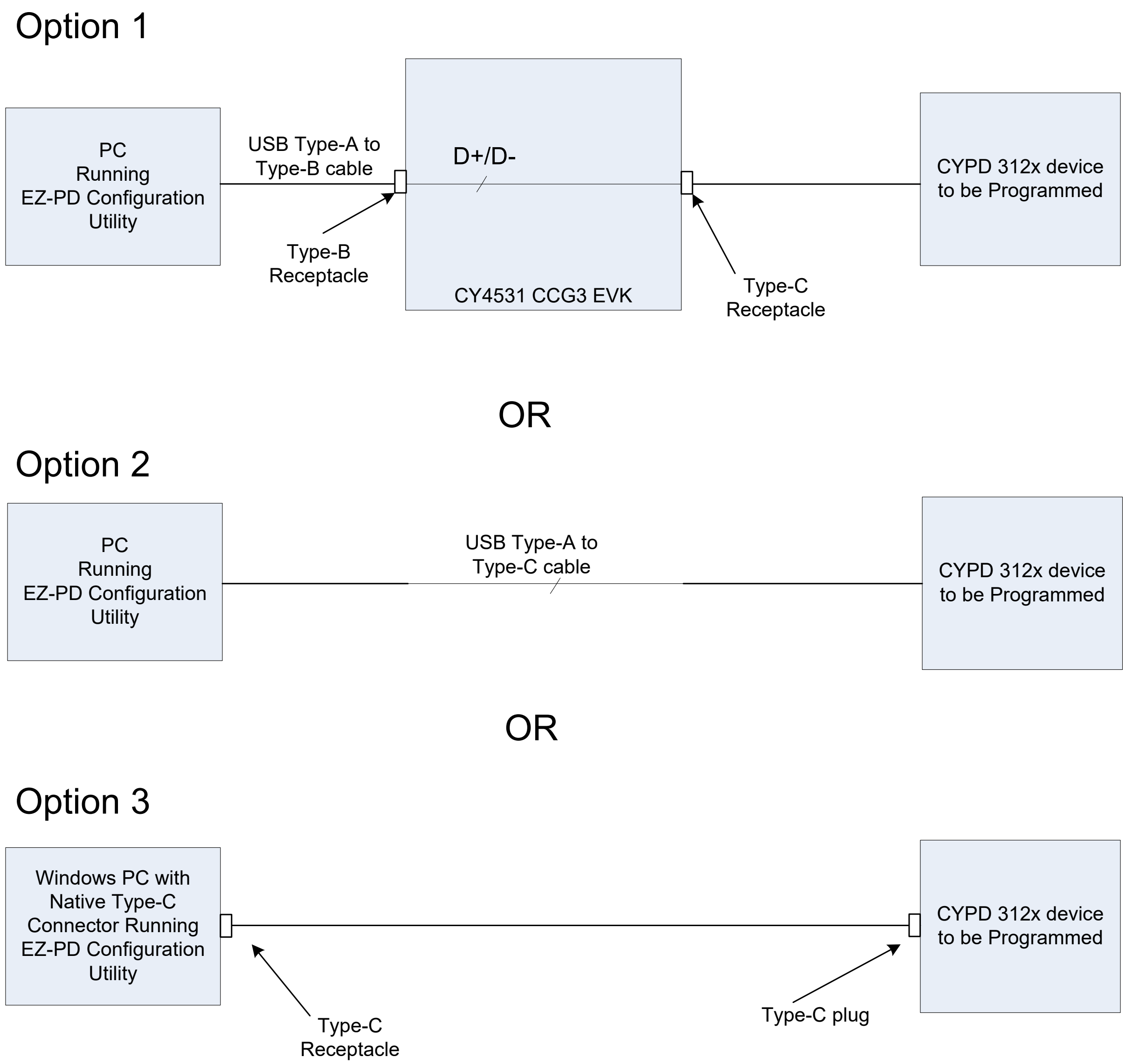
Figure 9. Application Firmware Update over CC Line



Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531 CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

Figure 10. Application Firmware Update over USB



Applications

Figure 11 illustrates the application diagram of a power adapter using a CCG3 device. In this application, CCG3 is used as DFP (power provider) only. The maximum power profile that can be supported by power adapters is up to 20 V, 100 W using 40-pin QFN CCG3 devices. CCG3 has the ability to drive both types of FETs and the state of GPIO P1.0 (floating or grounded) indicates the type of FET (N-MOS or P-MOS FET) being used in the power provider path.

CCG3 integrates all termination resistors and uses GPIOs (VSEL0 and VSEL1) to indicate the negotiated power profile. If required, the power profile can also be selected using CCG3 serial interfaces (I^2C, SPI) or PWM. The VBUS voltage on the Type-C port is monitored using internal circuits to detect under-voltage and overvoltage conditions. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is provided with a resistor connected to the VBUS_DISCHARGE pin of the CCG3 device.

Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor using the “OC” and “VBUS_P” pins of the CCG3 device. The VBUS provider through the Type-C connector can be turned on or off using the provider path FETs.

The power provider FETs are controlled by high-voltage gate driver outputs (VBUS_P_CTRL0 and VBUS_P_CTRL1 pins of CCG3 device). The CCG3 device is also capable of supporting proprietary charging protocols over the DP and DM lines of the Type-C receptacle. By providing a 5-V source at the V5V pin of the CCG3 device, the device becomes capable of delivering the VCONN supply over either the CC1 or CC2 pins of the Type-C connector.

The CCG3 family's power adapter parts are shipped with bootloader and application firmware with limited functionality. Its purpose is to facilitate application flashing over CC line using the EZ-PD Configuration Utility. The power adapter requires an explicit power contract to be negotiated prior to enabling the EZ-PD Configuration utility to flash the application firmware. This application firmware, based on the state of the GPIO (P1.0), determines the type of provider load switch (NFET/PFET) and supplies the 5-V VBUS over Type-C.

Figure 11. Power Adapter Application Diagram (40-QFN Device)

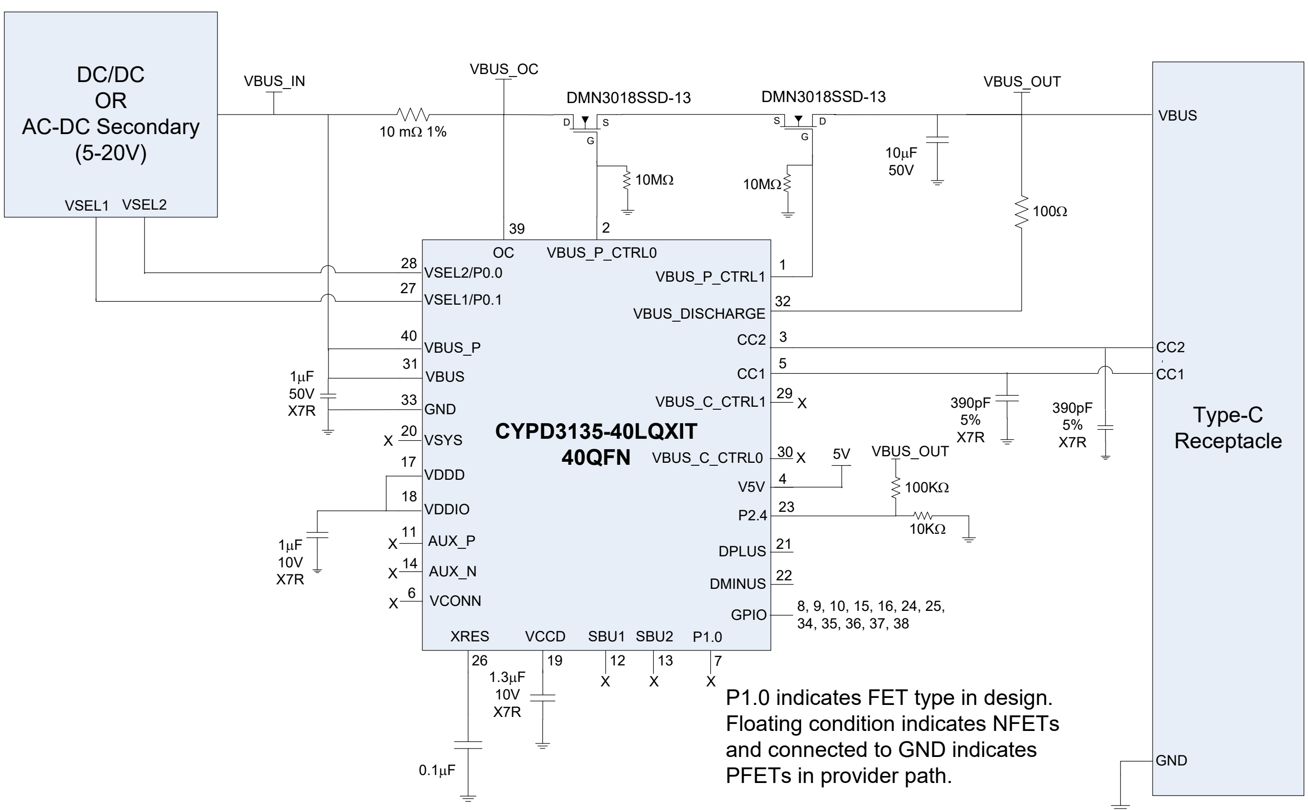


Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)

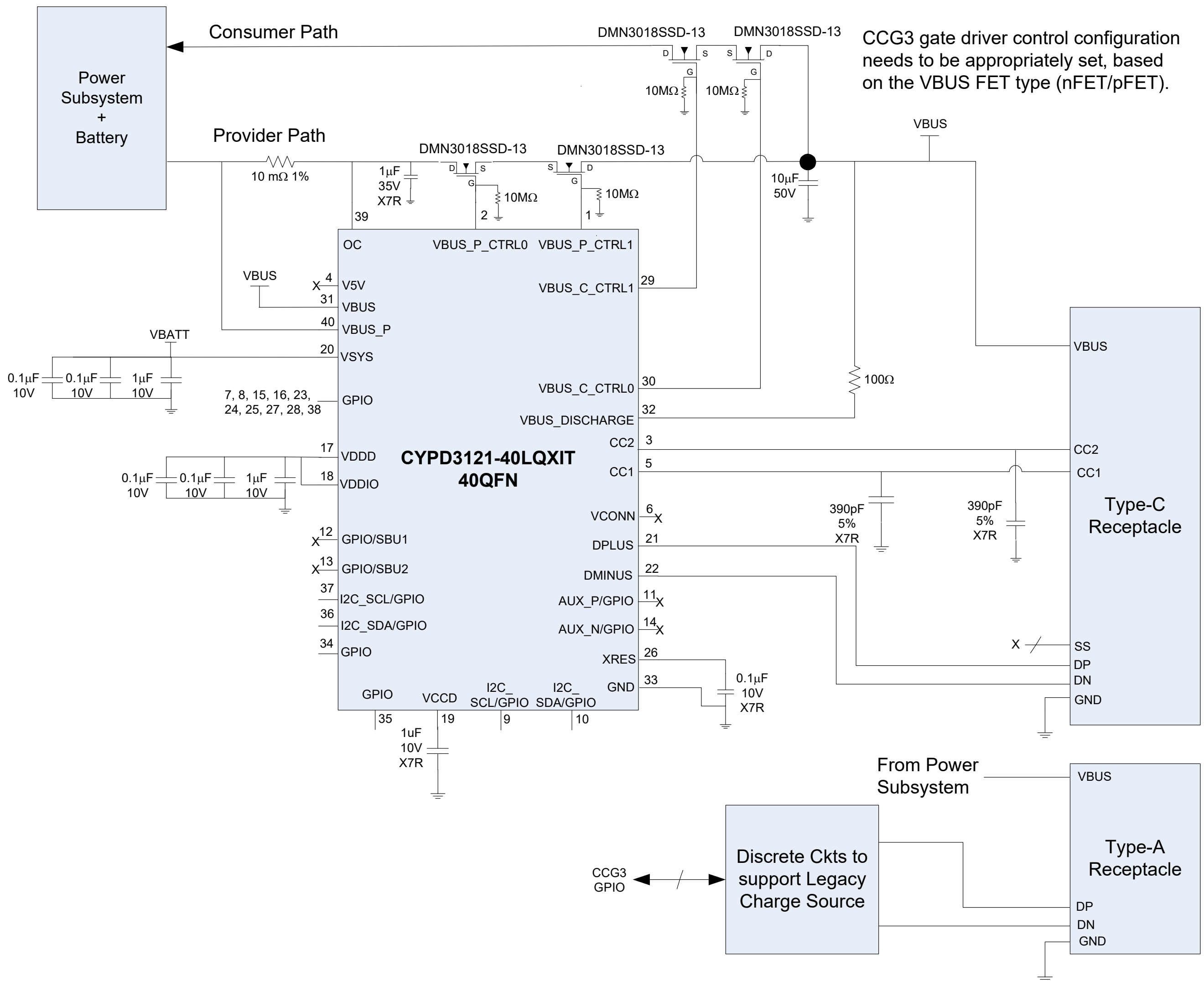


Figure 13 illustrates a USB Type-C to DisplayPort (4-lane) adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has a DisplayPort interface.

The application meets the requirements described in Section 4.2 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0 (Scenarios 2a and 2b USB Type-C to DisplayPort Cables).

Figure 13. USB Type-C to DisplayPort Adapter Application Diagram

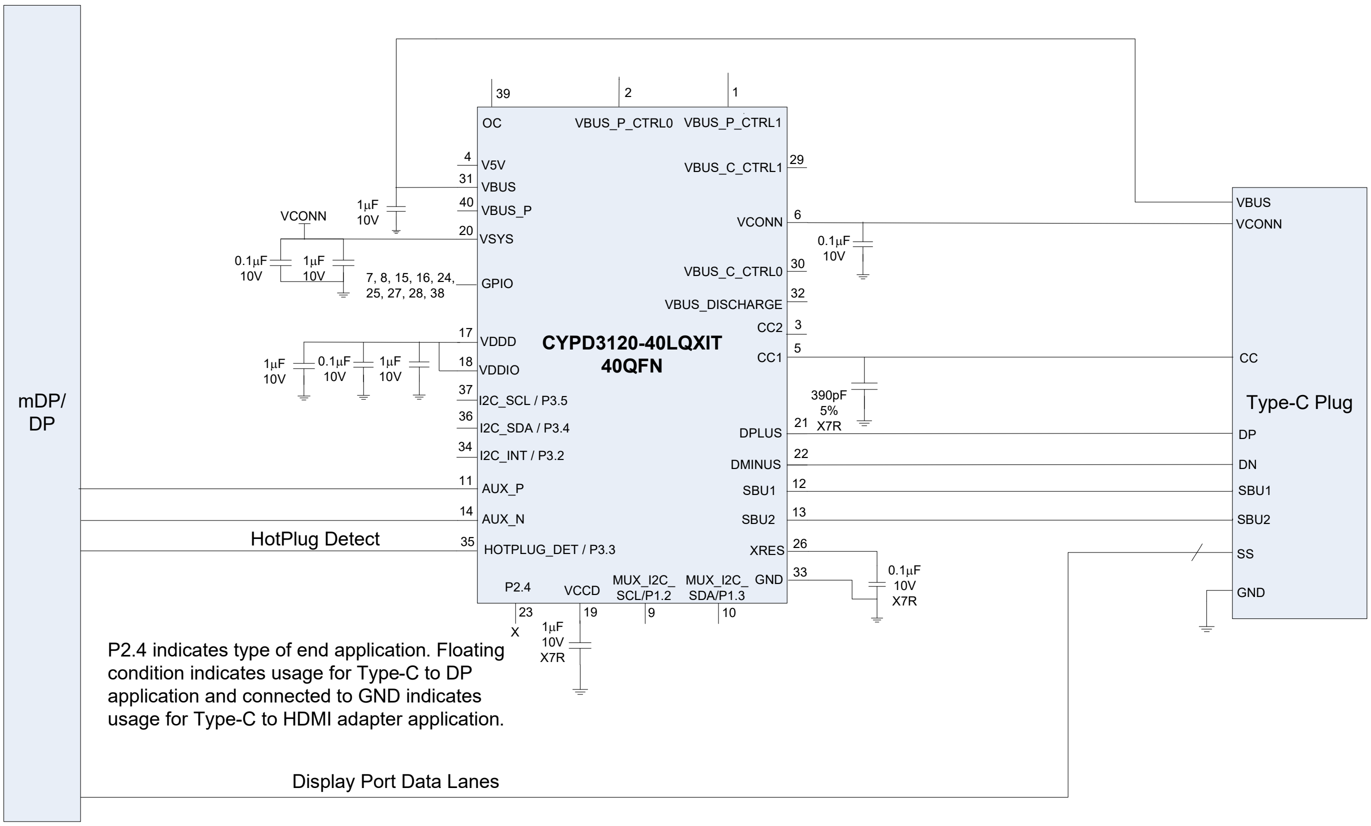


Figure 14 illustrates a USB Type-C to HDMI adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz.

Figure 14. USB Type-C to HDMI Adapter Application

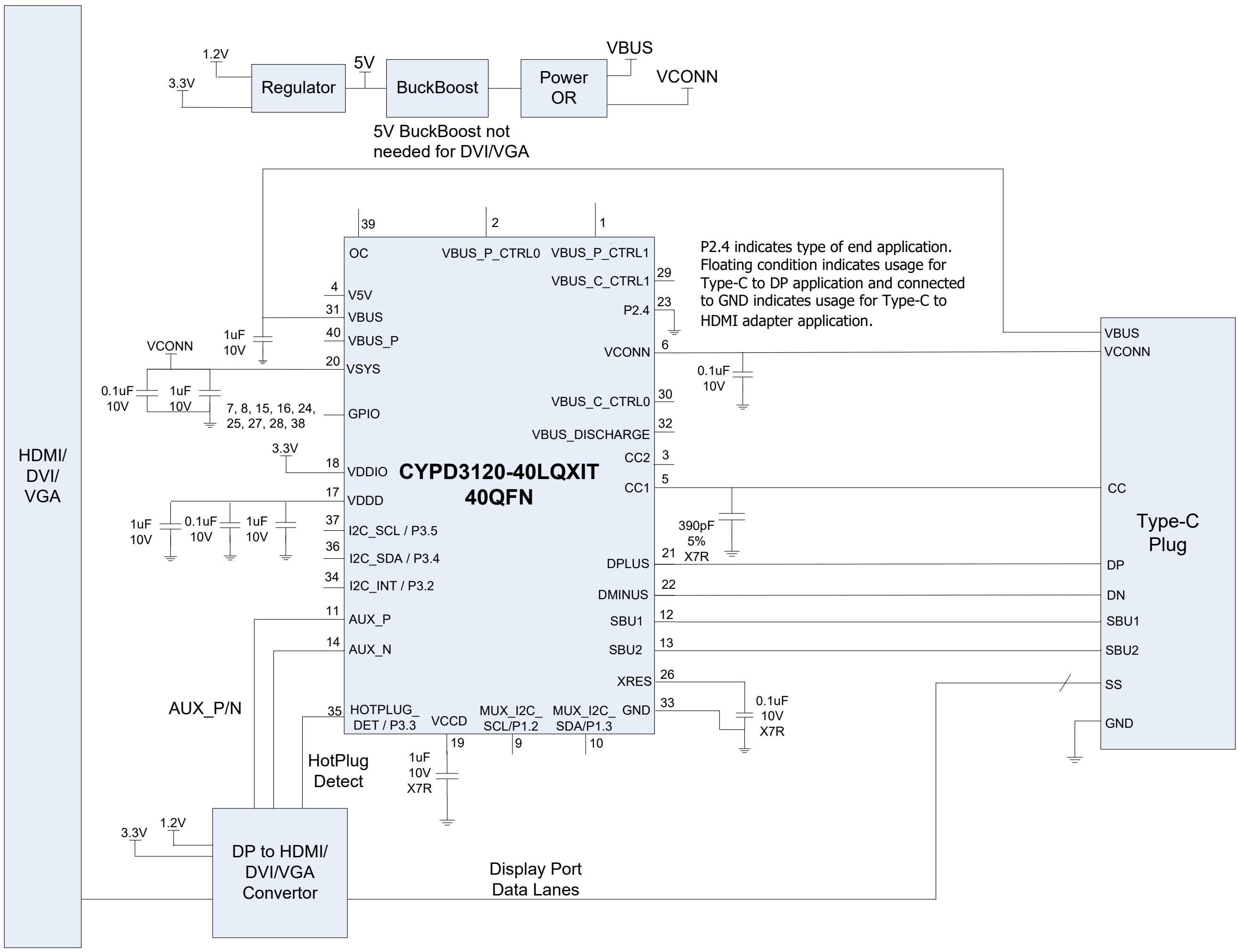


Figure 15 illustrates a Notebook DRP application diagram using a CCG3 device. The Type-C port can be used as a power provider or a power consumer. The CCG3 device communicates with the embedded controller (EC) over I^2C. It also controls the Data Mux to route the HighSpeed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU, SuperSpeed, and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Figure 15. DRP Application Diagram

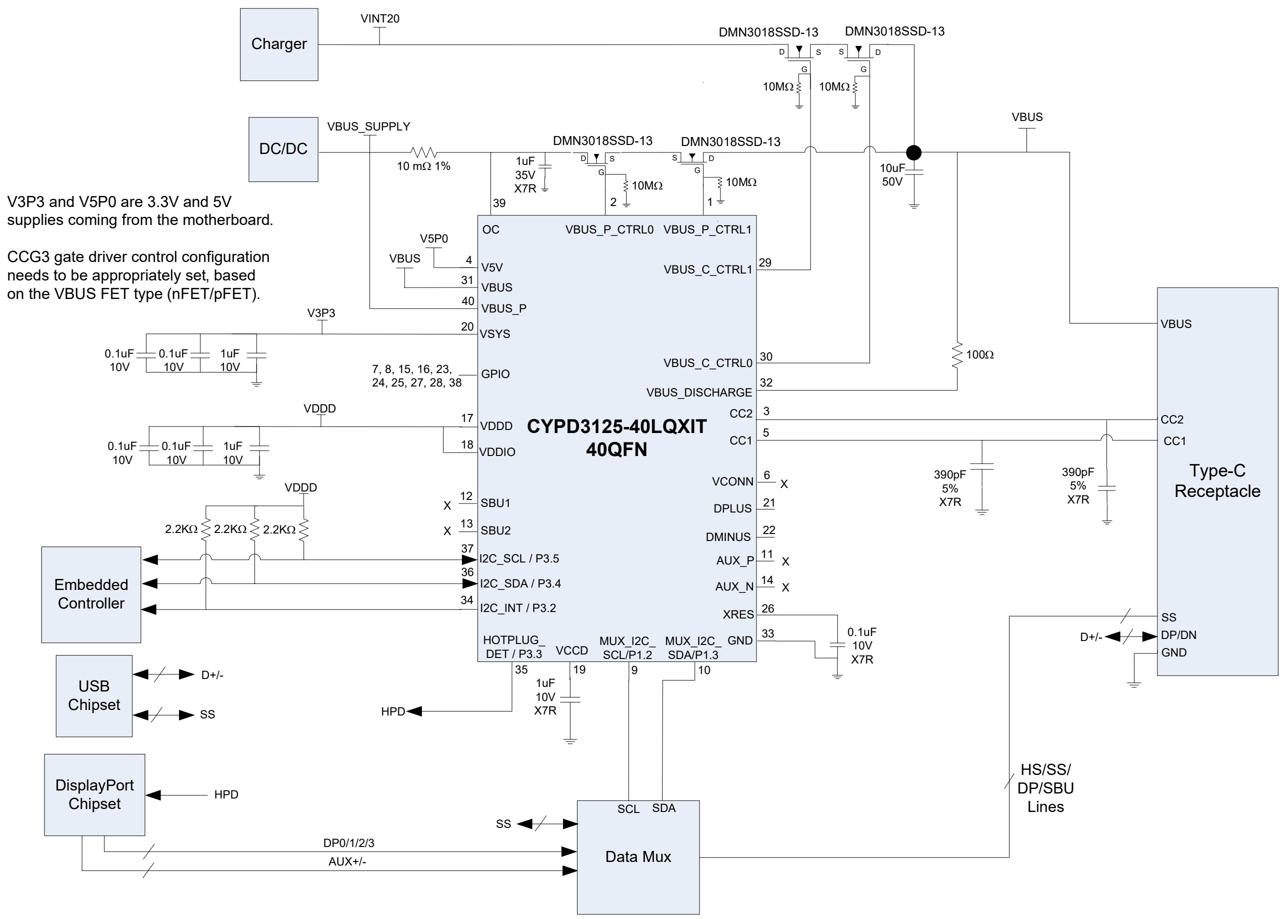
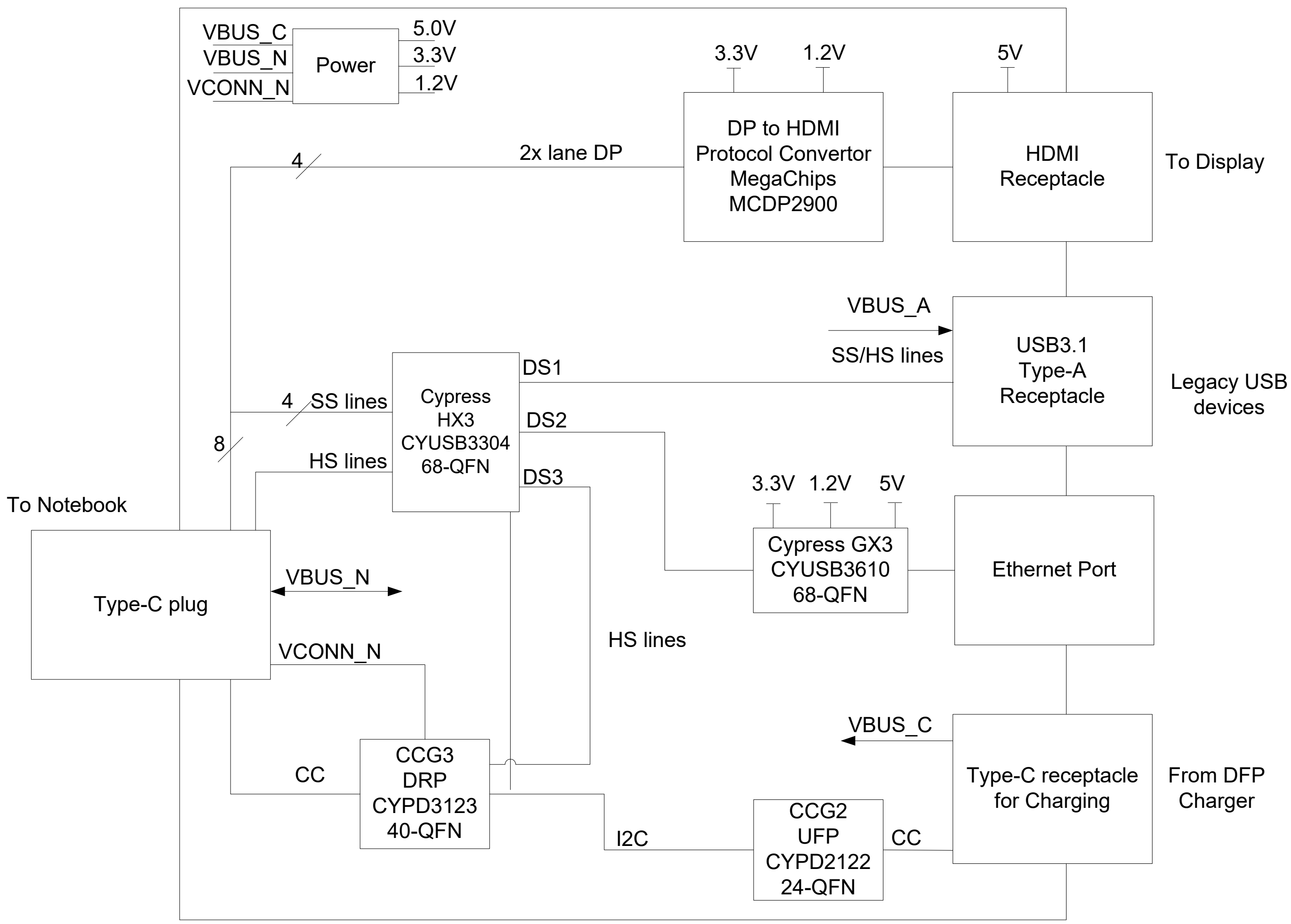


Figure 16 illustrates a CCG3 device based Charge-through Dongle application block diagram. This Charge-through dongle application also implements Cypress's USB SuperSpeed Hub controller HX3 (CYUSB3304-68LTXI) available in 68-QFN package, Low-power single chip USB 3.0 to Gigabit Ethernet Bridge Controller GX3 (CYUSB3610-68LTXC) available in 68-QFN package and the CCG2 (CYPD2122-24LQXI) which acts as an Upstream Facing Port (UFP) and sinks power when connected to USB Type-C chargers.

This application enables connectivity between a USB Type-C Notebook and HDMI Display, legacy USB device and Gigabit Ethernet while also connecting a USB Type-C charging cable. The Charge-Through Dongle solution allows simultaneous HDMI display, Superspeed data transfers, Ethernet connection and charging of a USB Type-C Notebook. Charge-Through Dongle is also widely known as Multiport Adapter. More details including the schematic of the CCG3 device based Charge-through Dongle reference design can be found here.

Figure 16. Charge-through Dongle Application Block Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	
V_{5V}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CONN_MAX}	Max voltage relative to V_{SS}	–	–	6	V	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.

Table 4. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	VSYS	–	2.7	–	5.5	V	UFP Mode.
SID.PWR#1_A	VSYS	–	3	–	5.5	V	DFP/DRP or Gate Driver Modes
SID.PWR#23	VCONN	Power Supply Input Voltage	2.7	–	5.5	V	–
SID.PWR#13	VDDIO	IO Supply Voltage	1.71	–	5.5[2]	V	2.7V < VDDD < 5.5 V
SID.PWR24	VCCD	Output Voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	IDD	Supply current	–	25	–	mA	From VSYS or VBUS VBUS = 5V, T_A = 25 °C / VSYS = 5 V, TA = 25 °C FS USB, CC IO in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	VSYS	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	VSYS	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#1_D	VSYS	Power supply for charger detect/emulation operation	3.15	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR#27	VBUS	Power supply input voltage	3.5	–	21.5	V	FS USB disabled. Total current consumption from VBUS <15 mA.
SID.PwR#28	VBUS	Power supply input voltage for USB operation	4.5	–	21.5	V	FS USB configured, USB Regulator disabled
SID.PWR#30	VBUS_P	Power supply input voltage	4.00	–	21.5	V	
SID.PWR#15	C_{efc}	External regulator voltage bypass for VCCD	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{exc}	Power supply decoupling capacitor for VSYS	0.8	1	–	µF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and TA = 25 °C.							
SID25A	I_{DD20A}	CC, I^2C, WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	VSYS = 3.3 V, T_A = 25 °C, All blocks except CPU are on, CC IO on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							
SID_DS	I_{DD_DS}	VSYS = 3.0 to 3.6 V. CC Attach, I^2C, WDT Wakeup on.	–	30	–	µA	Power Source = VSYS, DFP Mode, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	µA	Power Source = VSYS = 3.3 V, Type-C device not attached, T_A = 25 °C

Note

2. If VDDIO > VDDD, GPIO P2.4 cannot be used. It must be left unconnected. See Table 2 for pin numbers.

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to "Ready to accept I^2C/CC command"	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7× VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO –0.6	–	–	V	I_{OH} = 4 mA at 3V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO –0.5	–	–	V	I_{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization

Table 6. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 10. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 11. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 12. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kb/s	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kb/s	–	–	312	µA	–

Table 13. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 15. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 16. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 17. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 × T_{CPU}	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 18. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 19. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 21. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 22. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–25 °C ≤ T_A ≤ 85 °C, all VDDD
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	All VDDD

Internal Low-Speed OscillatorPower Down

Table 23. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 25. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	R_P_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	R_P_1.5A	DFP CC termination for 1.5A power	166	180	194.4	µA	–
SID.PD.3	R_P_3.0A	DFP CC termination for 3.0A power	304	330	356.4	µA	–
SID.PD.4	R_D	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	R_D_DB	UFP Dead Battery CC termination on CC1 and CC2, valid for 1.5A and 3.0A R_P termination values	4.08	5.1	6.12	kΩ	UFP Dead Battery CC termination on CC1 and CC2. For Default R_P termination, the voltage on CC1 and CC2 is guaranteed to be <1.32 V.
SID.PD.6	R_A	EMCA cable termination	0.8	1.0	1.2	kΩ	All supplies forced to 0 V and 0.2 V applied at VCONN.
SID.PD.7	R_A_OFF	EMCA cable termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at VCONN with R_A disabled.

Table 25. PD DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.8	R_{leak_1}	VCONN leaker for 0.1-μF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge.
SID.PD.9	R_{leak_2}	VCONN leaker for 0.5-μF load	–	–	43.2	kΩ	
SID.PD.10	R_{leak_3}	VCONN leaker for 1.0-μF load	–	–	21.6	kΩ	
SID.PD.11	R_{leak_4}	VCONN leaker for 2.0-μF load	–	–	10.8	kΩ	
SID.PD.12	R_{leak_5}	VCONN leaker for 5.0-μF load	–	–	4.32	kΩ	
SID.PD.13	R_{leak_6}	VCONN leaker for 10-μF load	–	–	2.16	kΩ	
SID.PD.14	I_{leak}	Leaker on VCONN for discharge upon cable detach	150	–	550	μA	–
SID.PD.15	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–400	–	400	mV	Relative to the remote BMC transmitter. Guaranteed by characterization.

Table 26. CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CSA.1	Out_E_Trim_15_DS	Overall Error at Av = 15 using deep sleep reference	–7.00	–	7.00	%	Guaranteed by characterization.
SID.CSA.2	Out_E_Trim_15_BG	Overall Error at Av = 15 using bandgap reference	–4.50	–	4.50	%	Guaranteed by characterization.
SID.CSA.3	Out_E_Trim_100	Overall Error at Av = 100 using either bandgap or deep sleep reference	–24.50	–	24.50	%	–

Table 27. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold Accuracy, $V_{BUS} \leq 16$ V	–6		6	%	Tested at VBUS = 3.75 V, 4.5 V, 5.25 V, 12 V, 16 V
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold Accuracy, $V_{BUS} > 16$ V	–10		10	%	Tested at VBUS = 20 V

Gate Driver Specifications

Table 28. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
DC.NGDO.1	VGS1	Gate to Source Overdrive	5	–	16.5	V	1. Gate driver Supply Voltage ≥ 5V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.2	VGS2	Gate to Source Overdrive	3.75	–	16.5	V	1. Gate driver Supply Voltage ≥ 3.75V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.6	R_{PD}	Resistance when "pull down" enabled	–	–	5	kΩ	–

Table 29. Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.NGDO.1	T_{ON}	Gate turn-on time to gate_driver_supply_voltage + 5V for supply voltage ≥ 5V and VBUS * 2 for supply voltage < 5V	–	–	1	ms	1. Gate driver configuration = NFET 2. Load = The gate of a SI9936 MOSFET

SBU

Table 30. Analog Crossbar Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SBU.1	Ron_sw	Switch ON Resistance	–	–	10	Ω	Voltage input from 0 V to 3.6 V
SID.SBU.2	Rpu_aux_1	AUX_P/N Pull-up Resistance – 100k	80	–	120	kΩ	–
SID.SBU.3	Rpu_aux_2	AUX_P/N Pull-up Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.4	Rpd_aux_1	AUX_P/N Pull-down Resistance – 100k	80	–	120	kΩ	–
SID.SBU.5	Rpd_aux_2	AUX_P/N Pull-down Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.6	Rpd_aux_3	AUX_P/N Pull-down Resistance – 470k	329	–	611	kΩ	–
SID.SBU.7	Rpd_aux_4	AUX_P/N Pull-down Resistance – 4.7M	3.29	–	6.11	MΩ	–

Charger Detect

Table 31. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CD.1	VDAT_REF	BC1.2 Data Detect Voltage Threshold	250	–	400	mV	–
SID.CD.2	VDM_SRC	BC1.2 DM Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.3	VDP_SRC	BC1.2 DP Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.4	IDM_SINK	BC1.2 DM Current Sink	25	–	175	µA	–
SID.CD.5	IDP_SINK	BC1.2 DP Current Sink	25	–	175	µA	–
SID.CD.6	IDP_SRC	BC1.2 DP DCD Current Source	7	–	13	µA	–
SID.CD.7	RDP_UP	USB FS DP Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.8	RDM_UP	USB FS DM Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.9	RDP_DWN	USB FS DP Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.10	RDM_DWN	USB FS DM Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.11	RDAT_LKG	DP/DM Data Line Leakage Termination	300	–	500	kΩ	The charger detect function and data line leakage is enabled.
SID.CD.12	RDCP_DAT	BC1.2 DCP Port Resistance between DP and DM	–	–	40	Ω	–
SID.CD.13	VSETH	USB FS Logic Threshold	1.26	–	1.54	V	–

Analog to Digital Converter

Table 32. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	–

Table 33. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Table 34. VBUS_C Regulator DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.20vreg.1	VBUSREG	VBUS regulator output voltage measured at VDDD for VBUS = 4.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 30 mA.
SID.20vreg.2	VBUSREG2	VBUS regulator output voltage measured at VDDD for VBUS = 3.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 15 mA.
SID.20vreg.6	VBUSLINREG	VBUS regulator line regulation for VBUS from 4.5 V to 21.5 V	–	–	0.5	%/V	VBUS supply varied from 4.5 V to 21.5 V and the change in the VDDD measured. Guaranteed by Characterization.
SID.20vreg.8	VBUSLOADREG	VBUS regulator load regulation for VBUS from 4.5 V to 21.5 V	–	–	0.2	%/mA	Supply of 4.5 V - 21.5 V applied on VBUS and the load current swept from 0 to 30 mA. The change in VDDD is measured. Guaranteed by Characterization.

Table 35. VBUS_C Regulator AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.20vreg.1	T_{START}	Regulator Start-up time	–	–	120	µs	Apply VBUS and measure start time on VDDD pin.
AC.20vreg.2	T_{STOP}	Regulator power down time	–	–	1	µs	Time from assertion of an internal disable signal to for load current on VDDD to decrease from 30 mA to 10 µA.

Table 36. VSYS Switch Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.vddsw.1	Res_sw	Resistance from VSYS supply input to the output supply VDDD	–	–	1.5	Ω	Measured with a load current of 5 mA - 10 mA on VDDD.

Memory

Table 37. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	TBULKERASE	Bulk erase time (64k Bytes)	–	–	35	ms	–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	FRET1	Flash retention, $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	FRET2	Flash retention, $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	FRET3	Flash retention, $T_A \leq 105$ °C, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

Ordering Information

Table 38 lists the EZ-PD CCG3 part numbers and features.

Table 38. EZ-PD CCG3 Ordering Information

Part Number	Application	Termination Resistor	Role	Default FW	Package	Si ID
CYPD3120-40LQXIT	Dongle	R_P, R_D[4], R_{D_DB}	UFP	USB Bootloader and Application FW	40-QFN	1D00
CYPD3120-40LQXI						
CYPD3121-40LQXIT	Power Banks	R_P[5], R_D, R_{D_DB}[6]	DRP	USB Bootloader	40-QFN	1D02
CYPD3121-40LQXI						
CYPD3122-40LQXIT	Monitor (DFP)	R_P, R_D, R_{D_DB}	DFP	I^2C Bootloader	40-QFN	1D03
CYPD3122-40LQXI						
CYPD3123-40LQXIT	Charge-through Dongle	R_P, R_D, R_{D_DB}	DRP	USB Bootloader and Application FW	40-QFN	1D09
CYPD3123-40LQXI						
CYPD3125-40LQXIT	Notebooks, Smartphones	R_P, R_D, R_{D_DB}	DRP	I^2C Bootloader	40-QFN	1D04
CYPD3125-40LQXI						
CYPD3126-42FNXIT	DRP	R_P, R_D[4], R_{D_DB}	DRP	I^2C Bootloader	42-CSP	1D07
CYPD3135-32LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW[7]	32-QFN	1D08
CYPD3135-32LQXQ						
CYPD3135-40LQXIT	Power Adapter	R_P	DFP	CC Bootloader and Application FW[7]	40-QFN	1D05
CYPD3135-40LQXI						
CYPD3135-40LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW[7]	40-QFN	1D05
CYPD3135-40LQXQ						

Ordering Code Definitions

CY PD X X XX - XX XX X X X

- T = Tape and Reel
- Temperature Grade: I = Industrial (–40 °C - 85 °C), Q = Extended industrial (–40 °C - 105 °C)
- Lead: X = Pb-free
- Package Type: FN = CSP; LQ = QFN
- Number of pins in the package
- Application and Feature Combination Designation
- Number of Type-C Ports: 1 = 1 Port, 2 = 2 Port
- Product Type: 3 = Third-generation product family, CCG3
- Marketing Code: PD = Power Delivery product family
- Company ID: CY = Cypress

Notes

3. Termination resistor denoting an EMCA.
4. Termination resistor denoting an upstream facing port.
5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting dead battery termination.
7. The CYPD3135 parts are shipped with bootloader and application firmware with limited functionality. Its purpose is to facilitate application flashing over CC line using the EZ-PD Configuration Utility. The power adapter requires an explicit power contract to be negotiated prior to enabling the EZ-PD Configuration utility to flash the application firmware. This application firmware, based on the state of the GPIO (P1.0), determines the type of provider load switch (NFET/PFET) and supplies the 5V VBUS over Type-C.

Packaging

Table 39. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	17	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	2	°C/W
T_{JA}	Package θ_{JA} (42-ball WLCSP)	–	–	–	34	°C/W
T_{JC}	Package θ_{JC} (42-ball WLCSP)	–	–	–	0.3	°C/W
T_{JA}	Package θ_{JA} (32-pin QFN)	–	–	–	18	°C/W
T_{JC}	Package θ_{JC} (32-pin QFN)	–	–	–	4	°C/W

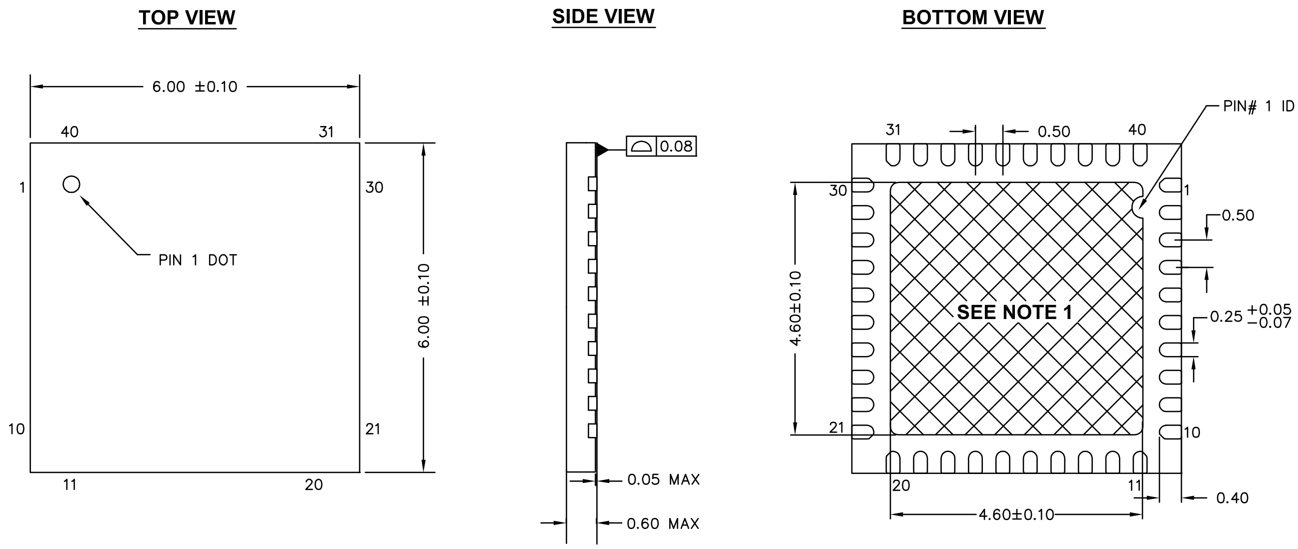
Table 40. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds
42-ball WLCSP	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
42-ball WLCSP	MSL 1
40-pin QFN	MSL 3
32-pin QFN	MSL 3

Figure 17. 40-pin QFN Package Outline, 001-80659

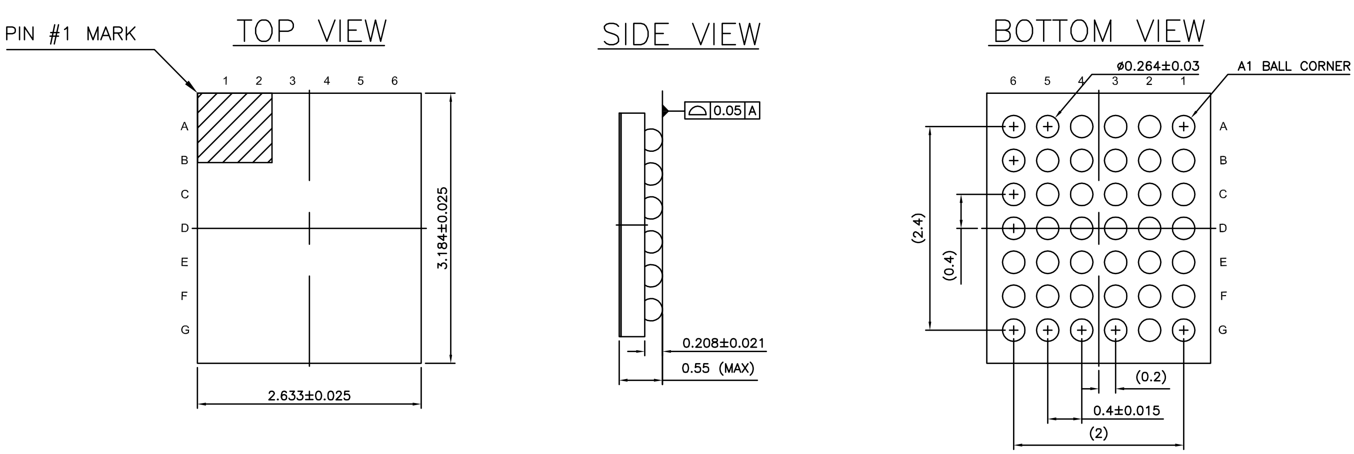


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

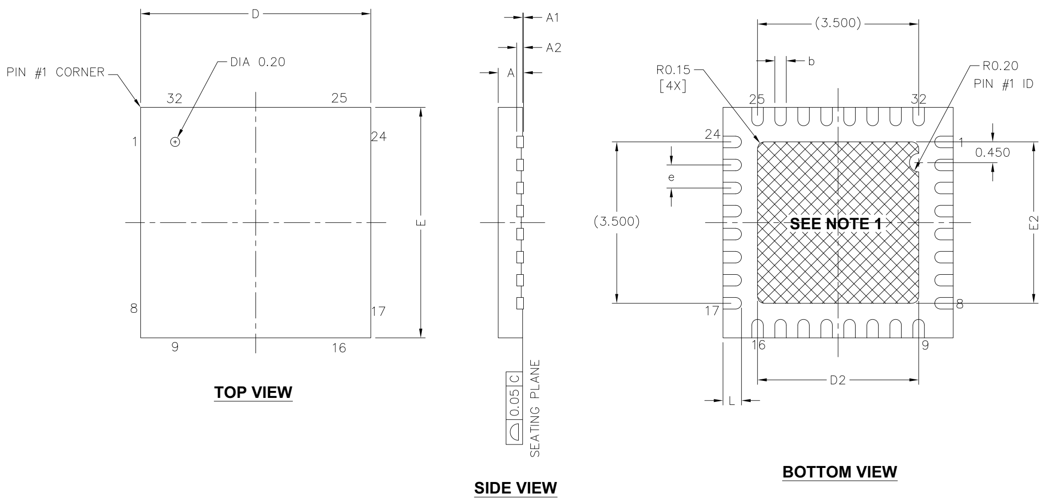
Figure 18. 42-ball CSP Package Outline, 002-04062



002-04062 *A

ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

Figure 19. 32-pin QFN Package Outline, 001-42168



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	-	0.020	0.045
A2	0.15 BSC		
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
b	0.18	0.25	0.30
e	0.50 TYP		

NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *F

Acronyms

Table 42. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunder-bolt™	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG2 pins used to connect to a USB port
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4905678	VGT	09/11/2015	New data sheet.
*A	4953333	VGT	10/08/2015	Updated General Description: Updated the number of GPIOs to 20. Updated Functional Overview: Updated GPIO: Updated the number of GPIOs to 20. Updated Pinouts: Updated Table 2. Updated Figure 4. Added Figure 6.
*B	5007726	VGT	11/25/2015	Changed status from Advance to Preliminary. Updated Features. Added EZ-PD CCG3 Block Diagram. Updated Functional Overview: Updated USB-PD Subsystem (USBPD SS) (Updated description). Added Full-Speed USB Subsystem. Updated Pinouts: Updated Table 2. Updated Figure 4. Updated Figure 6. Added Applications. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 3. Updated Device-Level Specifications: Updated Table 4. Updated Table 5. Updated I/O: Updated Table 6. Updated XRES: Updated Table 8. Updated System Resources: Updated Power-on-Reset (POR) with Brown Out SWD Interface: Updated Table 18. Updated Table 19. Updated Table 20. Updated Internal Main Oscillator: Updated Table 22. Updated Internal Low-Speed OscillatorPower Down: Updated Table 23. Updated Table 24. Updated Internal Low-Speed OscillatorPower Down: Updated Table 25.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	5007726	VGT	11/25/2015	Updated Analog to Digital Converter: Updated Table 32. Updated Table 33. Updated Packaging: Added Figure 18 (spec 002-04062 *A).
*C	5080470	VGT	01/11/2016	Updated General Description. Updated Features. Updated Logic Block Diagram. Updated Power Systems Overview. Updated Pinouts: Updated Table 2. Added table “CCG3 Pin Description for 16-SOIC Device”. Added figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure . Updated Figure 11. Updated figure “Power Adapter Application Diagram (16-SOIC Device)”. Updated Figure 15. Updated Ordering Information. Updated Packaging: Added spec 51-85022 *E. Added Errata.
*D	5137796	VGT	03/09/2016	Updated Pinouts: Updated table “CCG3 Pin Description for 16-SOIC Device”. Updated figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure 11. Updated Figure 12. Updated Ordering Information Updated Errata. Updated to new template.
*E	5240836	VGT	04/28/2016	Updated General Description: Updated description. Updated Features: Updated Type-C and USB-PD Support: Updated description. Updated Packages: Updated description. Updated Logic Block Diagram. Updated Functional Overview: Updated Integrated Billboard Device: Updated description. Updated USB-PD Subsystem (USBPD SS): Updated description. Added Figure 2 and Figure 5.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	5240836	VGT	04/28/2016	Updated Power Systems Overview: Updated description. Updated Figure 3. Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to VDDIO pin. Removed table “CCG3 Pin Description for 16-SOIC Device”. Removed figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Removed figure “Power Adapter Application Diagram (16-SOIC Device)”. Added Figure 12. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated details in “Details/Conditions” column corresponding to “SID.PWR#1_A” Spec ID and “V_{SYS}” parameter. Replaced “V_{DDD}” with “5.5” in “Max” column corresponding to “SID.PWR#13” Spec ID and “V_{DDIO}” parameter. Added “SID.PWR#13_A” Spec ID corresponding to “V_{DDIO}” parameter and its details. Added “SID.PWR#1_C” and “SID.PWR#1_D” Spec IDs corresponding to “V_{SYS}” parameter and its details. Replaced “enabled” with “disabled” in “Details/Conditions” column corresponding to “SID.PwR#28” Spec ID and “V_{BUS}” parameter. Updated details in “Description” and “Details/Conditions” columns corresponding to “SID307” Spec ID and “I_{DD_XR}” parameter. Updated System Resources: Added Gate Driver Specifications, Charger Detect. Updated Ordering Information: Updated part numbers. Updated details in “Application” column corresponding to part number “CYPD3121-40LQXIT”. Updated Ordering Code Definitions Updated Packaging: Removed spec 51-85022 *E. Removed Errata.
*F	5342389	VGT	07/28/2016	Added Available Firmware and Software Tools, CCG3 Programming and Bootloading, and References and Links to Applications Collaterals. Added descriptive notes for the application diagrams. Updated Features, Applications and Timer/Counter/PWM Block (TCPWM). Updated Table 2 through Table 6, Table 18, Table 19, Table 22, Table 23, Table 25, and Table 31 through Table 38. Updated Figure 7, Figure 8, Figure , Figure 11, and Figure 19 (package diagram spec 001-42168 *E). Added Figure 5, Figure 13, and Figure 14. Added Table 26, Table 27, Table 37, and Table 39 through Table 41. Added VDM in Acronyms. Updated Cypress logo and copyright information.
*G	5449433	VGT	09/26/2016	Added Table 34 through Table 36. Updated Table 3, Table 4, Table 6, and Table 37. Updated Copyright and Disclaimer. Added Compliance information in Sales, Solutions, and Legal Information.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	5514508	VGT	01/13/2017	Removed Preliminary document status. Updated Sales information and Copyright details. Added Gate Driver Specifications in Table 28 and Table 29. Updated Applications. Added Figure 16. Updated Ordering Information: Added "CYPD3123-40LQXIT" part number. Removed "CYPD3105-42FNXIT" part number.
*I	5662219	VGT	03/29/2017	Updated Table 2, added non Tape and Reel part numbers and Note 7 in Table 38, Updated description prior to Figure 11.
*J	6032274	VGT	2/21/2018	Updated description of V5V pin in Table 2. Removed parameter SID.PWR#13_A from Table 4. Updated description in USB-PD Subsystem (USBPD SS). Updated Packaging: 32-pin QFN Package Outline, 001-42168 (*E to *F).

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