EiceDRIVER™ 1EDI Compact (1ED-AF)

Single channel isolated gate driver IC with separate output

Features

- Single channel isolated gate driver
- For 600 V/650 V/1200 V IGBTs, MOSFETs and SiC MOSFETs
- Up to 10 A typical peak current at rail-to-rail outputs
- Separate source and sink outputs
- Galvanically isolated coreless transformer driver
- Wide input voltage operating range
- Suitable for operation at high ambient temperature and in fast switching applications
- Small and cost optimized DSO-8 150 mil package with 4 mm creepage
- 40 V absolute maximum output supply voltage

Potential applications

- AC and brushless DC motor drives
- High voltage DC/DC-converter and DC/AC-inverter
- Induction heating resonant application
- UPS-systems
- Commercial air-conditioning (CAC)
- Server and telecom switched mode power supplies (SMPS)
- Solar

Product type	Typical output current and configuration	UVLO	Propagation delay	Package marking
1EDI05I12AF	1.3 A source and sink outputs	12 V	300 ns	1I05I12A
1EDI20I12AF	4.0 A source and sink outputs	12 V	300 ns	1I20I12A
1EDI20N12AF	4.0 A source and sink outputs	9.1 V	120 ns	1I20N12A
1EDI40I12AF	7.5 A source and sink outputs	12 V	300 ns	1I40I12A
1EDI60I12AF	10.0 A source and sink outputs	12 V	300 ns	1I60I12A
1EDI60N12AF	10.0 A source and sink outputs	9.1 V	120 ns	1I60N12A

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 1EDIxxI12AF and 1EDIxxN12AF are galvanically isolated single channel gate driver in a DSO-8 narrow body package that provide output currents up to 10 A at separated output pins.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using scaled CMOS threshold levels to support even 3.3 V microcontrollers.

Data transfer across the isolation barrier is realized by the coreless transformer technology.

Every driver family member comes with logic input and driver output undervoltage lockout (UVLO) and active shutdown.

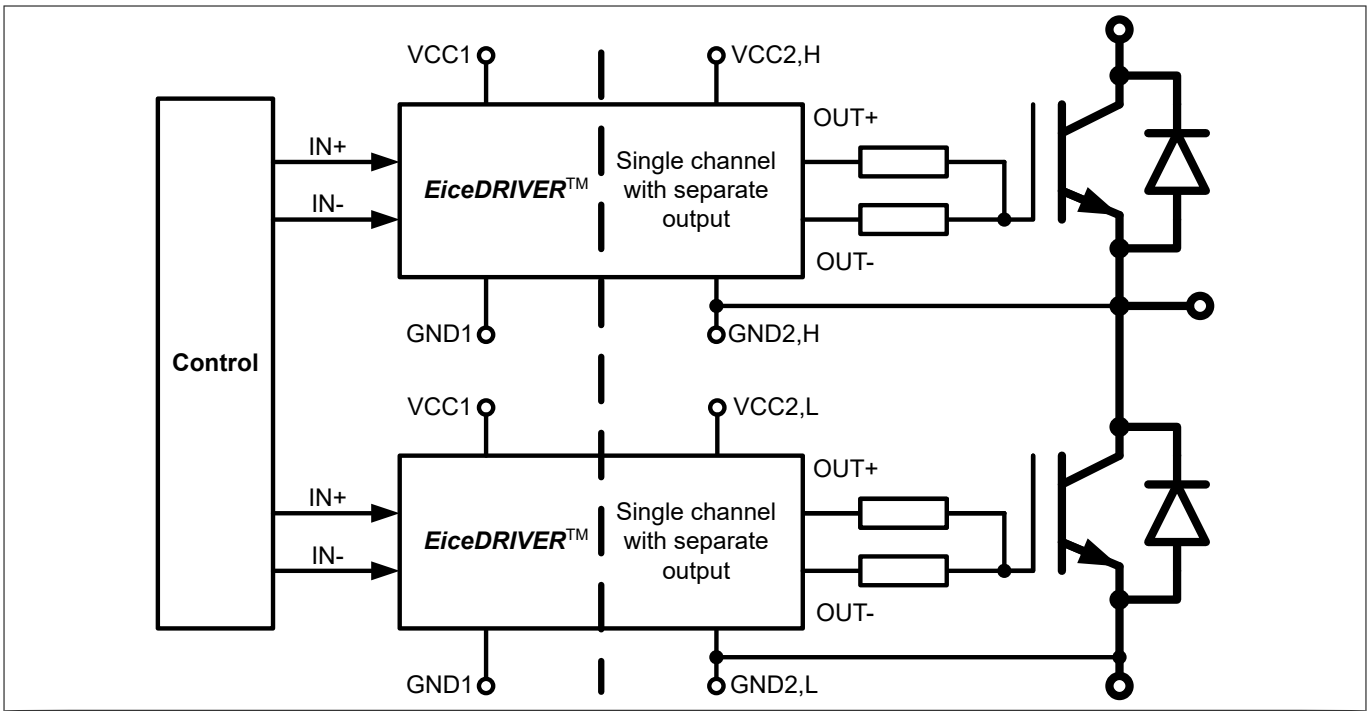

Figure 1 Typical application

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1 Block diagram

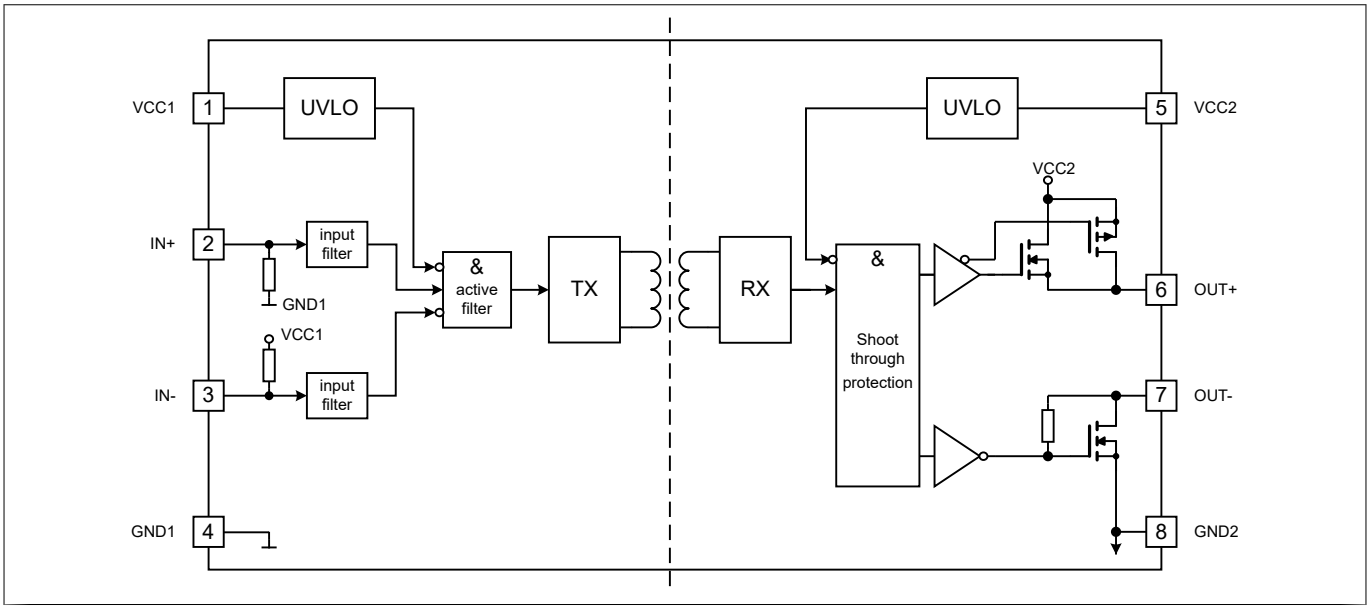


Figure 2 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration

Table 1 Pin configuration

Pin No.	Name	Function
1	*VCC1*	Positive logic supply
2	*IN+*	Non-inverted driver input (active high)
3	*IN-*	Inverted driver input (active low)
4	*GND1*	Logic ground
5	*VCC2*	Positive power supply output side
6	*OUT+*	Driver source output
7	*OUT-*	Driver sink output
8	*GND2*	Power ground

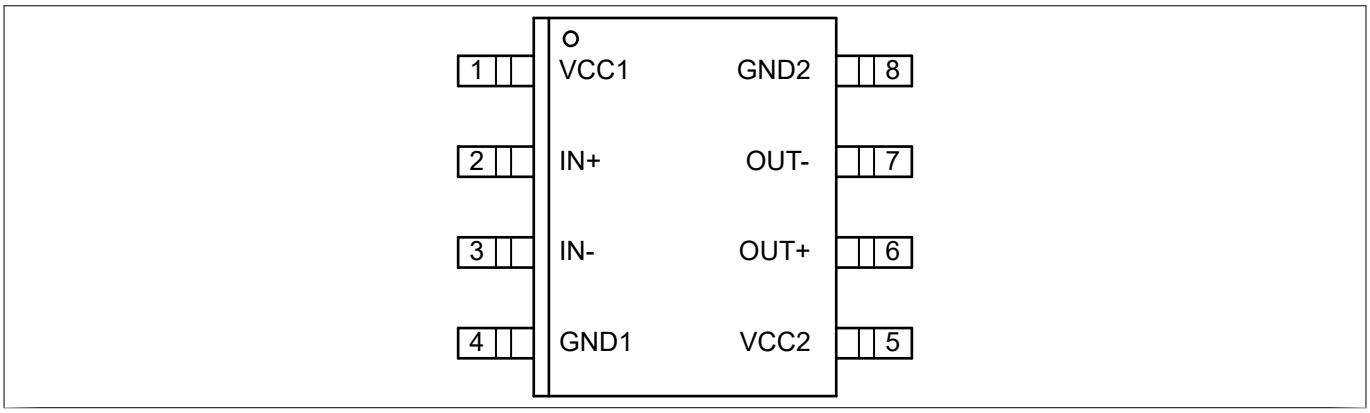


Figure 3 DSO-8 narrow body (top view)

2.2 Pin functionality

VCC1

Logic input supply voltage of 3.3 V up to 15 V wide operating range.

***IN+* non inverting driver input**

IN+ non-inverted control signal for driver output if *IN-* is set to low. (Output sourcing active at *IN+* = high and *IN-* = low)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at *IN+*. An internal weak pull-down-resistor favors off-state.

***IN-* inverting driver input**

IN- inverted control signal for driver output if *IN+* is set to high. (Output sourcing active at *IN-* = low and *IN+* = high)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at *IN-*. An internal weak pull-up-resistor favors off-state.

GND1

Ground connection of input circuit.

***GND2* reference ground**

Reference ground of the output driving circuit.

In case of a bipolar supply (positive and negative voltage referred to IGBT emitter) this pin is connected to the negative supply voltage.

VCC2

Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.

***OUT+* driver source output**

Driver source output pin to turn on external IGBT. During on-state the driving output is switched to *VCC2*. Switching of this output is controlled by *IN+* and *IN-*. This output will also be turned off at an UVLO event.

During turn off the *OUT+* terminal is able to sink approx. 100 mA. In case of an unconnected *OUT-* the complete gate charge is discharged through this channel resulting in a slow turn off.

***OUT-* driver sink output**

Driver sink output pin to turn off external IGBT. During off-state the driving output is switched to *GND2*. Switching of this output is controlled by *IN+* and *IN-*. In case of UVLO an active shut down keeps the output voltage at a low level.

3 Functional description

The 1EDIxxI12AF and 1EDIxxN12AF are general purpose isolated gate drivers. Basic control and protection features support fast and easy design of highly reliable systems.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range supports the direct connection of various signal sources like DSPs and microcontrollers.

The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and enhance dV/dt control.

3.1 Supply

The driver can operate over a wide supply voltage range, either unipolar or bipolar.

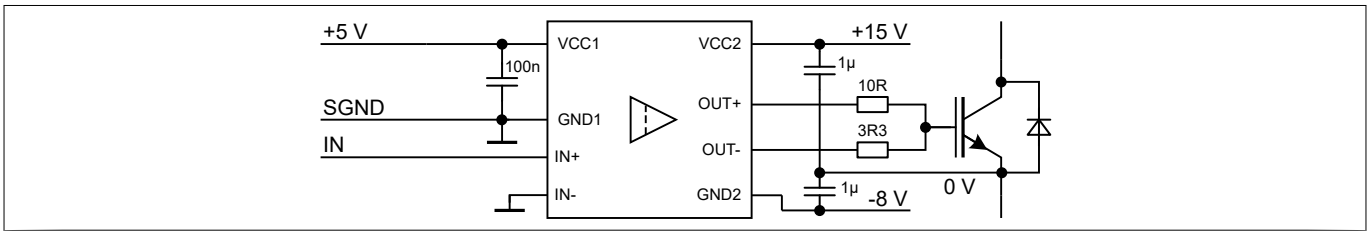


Figure 4 Application example bipolar supply

With bipolar supply the driver is typically operated with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V at *GND2* relative to the emitter of the IGBT. Negative supply can help to prevent a dynamic turn on due to the additional charge which is generated from IGBT's input capacitance.

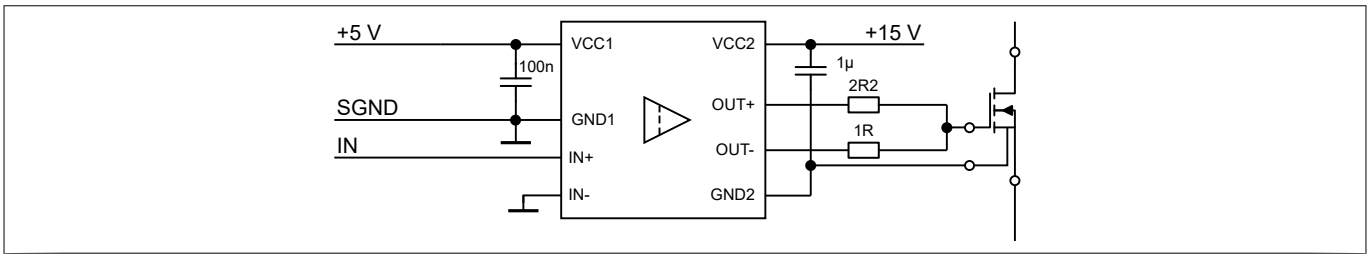


Figure 5 Application example unipolar supply

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15 V at *VCC2*. In this case, careful evaluation for turn off gate resistor selection is recommended to avoid dynamic turn on.

3.2 Protection features

3.2.1 Undervoltage lockout (UVLO)

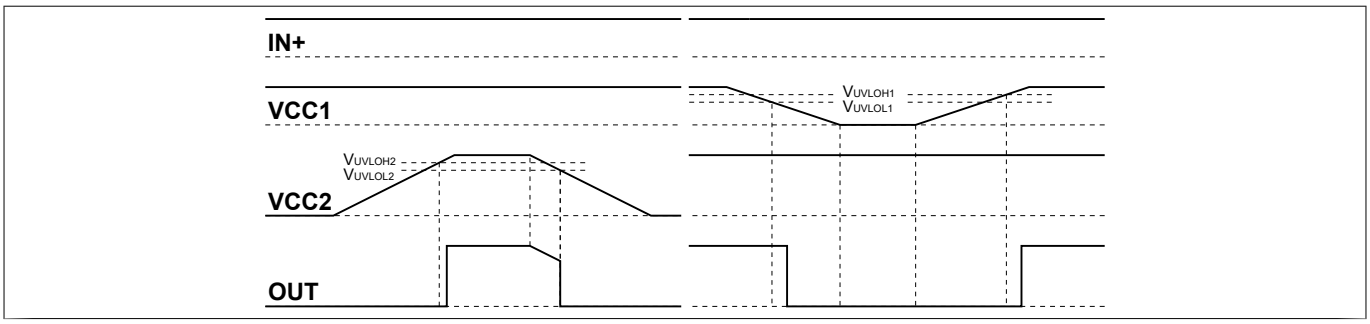


Figure 6 UVLO behavior

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective V_{UVLOH} levels.

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at *IN+* and *IN-* are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

Note: V_{VCC2} is always referred to GND2 and does not differentiate between unipolar or bipolar supply.

3.2.2 Active shut-down

The active shut-down feature ensures a safe IGBT off-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT gate is clamped at *OUT-* to *GND2*.

3.2.3 Short circuit clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An internal protection circuit at *OUT+* limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

3.3 Non-inverting and inverting inputs

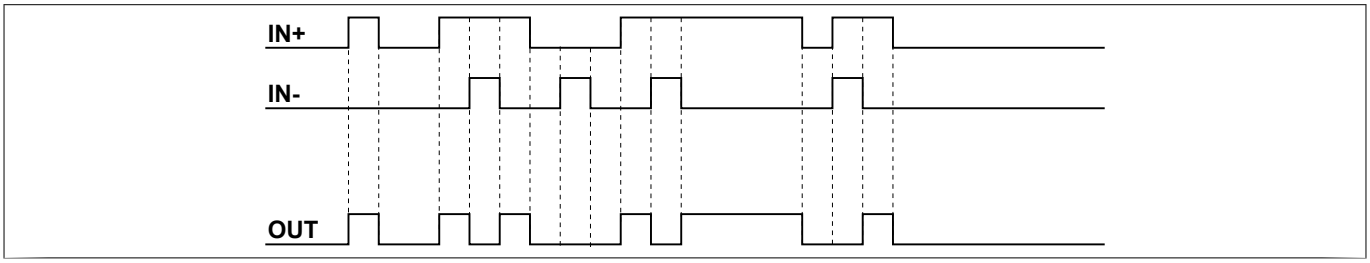


Figure 7 Logic input to output switching behavior

There are two possible input modes to control the IGBT. At non-inverting mode *IN+* controls the driver output while *IN-* is set to low. At inverting mode *IN-* controls the driver output while *IN+* is set to high. A minimum input pulse width is defined to filter occasional glitches.

3.4 Driver outputs

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

4 Electrical parameters

4.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Table 2 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	-0.3	40	V	[1]
Gate driver output	V_{OUT}	V_{GND2}-0.3	V_{VCC2}+0.3	V	[1]
Positive power supply input side	V_{VCC1}	-0.3	18.0	V	–
Logic input voltages (*IN+*,*IN-*)	$V_{LogicIN}$	-0.3	18.0	V	–
Input to output isolation voltage (*GND2*)	V_{GND2}	-1200	1200	V	*GND2 - GND1*
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Comparative tracking index	*CTI*	600	–		IEC 60601-1: Material group II
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	[2] @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	[2] @T_A = 25°C
Thermal resistance (Input side)	$R_{THJA,IN}$	–	145	K/W	[2] @T_A = 85°C
Thermal resistance (Output side)	$R_{THJA,OUT}$	–	165	K/W	[2] @T_A = 85°C
ESD capability	$V_{ESD,HBM}$	–	2	kV	Human body model[3]
	$V_{ESD,CDM}$	–	1	kV	Charged device model[4]

1 With respect to *GND2*.
2 See Figure 11 for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
3 According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
4 According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

4.2 Operating parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Table 3 Operating parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	13	35	V	[5]
Power supply input side	V_{VCC1}	3.1	17	V	–
Logic input voltages (*IN+*,*IN-*)	$V_{LogicIN}$	-0.3	17	V	–
Switching frequency	f_{sw}	–	1.0	MHz	[6][7]
Ambient temperature	T_A	-40	125	°C	–
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	4.8	K/W	[7] at T_A = 85°C
Common mode transient immunity (CMTI)	$\lvert dV_{ISO}/dt \rvert$	–	100	kV/µs	[7] at 1000 V

4.3 Electrical characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3, GND2 for pins 5 to 7).

4.3.1 Voltage supply

Table 4 Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO threshold input chip	V_{UVLOH1}	–	2.85	3.1	V	–
	V_{UVLOL1}	2.55	2.75	–	V	–
UVLO hysteresis input chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.09	0.10	–	V	–
UVLO threshold output chip (1EDIxxI12AF)	$V_{UVLOH2,1}$	–	12.0	12.7	V	[8]
	$V_{UVLOL2,1}$	10.5	11.1	–	V	[8]
UVLO hysteresis output chip ($V_{UVLOH2,1}$ - $V_{UVLOL2,1}$)	$V_{HYS2,1}$	0.70	0.85	–	V	–

(table continues...)

5 With respect to *GND2*.
6 do not exceed max. power dissipation
7 Parameter is not subject to production test - verified by design/characterization
8 With respect to *GND2*.

Table 4 (continued) Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO threshold output chip (1EDIxxN12AF)	$V_{UVLOH2,2}$	–	9.1	10.0	V	8)
	$V_{UVLOL2,2}$	8.0	8.5	–	V	8)
UVLO hysteresis output chip ($V_{UVLOH2,2}$ - $V_{UVLOL2,2}$)	$V_{HYS2,2}$	0.55	0.60	–	V	–
Quiescent current input chip	I_{Q1}	–	0.65	1.0	mA	V_{VCC1} = 5 V *IN+* = High, *IN-* = Low =>*OUT* = High
Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V *IN+* = High, *IN-* = Low =>*OUT* = High

4.3.2 Logic input

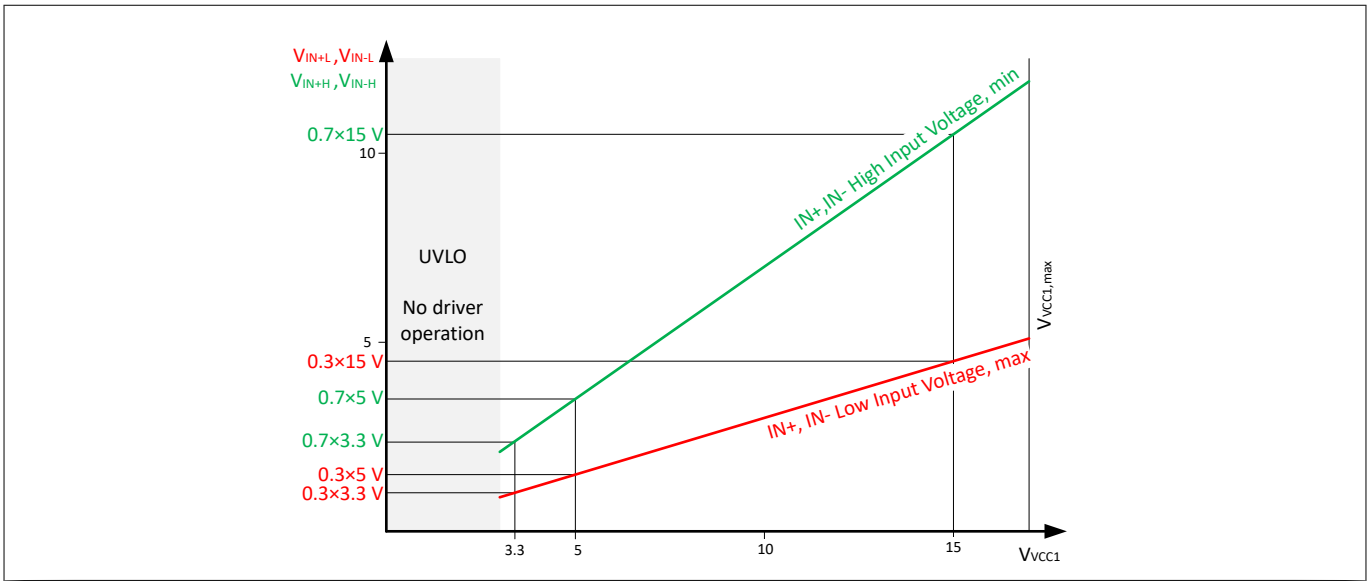


Figure 8 *VCC1* scaled input threshold voltage of *IN+* and *IN-*

Beginning from the input undervoltage lockout level, threshold levels for *IN+* and *IN-* are scaled to V_{VCC1}. The high input threshold is 70% of V_{VCC1} and the low input threshold is at 30% of V_{VCC1}.

8 With respect to *GND2*.

Table 5 Logic input

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
IN+,*IN-* low input voltage	V_{IN+L}, V_{IN-L}	–	–	0.3 × V_{VCC1}		[9] 3.1 V ≤ V_{VCC1} ≤ 17 V
IN+,*IN-* high input voltage	V_{IN+H}, V_{IN-H}	0.7 × V_{VCC1}	–	–		
IN+,*IN-* low input voltage	V_{IN+L}, V_{IN-L}	–	–	1.5	V	V_{VCC1} = 5.0 V
IN+,*IN-* high input voltage	V_{IN+H}, V_{IN-H}	3.5	–	–	V	
IN- input current	I_{IN-}	–	70	200	µA	V_{VCC1} = 5.0 V, V_{IN-} = *GND1*
IN+ input current	I_{IN+}	–	70	200	µA	V_{VCC1} = 5.0 V, V_{IN+} = V_{VCC1}

4.3.3 Gate driver

Note: minimum Peak current rating valid over temperature range!

Table 6 Gate driver

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output peak current (source)	$I_{OUT+,PEAK}$			–	A	[10] [11] *IN+* = High, *IN-* = Low, V_{VCC2} = 15 V
1EDI05I12AF		0.5	1.3			
1EDI20I12AF, 1EDI20N12AF		2.0	4.0			
1EDI40I12AF		4.0	7.5			
1EDI60I12AF, 1EDI60N12AF		6.0	10.0			
Low level output peak current (sink)	$I_{OUT-,PEAK}$			–	A	[10] [11] *IN+* = Low, *IN-* = Low, V_{VCC2} = 15 V
1EDI05I12AF		0.5	0.9			
1EDI20I12AF, 1EDI20N12AF		2.0	3.5			
1EDI40I12AF		4.0	6.8			
1EDI60I12AF, 1EDI60N12AF		6.0	9.4			

9 Parameter is not subject to production test - verified by design/characterization
10 specified min. output current is forced; voltage across the device $V_{(VCC2 - OUT+)}$ or $V_{(OUT- - GND2)}$ < V_{VCC2}.
11 Parameter is not subject to production test - verified by design/characterization

4.3.4 Short circuit clamping

Table 7 Short circuit clamping

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage (*OUT+*) (V_{OUT+} - V_{VCC2})	V_{CLPout}	–	0.9	1.3	V	[12] *IN+* = High, *IN-* = Low, *OUT* = High I_{OUT} = 500 mA, (pulse test t_{CLPmax} = 10 µs)

4.3.5 Dynamic characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V and V_{VCC2} = 15 V.

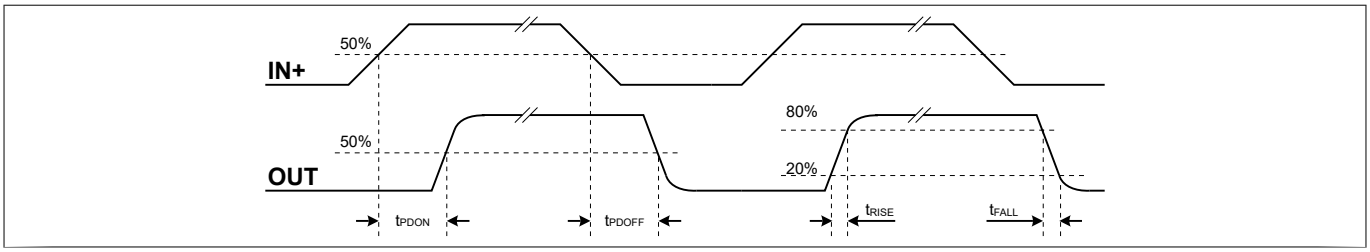


Figure 9 Propagation delay, rise and fall time

Table 8 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	t_{PDON}	270	300	330	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @25°C 1EDIxxI12AF
Input IN to output propagation delay OFF	t_{PDOFF}	270	300	330	ns	
Input IN to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-30	5	40	ns	
Input pulse suppression time *IN+*, *IN-*	t_{MININ+}, t_{MININ-}	230	240	–	ns	
Input IN to output propagation delay ON	t_{PDON}	95	120	142	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @25°C 1EDIxxN12AF
Input IN to output propagation delay OFF	t_{PDOFF}	105	125	150	ns	
Input IN to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-15	5	25	ns	

(table continues...)

12 With respect to *GND2*.

Table 8 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input pulse suppression time *IN+*, *IN-*	t_{MININ+}, t_{MININ-}	30	40	–	ns	
Input IN to output propagation delay ON variation due to temp	t_{PDONt}	–	–	14	ns	[13] C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
Input IN to output propagation delay OFF variation due to temp	t_{PDOFFt}	–	–	14	ns	
Input IN to output propagation delay distortion variation due to temp (t_{PDOFF}-t_{PDON})	$t_{PDISTOt}$	–	–	8	ns	
Rise time	t_{RISE}	–	10	20	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%
Fall time	t_{FALL}	–	9	19	ns	

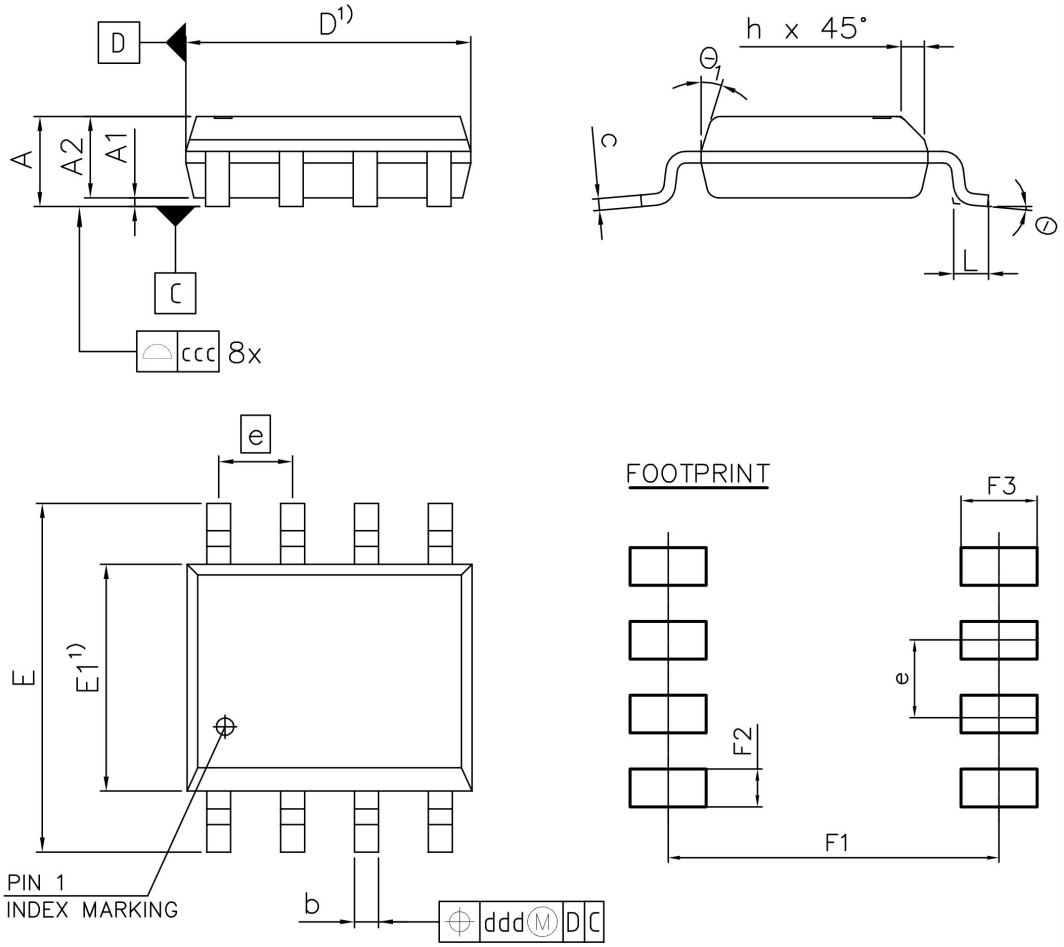
4.3.6 Active shut down

Table 9 Active shut down

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}	–	2.2	2.5	V	[14] I_{OUT-}/$I_{OUT-,PEAK}$=0.1, *VCC2* open

13 Parameter is not subject to production test - verified by design/characterization
14 With respect to *GND2*.

5 Package outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ_1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

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REVISION
02

Figure 10 DSO-8 narrow body (Plastic (green) dual small outline package)

6 Application notes

6.1 Reference layout for thermal data

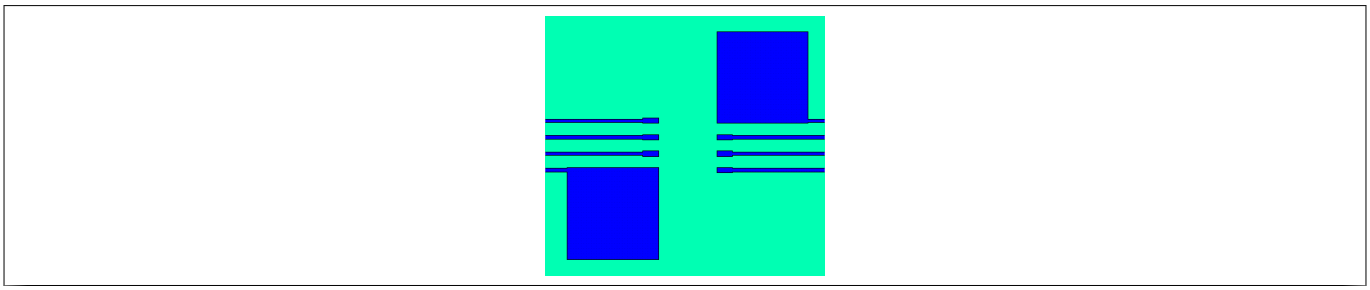

Figure 11 Reference layout for thermal data (Copper thickness 35 µm)

This PCB layout represents the reference layout used for the thermal characterization.

Pin 4 (GND1) and pin 8 (GND2) require each a ground plane of 100 mm^2 for achieving maximum power dissipation. The package is built to dissipate most of the heat generated through these pins.

The thermal coefficient junction-top ($\Psi_{th,jt}$) can be used to calculate the junction temperature at a given top case temperature and driver power dissipation:

$$T_j = \Psi_{\text{th,jt}} \cdot P_D + T_{\text{top}}$$

6.2 Printed circuit board guidelines

The following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and to reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

Revision history

Document version	Date of release	Description of changes
1.10	2023-06-23	Change of template and version numbering system formatting updated for electrical parameters and pins, separate output variant data sheets merged minimum value of t_{RISE} and t_{FALL} removed Added footnote for gate driver output current
2.0	2014-11-10	Completion of parameters and editorial changes
1.01	2014-10-14	Completion of parameters

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