

Automotive-grade N-channel 650 V, 0.024 Ω typ., 69 A, MDmesh™ V Power MOSFET in a TO-247 package

Datasheet - production data

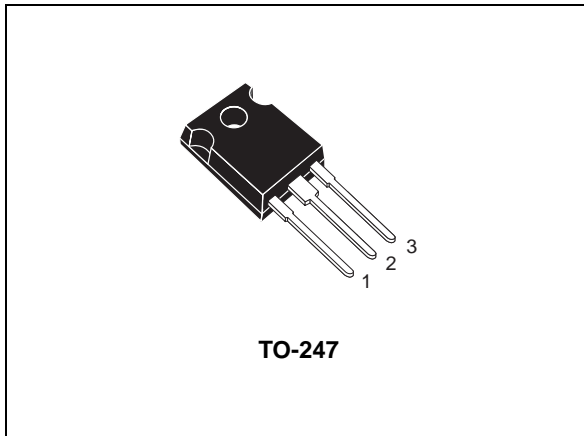
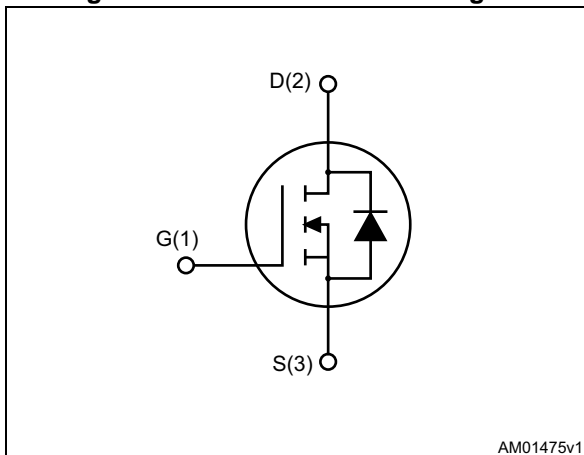


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{jmax.}$	$R_{DS(on) max.}$	I_D
STW78N65M5	710 V	0.032 Ω	69 A

- Designed for automotive applications and AEC-Q101 qualified
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STW78N65M5	78N65M5	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	69	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	41.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	276	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	450	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 69\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
3. $V_{DS} \leq 520\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	0.28	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	15	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	2000	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 34.5\text{ A}$		0.024	0.032	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	9000	-	pF
C_{oss}	Output capacitance		-	210	-	pF
C_{rss}	Reverse transfer capacitance		-	9	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	768	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	205	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	1.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 34.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 16)	-	203	-	nC
Q_{gs}	Gate-source charge		-	50	-	nC
Q_{gd}	Gate-drain charge		-	84	-	nC

- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17) (see Figure 20)	-	163	-	ns
$t_{r(V)}$	Voltage rise time		-	14	-	ns
$t_{f(i)}$	Current fall time		-	14	-	ns
$t_{c(off)}$	Crossing time		-	26	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		69	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		276	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 69\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 69\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	504		ns
Q_{rr}	Reverse recovery charge		-	13		μC
I_{RRM}	Reverse recovery current	$V_{DD} = 100\text{ V}$ (see Figure 17)	-	49		A
t_{rr}	Reverse recovery time	$I_{SD} = 69\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	635		ns
Q_{rr}	Reverse recovery charge		-	19		μC
I_{RRM}	Reverse recovery current		-	59		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

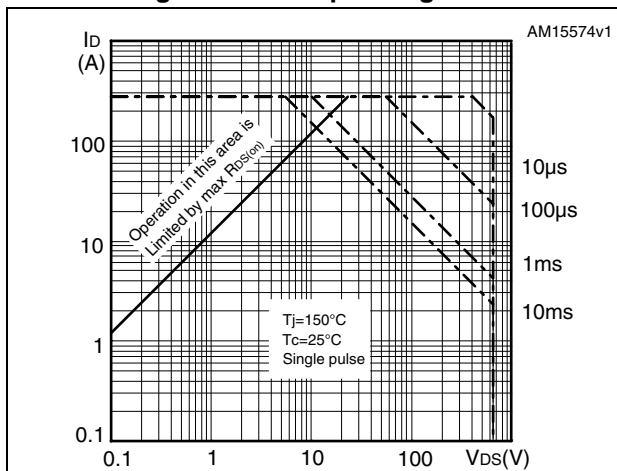


Figure 3. Thermal impedance

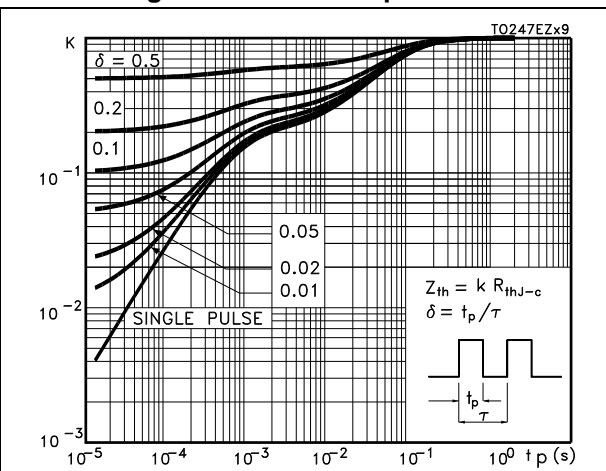


Figure 4. Output characteristics

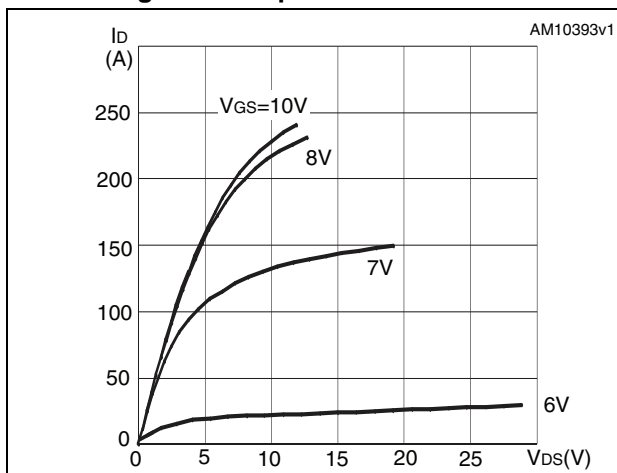


Figure 5. Transfer characteristics

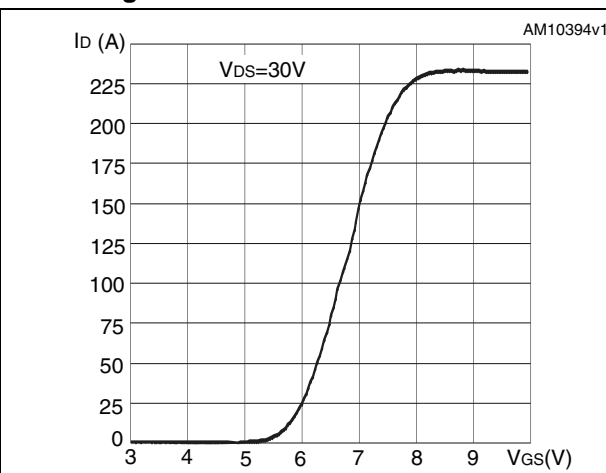


Figure 6. Gate charge vs gate-source voltage

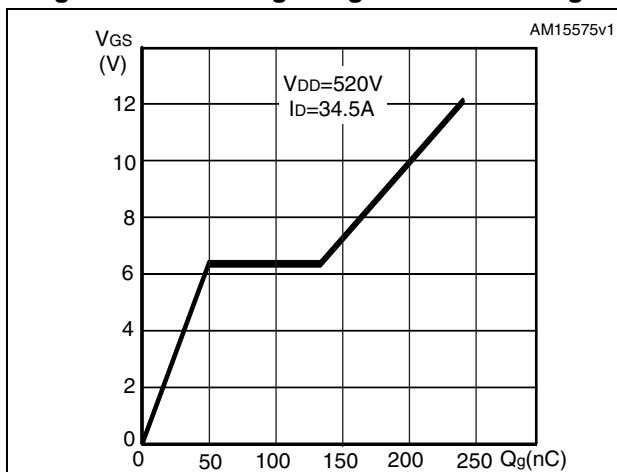


Figure 7. Static drain-source on-resistance

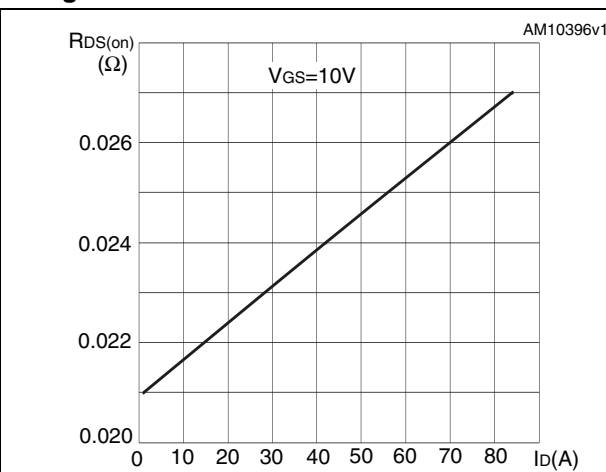


Figure 8. Capacitance variations

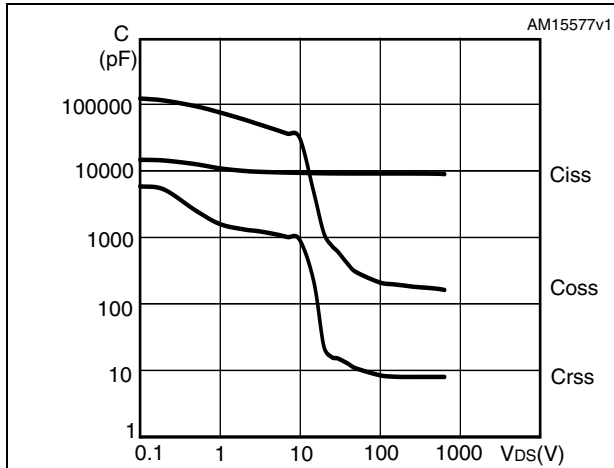


Figure 9. Output capacitance stored energy

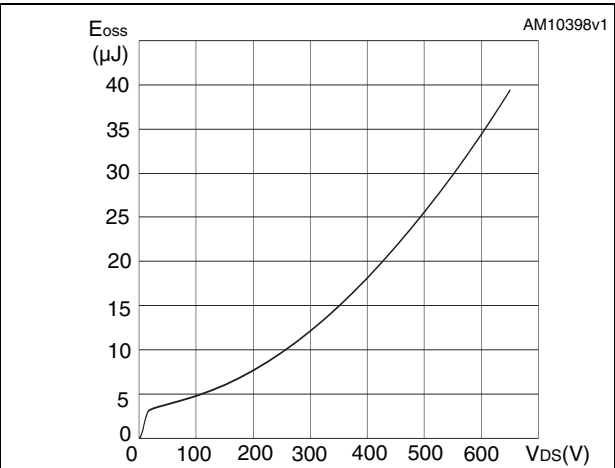


Figure 10. Normalized gate threshold voltage vs temperature

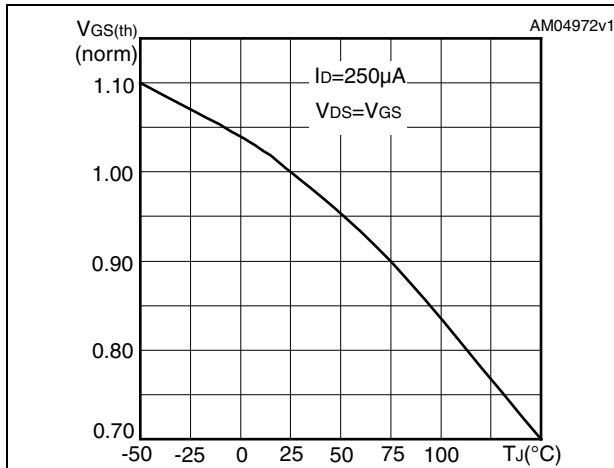


Figure 11. Normalized on-resistance vs temperature

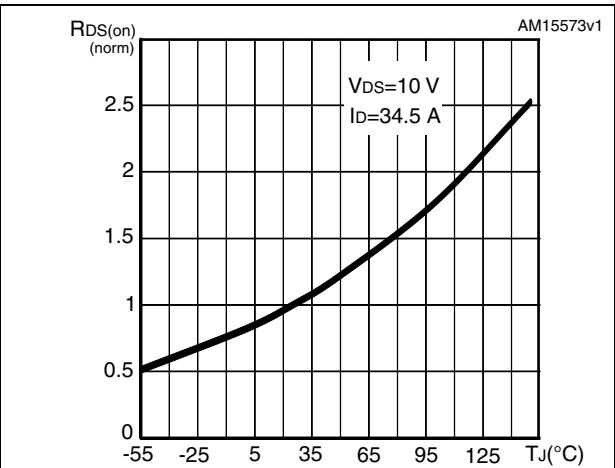


Figure 12. Source-drain diode forward characteristics

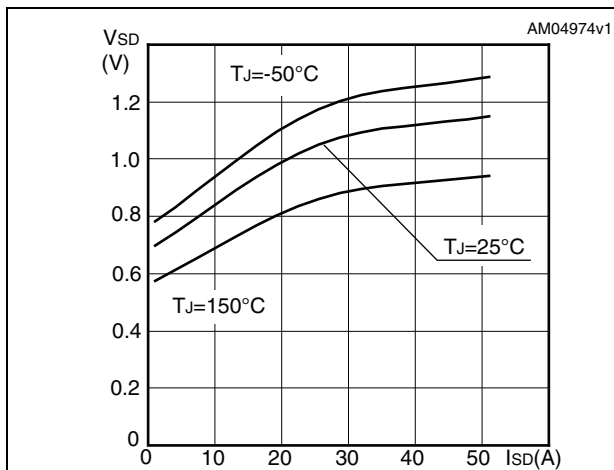


Figure 13. Normalized V_{DS} vs temperature

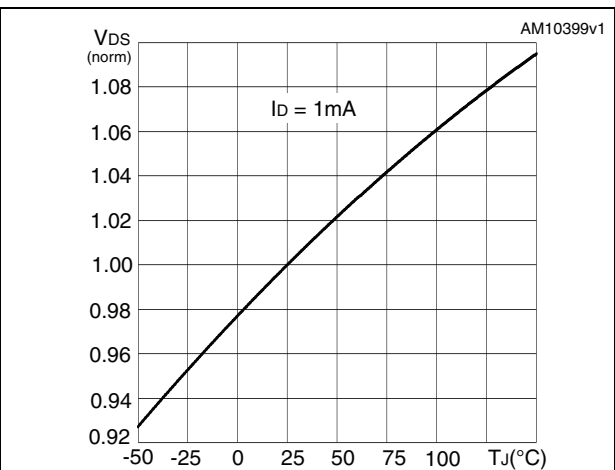
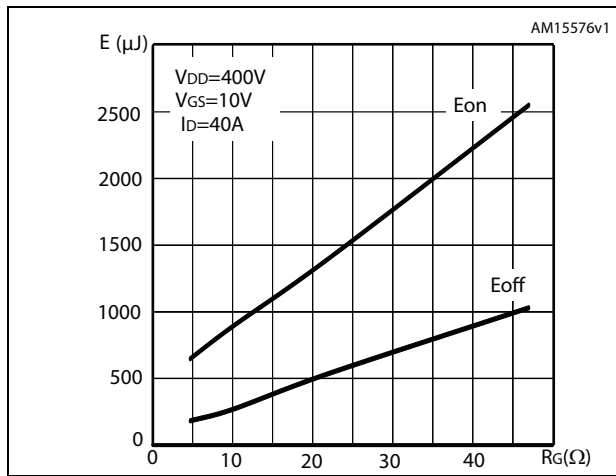


Figure 14. Switching losses vs gate resistance (1)



1. E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times



Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

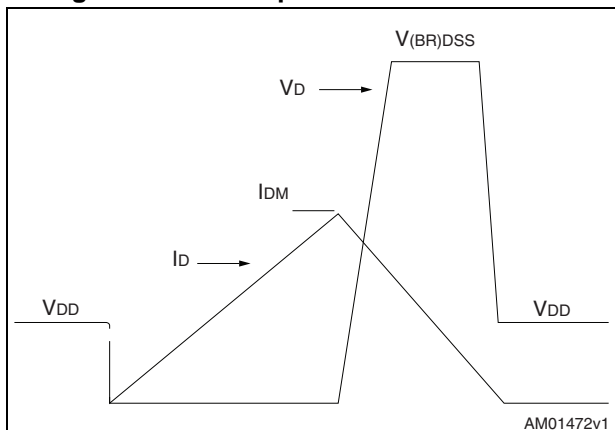
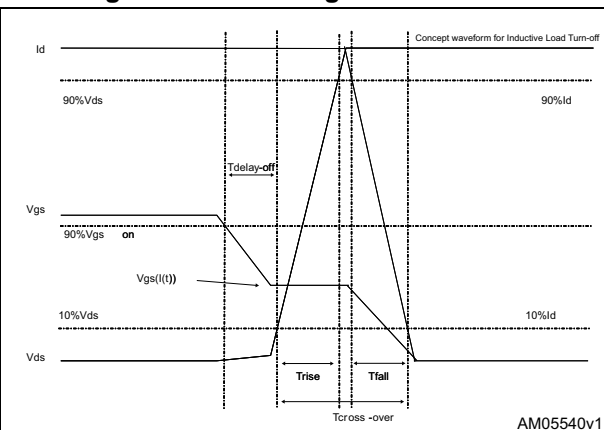


Figure 20. Switching time waveform



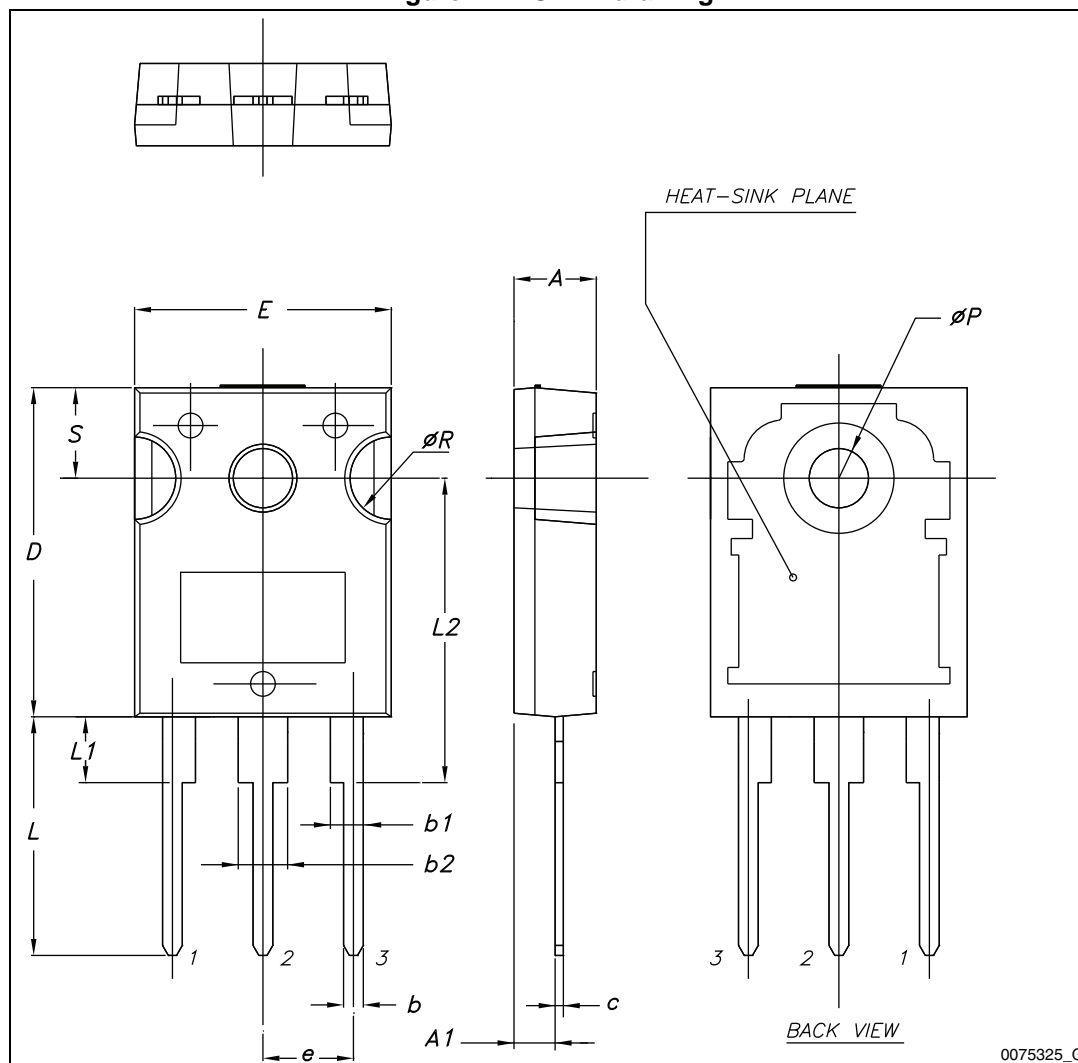
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing



0075325_G

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Jul-2012	1	First release.
22-Jan-2013	2	Modified: $R_{DS(on)}$ on first page, I_D , I_{DM} on Table 2 , note 2 on Table 2 , typical values on Table 6 , 7 , max and typical values on Table 8 , Figure 2 , 6 , 8 , 9 , 11 and 14
07-Aug-2013	3	<ul style="list-style-type: none">– Minor text changes– Modified: Applications in first page– Added: MOSFET dv/dt ruggedness parameter in Table 2– Added: Table 4: Avalanche characteristics– Modified: Figure 15, 16, 17 and 18
08-Aug-2013	4	<ul style="list-style-type: none">– Minor text changes– Modified: Figure 14

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