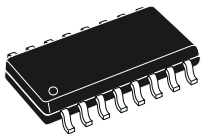
L6699

Enhanced high voltage resonant controller

Datasheet – production data

Features

- Symmetrical duty cycle, variable frequency control of resonant half bridge
- Self-adjusting adaptive deadtime
- High-accuracy oscillator
- 2-level OCP: frequency-shift and immediate shutdown
- Interface with PFC controller
- Anti-capacitive-mode protection
- Burst-mode operation at light load
- Input for brownout protection or power-on/off sequencing
- “Safe-start” procedure prevents hard switching at startup
- 600 V rail compatible high-side gate driver with integrated bootstrap diode and high dv/dt immunity
- -300/800 mA high-side and low-side gate drivers with UVLO pull-down
- SO16N package



SO16N

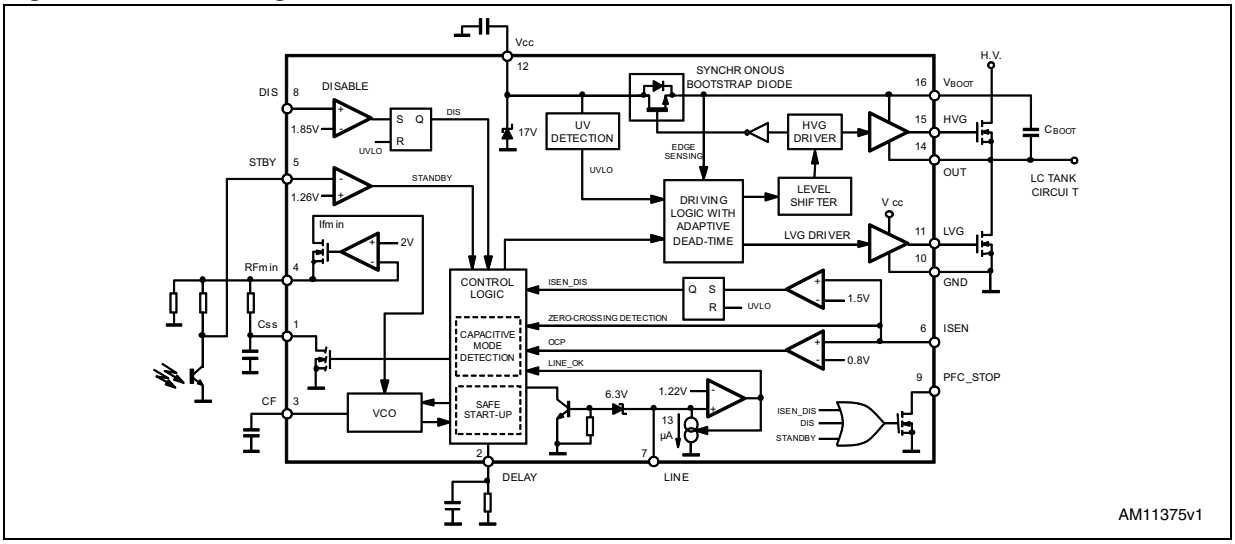
Applications

- SMPS for LCD TVs, desktop and AIO PCs, servers, Telecom power
- AC-DC adapter, open frame SMPS

Table 1. Device summary

Order codes	Package	Packing
L6699D	SO16N	Tube
L6699DTR		Tape and reel

Figure 1. Block diagram



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1 Description

The L6699 is a double-ended controller specific to series-resonant half bridge topology. Both LLC and LCC configurations are supported. It provides symmetrical complementary duty cycle: the high-side switch and the low-side switch are driven ON/OFF 180° out-of-phase for exactly the same time. Output voltage regulation is obtained by modulating the operating frequency. The deadtime inserted between the turn-off of one switch and the turn-on of the other one is automatically adjusted to best fit the transition times of the half bridge midpoint. To drive the high-side switch with the bootstrap approach, the IC incorporates a high voltage floating structure able to withstand more than 600 V with a synchronous-driven high voltage DMOS that replaces the external fast-recovery bootstrap diode.

The IC enables the user to set the operating frequency range of the converter by means of a high-accuracy externally programmable oscillator.

At startup, in addition to the traditional frequency-shift soft-start (the switching frequency starts from a preset maximum value and then decays as far as the steady-state value determined by the control loop), a proprietary circuit controls the half bridge to prevent hard-switching from occurring in the initial cycles because of the unbalance in the V·s applied to the transformer.

At light load the IC can be forced to enter a controlled burst-mode operation that keeps the converter input consumption as low as possible.

IC protection functions include a current sense input for OCP with frequency shift and delayed shutdown with automatic restart. Fast shutdown with automatic restart occurs if this first-level protection cannot control the primary current. Additionally, the IC prevents the converter from working in or too close to the capacitive mode, to guarantee soft-switching. A latched disable input (DIS) can be used to implement OTP and/or OVP. The combination of these protection features offers the highest degree of safety.

Other functions include a not-latched active-low disable input with current hysteresis, useful for power sequencing or for brownout protection, and an interface with the PFC controller that enables the switching-off of the pre-regulator during fault conditions or during burst-mode operation.

2 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{BOOT}	16	Floating supply voltage ($I_{leak} \leq 5\mu A$)	-1 to 618	V
HVG	15	HVG voltage	V_{OUT} -0.3 to V_{BOOT} +0.3	V
V_{OUT}	14	Floating ground voltage	-3 up to a value included in the range V_{BOOT} -18 and V_{BOOT}	V
dV_{OUT}/dt	14	Floating ground max. slew rate	50	V/ns
V_{CC}	12	IC supply voltage (Icc ≤ 25 mA)	Self-limited	V
LVG	11	LVG voltage	-0.3 to V_{CC} +0.3	V
V_{PFC_STOP}	9	Maximum voltage (pin open)	-0.3 to V_{CC}	V
I_{PFC_STOP}	9	Maximum sink current (pin low)	Self-limited	A
$V_{LINEmax}$	7	Maximum pin voltage (Ipin ≤ 1 mA)	Self-limited	V
I_{RFmin}	4	Maximum source current	2	mA
V_{ISEN}	6	Current sense voltage	-3 to 5	V
---	1 to 5, 8	Analog inputs & outputs voltage	-0.3 to 5	V
T_j	---	Junction temperature operating range	-40 to 150	°C
T_{stg}	---	Storage temperature	-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction-to-ambient (SO16N)	120	°C/W
P_{tot}	Power dissipation @tamb = 50 °C (SO16N)	0.83	W

4 Pin connections

Figure 2. Pin connections (top view)

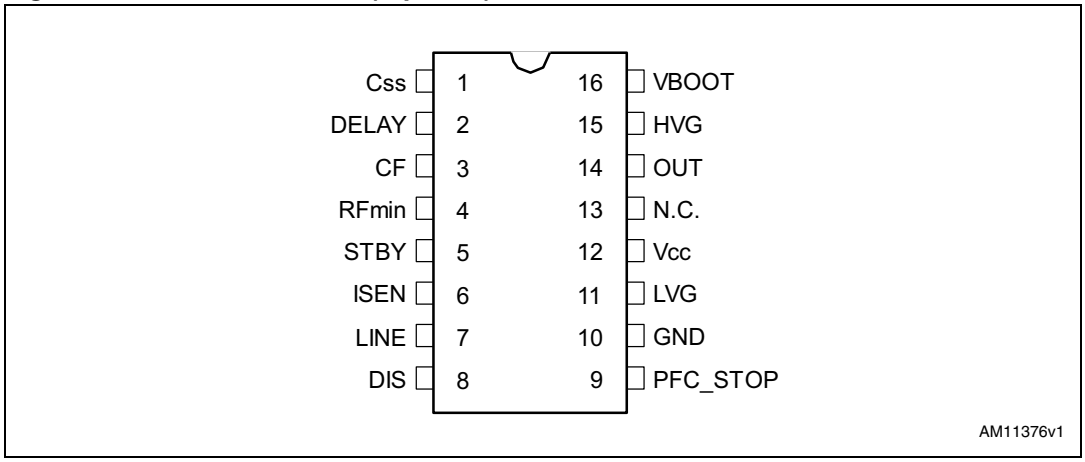


Table 4. Pin functions

N.	Name	Function
1	C_{SS}	Soft-start. This pin connects an external capacitor to GND and a resistor to RF_{min} (pin 4) that set both the initial oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (V_{CC} < UVLO, LINE < 1.25 V, DIS > 1.85 V, ISEN > 1.5 V, DELAY > 2 V) to make sure it is soft-started next. Additionally the switch is activated when the voltage on the current sense pin (ISEN) exceeds 0.8 V or when the converter is working too close to, or in, the capacitive-mode operation.
2	DELAY	Delayed shutdown upon overcurrent. A capacitor and a resistor are connected from this pin to GND to set both the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching. Every time the voltage on the ISEN pin exceeds 0.8 V the capacitor is charged by 350 µA current pulses and is slowly discharged by the external resistor. If the voltage on the DELAY pin reaches 2 V, the soft-start capacitor is completely discharged so that the switching frequency is pushed to its maximum value and the 350 µA current source is kept always on. As the voltage on the DELAY pin exceeds 3.5 V the IC stops switching and the internal generator is turned off, so that the voltage on the pin decays because of the external resistor. The IC is soft-restarted as the voltage drops below 0.3 V. In this way, under short-circuit conditions, the converter works intermittently with very low input average power. If the voltage on the ISEN pin exceeds 1.5 V, the L6699 is immediately stopped and the 350 µA current source is kept on until the voltage on the DELAY pin reaches 3.5 V. Then, the generator is turned off and the voltage on the pin decays because of the external resistor. Also in this case the IC is soft-restarted as the voltage drops below 0.3 V.
3	CF	Timing capacitor. A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RF_{min}) and determines the switching frequency of the converter.

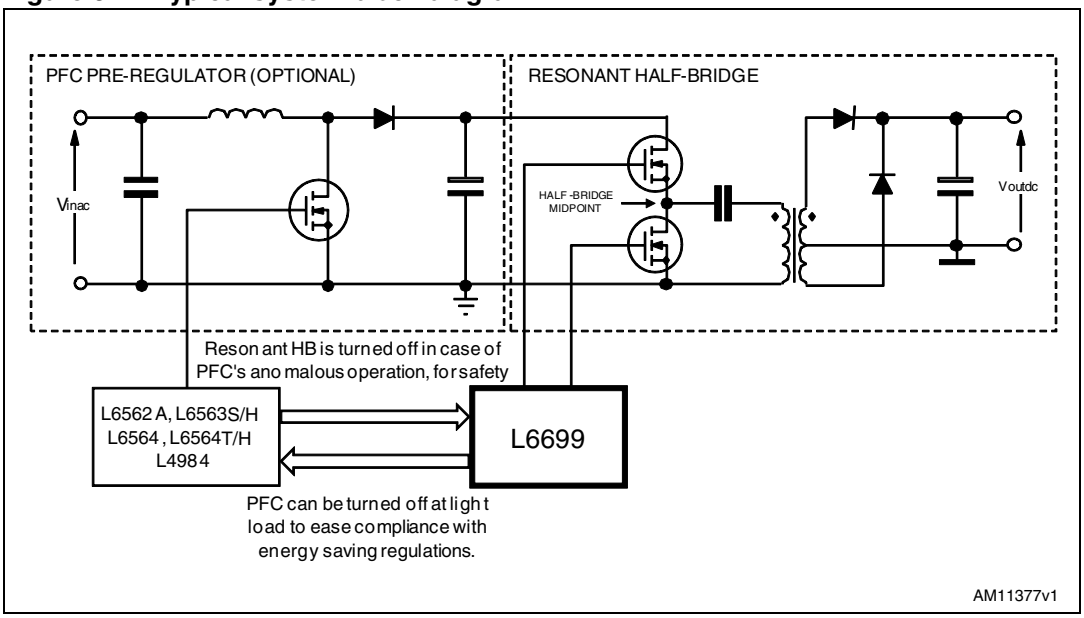
Table 4. Pin functions (continued)

N.	Name	Function
4	RF_{min}	Minimum oscillator frequency setting. This pin provides an accurate 2 V reference, and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency. To close the feedback loop that regulates the converter output voltage by modulating the oscillator frequency, the phototransistor of an optocoupler is connected to this pin through a resistor. The value of this resistor sets the maximum operating frequency. Initial operating frequency should be set below 300 kHz; it is recommended not to exceed such limit. An R-C series connected from this pin to GND sets frequency shift at startup to prevent excessive energy inrush (soft-start).
5	STBY	Burst-mode operation threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.26 V). If the voltage on the pin is lower than the reference, the IC enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 30 mV. Soft-start is not invoked. This function realizes burst-mode operation when the load falls below a level that can be programmed by properly choosing the resistor connecting the optocoupler to the RF_{min} pin (see *Figure 1: Block diagram*). Tie the pin to RF_{min} if burst-mode is not used.
6	ISEN	Current sense input. The pin senses the instantaneous primary current though a sense resistor or a capacitive divider for lossless sensing. If the voltage exceeds a 0.8 V threshold the soft-start capacitor connected to pin 1 is internally discharged: the frequency increases and so limits the power throughput. Under output short-circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time set at pin 2. If the current keeps on building up despite this frequency increase, a second comparator referenced to 1.5 V disables switching immediately and activates a restart delay procedure (see DELAY pin description for more information). This pin is used also for capacitive-mode operation detection and for hard-switching prevention at startup. Do not short the pin to ground; this would prevent the device from operating correctly.
7	LINE	Line sensing input. The pin is to be connected to the high voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.25 V shuts down the IC, lowers its consumption and discharges the soft-start capacitor. IC operation is enabled as the voltage exceeds 1.25 V. The comparator is provided with current hysteresis: an internal 13 µA current generator is ON as long as the voltage applied at the pin is below 1.25 V, and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. The voltage on the pin is top-limited by an internal Zener. Tie the pin to V_{CC} with a =100 kΩ resistor if not used.
8	DIS	Latched device shutdown. Internally, the pin connects a comparator that, when the voltage on the pin exceeds 1.85 V, shuts the IC down and brings its consumption almost to a “before startup” level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the V_{CC} pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.
9	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin, normally open, is intended for stopping the PFC controller, for protection purposes or during burst-mode operation. It goes low when the IC is shut down by DIS > 1.85 V, ISEN > 1.5 V and STBY < 1.25 V. The pin is pulled low also when capacitive mode operation is detected and when the voltage on the DELAY pin exceeds 2 V. In this latter case it goes back open as the voltage falls below 0.3 V. During UVLO, it is open. Leave the pin unconnected if not used.

Table 4. Pin functions (continued)

N.	Name	Function
10	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
11	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the lower MOSFET of the half bridge leg. The pin is actively pulled to GND during UVLO.
12	V_{CC}	Supply voltage of both the signal part of the IC and the low-side gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND may be useful to obtain a clean bias voltage for the signal part of the IC.
13	N.C.	High voltage spacer. The pin is not internally connected to isolate the high voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	OUT	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Lay out the connection of this pin carefully to avoid too large spikes below ground.
15	HVG	High-side floating gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the upper MOSFET of the half bridge leg. A resistor internally connected to pin 14 (OUT) ensures that the pin is not floating during UVLO.
16	V_{BOOT}	High-side gate-drive floating supply voltage. The bootstrap capacitor connected between this pin and pin 14 (OUT) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure replaces the normally used external diode.

Figure 3. Typical system block diagram



5 Electrical data

Tj = -25 to +125 °C, V_{CC} = 15 V, V_{BOOT} = 15 V, C_{HVG} = C_{LVG} = 1 nF; C_F = 470 pF; RF_{min} = 12 KΩ; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Ic supply voltage						
V_{CC}	Operating range	After device turn-on	8.85		16	V
V_{CCOn}	Turn-on threshold	Voltage rising	10	10.7	11.4	V
V_{CCOff}	Turn-off threshold	Voltage falling	7.45	8.15	8.85	V
Hys	Hysteresis			2.55		V
V_Z	V_{CC} clamp voltage	Iclamp = 15 mA	16	17	17.9	V
Supply current						
$I_{start-up}$	Startup current	Before device turn-on V_{CC} = V_{CCOn} - 0.2 V		250	300	µA
I_q	Quiescent current	Device on, V_{STBY} = 1 V		1	1.3	mA
I_{op}	Operating current	Device on, V_{STBY} = V_{RFmin}		3	4.1	mA
I_q	Residual consumption	V_{DIS}>1.92 V or V_{DELAY}>3.65 V or V_{LINE}<1.2 V		400	500	µA
High-side floating gate-drive supply						
$R_{DS(on)}$	Synchronous bootstrap diode ON-resistance	V_{LVG} = high		150		
Overcurrent comparator						
I_{ISEN}	Input bias current	V_{ISEN} = 0 to $V_{ISENdis}$			-1	µA
V_{ISENx}	Frequency shift threshold	Voltage rising (1)	0.76	0.80	0.84	V
$V_{ISENdis}$	Immediate stop threshold	Voltage rising (1)	1.43	1.5	1.55	V
Line sensing						
V_{LINE}	Threshold voltage	Voltage rising or falling (1)	1.18	1.22	1.26	V
I_{Hys}	Current hysteresis	V_{LINE} = 1.2 V	10	13	16	µA
V_{clamp}	Clamp level	I_{LINE} = 1 mA	6			V
Latched disable function						
I_{DIS}	Input bias current	V_{DIS} = 0 to 1.92 V			-1	µA
V_{DIS}	Disable threshold	Voltage rising (1)	1.78	1.85	1.92	V
Oscillator						
f_{osc}	Oscillation frequency		58.2	60	61.8	kHz
		R_{RFmin} = 2.7 kΩ	225	235	245	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_D (2)	Deadtime self-adjustment range	Minimum value		0.23		µs
		Maximum value		0.7		
V_{CFp}	Peak value			3.9		V
V_{CFv}	Valley value			0.9		V
V_{REF}	Voltage reference on pin 4	(1)	1.93	2	2.07	V
		I_{REF} = -2 mA (1)	1.8	2	2.07	
K_M	Current mirroring ratio			1		A/A
RF_{min}	Timing resistor range		1		100	kΩ
Zero-current comparator						
$V_{ZCD\ neg}$	Threshold voltage (-)			-10		mV
$V_{ZCD\ pos}$	Threshold voltage (+)			+10		mV
Pfc_stop function						
I_{leak}	High level leakage current	V_{PFC_STOP} = V_{CC}, V_{DIS} = 0 V			1	µA
R_{PFC_STOP}	ON-state resistance	I_{PFC_STOP} = 1 mA, V_{DIS} > 1.92 V		130	200	Ω
Soft-start function						
I_{leak}	Open-state current	V(C_{SS}) = 2 V			0.5	µA
R	Discharge resistance			120		Ω
T_{DISCH}	C_{SS} discharge duration	V_{ISEN} > V_{ISENx} or approaching capacitive-mode		5		µs
		Capacitive-mode detected		50		
Standby function						
I_{STBY}	Input bias current	V_{STBY} = 0 to 1.3 V			-1	µA
V_{STBY}	Disable threshold	Voltage falling (1)	1.22	1.26	1.3	V
Hys	Hysteresis	Voltage rising		30		mV
Delayed shutdown function						
I_{leak}	Open-state current	V_{DELAY} = 1 V		1		µA
		V_{DELAY} = 1 V, after shutdown		-0.1	-0.5	
I_{CHARGE}	Charge current	V_{DELAY} = 2.5 V, V_{ISEN} = 0.85 V	250	350	450	µA
Vth_1	Threshold for forced operation at max. frequency	Voltage rising (1)	1.92	2.0	2.08	V
Vth_2	Shutdown threshold	Voltage rising (1)	3.35	3.5	3.65	V
Vth_3	Restart threshold	Voltage falling (1)	0.27	0.3	0.33	V
Low-side gate driver (voltages referred to GND)						
V_{LVGL}	Output low voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output high voltage	I_{source} = 5 mA	12.8	13.3		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall time			30		ns
t_r	Rise time			60		ns
	UVLO saturation	V_{CC} = 0 to V_{CCOn}, I_{sink} = 2 mA			1.1	V
High-side gate driver (voltages referred to out)						
V_{LVGL}	Output low voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output high voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall time			30		ns
t_r	Rise time			60		ns
	HVG-OUT pull-down			22		kΩ

1. Values tracking each other.
2. Refer to adaptive deadtime section, *Figure 9*.

6 Application information

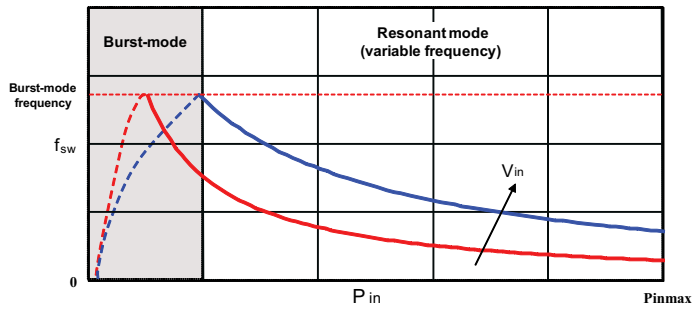
The L6699 is an advanced double-ended controller specific to resonant half bridge topology. In these converters the MOSFETs of the half bridge leg are alternately switched on and off (180° out-of-phase) for exactly the same time. This is commonly referred to as symmetrical operation at “50% duty cycle”, although the real duty cycle, i.e. the ratio of the ON-time of either switch to the switching period, is actually less than 50%. The reason is that there is a deadtime T_D inserted between the turn-off of either MOSFET and the turn-on of the other one, where both MOSFETs are off. This deadtime is essential in order for the converter to work correctly: it enables soft-switching and, then, high-frequency operation with high efficiency and low EMI emissions.

A special feature of this IC is that it is able to automatically adjust T_D within a range so that it best fits the transition times of the half bridge midpoint (adaptive deadtime). This allows the user to optimize the design of the resonant tank so that soft-switching can be achieved with a lower level of reactive energy (i.e. magnetizing current), therefore optimizing efficiency under a broader load range, from full to light load.

To perform converter output voltage regulation the device is able to operate in different modes (*Figure 1*), depending on the load conditions:

1. Variable frequency at heavy and medium/light load. A relaxation oscillator (see *Section 6.1: Oscillator* for more details) generates a symmetrical triangular waveform, which MOSFET switching is locked to. The frequency of this waveform is related to a current that is modulated by the feedback circuitry. As a result, the tank circuit driven by the half bridge is stimulated at a frequency dictated by the feedback loop to keep the output voltage regulated, therefore exploiting its frequency-dependent transfer characteristics.
2. Burst-mode control with no or very light load. When the load falls below a value, the converter enters a controlled intermittent operation, where a series of a few switching cycles at a nearly fixed frequency are spaced out by long idle periods where both MOSFETs are in the OFF-state. A further load decrease is translated into longer idle periods and then in a reduction of the average switching frequency. When the converter is completely unloaded, the average switching frequency can go down even to few hundred hertz, therefore minimizing magnetizing current losses as well as all frequency-related losses and making it easier to comply with energy saving specifications.

Figure 4. Multimode operation of the L6699



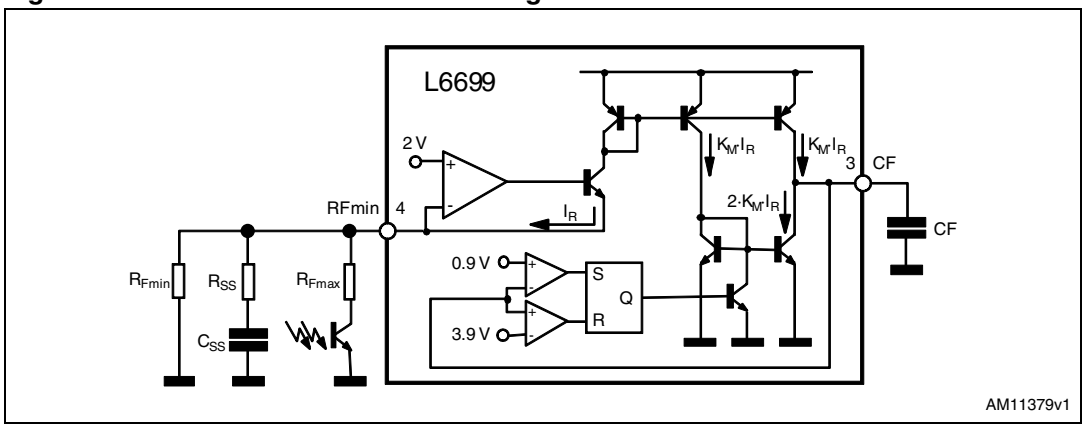
6.1 Oscillator

The oscillator is programmed externally by means of a capacitor (CF), connected from pin 3 (CF) to ground, that is alternately charged and discharged by the current defined with the network connected to pin 4 (RF_{min}). The pin provides an accurate 2 V reference with about 2 mA source capability; the higher the current sourced by the pin, the higher the oscillator frequency. The block diagram of *Figure 5* shows a simplified internal circuit that explains the operation.

The network that loads the RF_{min} pin generally comprises three branches:

1. a resistor RF_{min} connected between the pin and ground that determines the minimum operating frequency.
2. a resistor RFmax connected between the pin and the collector of the (emitter-grounded) phototransistor that transfers the feedback signal from the secondary side back to the primary side; while in operation, the phototransistor modulates the current through this branch - therefore modulating the oscillator frequency - to perform output voltage regulation; the value of RFmax determines the maximum frequency the half bridge is operated at when the phototransistor is fully saturated.
3. an R-C series circuit (C_{SS}+ R_{SS}) connected between the pin and ground that enables the setting up of a frequency shift at startup (see *Section 6.3: Safe-start procedure*). Note that the contribution of this branch is zero during steady-state operation.

Figure 5. Oscillator's internal block diagram



The following approximate relationships hold for the minimum and the maximum oscillator frequency respectively:

Equation 1

$$f_{min} = \frac{1}{3 \cdot CF \cdot RF_{min}} \quad ; \quad f_{max} = \frac{1}{3 \cdot CF \cdot \left(RF_{min} \,//\, RF_{max} \right)}$$

After fixing CF according to *Table 6*:

Table 6. Recommended values for CF as a function of the startup frequency f_{start}

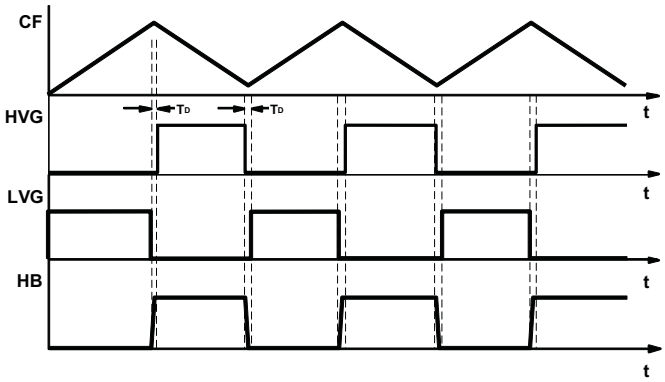
f_{start} [kHz]	CF [pF]	f_{start} [kHz]	CF [pF]
150	680	230 - 240	180
160	560	250	150
170	470	260	120
180	390	270	100
190 – 200	330	280	82
210	270	290	68
220	220	300	56

Value of RF_{min} and RF_{max} is selected so that the oscillator frequency is able to cover the entire range needed for regulation, from the minimum value f_{min} (at minimum input voltage and maximum load) to the maximum value f_{max} (at maximum input voltage and minimum load):

Equation 2

$$RF_{min} = \frac{1}{3 \cdot CF \cdot f_{min}} \quad ; \quad RF_{max} = \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

Figure 6. Oscillator waveforms and their relationship with gate-driving signals



A different selection criterion is given for RF_{max} if burst-mode operation is to be used (see *Section 7: Operation at no load or very light load*).

In *Figure 6* the timing relationship between the oscillator waveform and the gate-drive signal, as well as the midpoint of the half bridge leg (HB) is shown. Note that the low-side gate-drive is turned on while the oscillator's triangle is ramping up and the high-side gate-drive is turned on while the triangle is ramping down. In this way, at startup, or as the IC resumes switching during burst-mode operation, the low-side MOSFET is switched on first to charge the bootstrap capacitor. As a result, the bootstrap capacitor is always charged and ready to supply the high-side floating driver (see *Section 12: Bootstrap section*).

6.2 Adaptive deadtime

A deadtime T_D inserted between the turn-off of either switch and the turn-on of the complementary one, where both switches are in the OFF-state, is essential to achieve soft-switching. Its value must be larger than the time T_T needed for the rail-to-rail swing of the half bridge midpoint. This duration T_T depends on the total parasitic capacitance of the half bridge midpoint, which must be completely charged or depleted and the value of the resonant tank current during the transition.

With good approximation, the tank current during the transition time T_T can be considered constant and equal to the “switched current” I_S, i.e. the value of the tank current as the transition begins. If C_{HB} denotes the total parasitic capacitance of the half bridge midpoint (it includes the Coss of the MOSFETs, the transformer's primary winding parasitic capacitance, plus other stray contributors), the condition for soft-switching is:

Equation 3

$$T_T = \frac{C_{HB}}{I_S} Vin \leq T_D$$

which should be met under all operating conditions. This formula suggests that T_D should be large enough to always exceed T_T, especially with maximum Vin and at no load, where I_S is at a minimum and T_T at a maximum. However, a too long deadtime may lead to the loss of soft-switching too: in fact, the tank current must not change its sign within the deadtime, which could lead to the turn-on of either MOSFET with a non-zero drain-to-source voltage or, even worse, with the body diode of the other MOSFET conducting (capacitive mode operation - see *Section 9: Capacitive-mode detection function* for more details). This may occur at maximum load and minimum Vin, especially when the tank circuit is designed for a low magnetizing current to optimize light load efficiency. Additionally, a too long deadtime may increase conduction losses in the body diodes and significantly limit the operating frequency of the half bridge.

A good approach is to automatically adjust T_D so that it tracks T_T, keeping $T_T \leq T_D$ under all operating conditions. This is the objective of the adaptive deadtime function in the L6699.

Figure 7 and *Figure 8* show the principle schematic and its key waveforms. An edge detector (the |d/dt| block) senses that the half bridge midpoint (connected to the OUT pin) is swinging from B+ to GND or vice versa through the V_{BOOT} pin, which moves exactly following the OUT pin (due to Cboot there is a DC voltage difference between them). The output of the |d/dt| block is high as long as the OUT pin is swinging and, as the transition is completed, the output goes low. A monostable circuit, sensitive to negative-going edges, releases a pulse that marks the end of the deadtime.

Figure 7. Adaptive deadtime: principle schematic

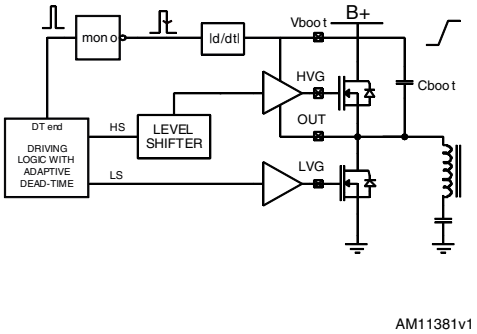
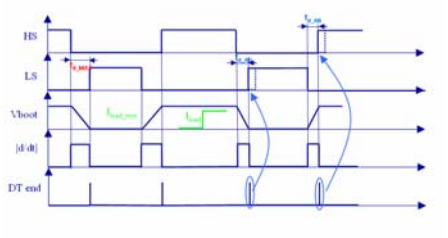
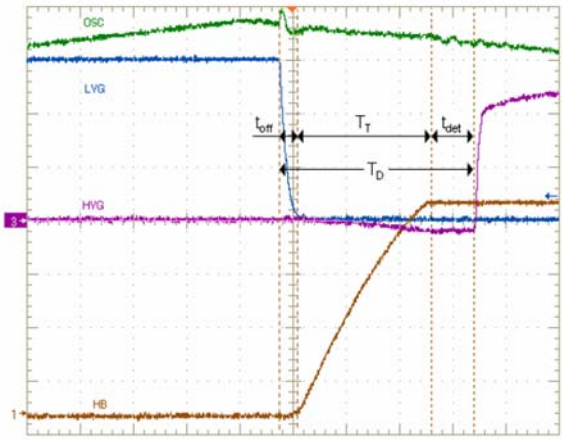


Figure 8. Relevant timing diagrams



Note that the “Driving logic…” block sets a minimum deadtime T_{D_MIN} (≈ 230 ns) below which T_D cannot go, to prevent simultaneous conduction of the high-side and the low-side switch, and also a maximum deadtime T_{D_MAX} to guarantee proper operation of the half bridge. T_{D_MAX} is internally set at either 700 ns or one fourth of the oscillator cycle, whichever is shorter.

Figure 9. Detailed view of deadtime during low-to-high transition of half bridge midpoint



The actual deadtime T_D that can be observed during operation does not depend only on the adjustment circuit of *Figure 7*. This fact can be explained with the aid of the oscilloscope image shown in *Figure 9*.

It illustrates a detailed view of the low-to-high transition of the half bridge midpoint (waveform labeled HB) along with the high-side gate-drive (HVG), the low-side gate-drive (LVG) and the oscillator voltage on pin CF (OSC). Obviously, the information that follows applies to the high-to-low transition as well.

There are three contributors to T_D:

- The turn-off delay t_{OFF} of the Power MOSFET, which depends on the input characteristics of the specific MOSFET and the speed its gate is driven
- The transition time T_T the half bridge midpoint takes for a rail-to-rail swing
- The detection time t_{det} that elapses from the end of the half bridge midpoint swing to the gate-drive signal of the other MOSFET going high; this includes the detection time as well as the propagation delay along the downstream logic circuitry up to the driver output.

It is important to point out that the value of T_{D_MIN} specified in the electrical characteristics is essentially tdet: therefore the minimum observable T_D is always longer. T_{D_MAX}, on the other hand, is counted starting from the negative-going edge of the gate-drive signal, so it actually fixes a maximum limit for T_D: $T_D \leq T_{D\_MAX}$.

Finally, it is worth stating that the adaptive deadtime function does not significantly increase efficiency by itself. It is a degree of freedom that must be exploited for this purpose when designing the resonant tank. Essentially, it allows the use of a higher magnetizing inductance in the transformer, which minimizes the magnetizing current and, then, the conduction losses associated to it. Additionally, this may reduce the switched current I_S to the minimum required to achieve soft-switching, therefore reducing turn-off switching losses in MOSFETs. Efficiency at medium and light load greatly benefits from this optimization.

6.3 Safe-start procedure

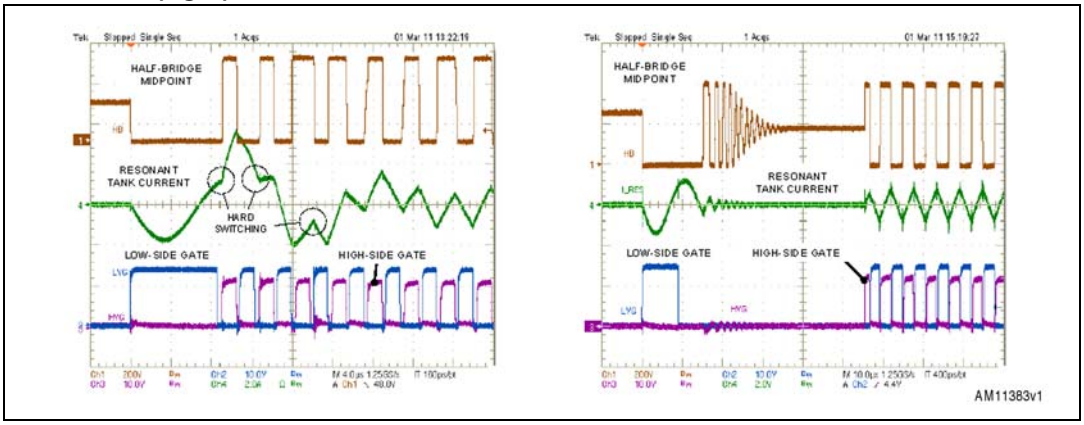
In the L6699 a new startup procedure, termed “safe-start”, has been implemented to prevent loss of soft-switching during the initial switching cycles, which is not 100% guaranteed by the usual soft-start procedure.

Sweeping the operating frequency from an initial high value, that should not exceed 300 kHz, down to the point where the control loop takes over, which is commonly referred to as soft-start, has a twofold benefit. On the one hand, since the deliverable power depends inversely on frequency, it progressively increases the converter's power capability, therefore avoiding excessive inrush current. On the other hand, it makes the converter initially work at frequencies higher than the upper resonance frequency of the LLC tank circuit, which ensures inductive-mode operation (i.e. with the tank current lagging the square wave voltage generated by the half bridge) and, therefore, soft-switching.

However, the last statement is true under a quasi-static approximation, i.e. when the operating point of the resonant tank is slowly varying around a steady-state condition. This approximation is not correct during the very first switching cycles of the half bridge, where the initial conditions of the tank circuit can be away from those under steady-state. Therefore, hard-switching is possible during the transient period needed to reach the slowly varying steady-state condition dictated by the soft-start action. A non-zero initial voltage on the resonant capacitor Cr and transformer flux imbalance during the previously mentioned transient period are the possible causes of hard-switching in the initial cycles.

In high voltage half bridge controllers it is customary to start the switching activity by turning on the low-side MOSFET for a preset time to pre-charge the bootstrap capacitor (see *Section 12: Bootstrap section*) and ensure proper driving of the high-side MOSFET from the first cycle. In traditional controllers, normal switching starts right at the end of the pre-charge time, as shown in the left-hand image in *Figure 10*.

Figure 10. Comparison startup behavior: traditional controller (left), with L6699 (right)



A non-zero initial voltage on the resonant capacitor may cause the very first turn-on of the high-side MOSFET to occur with non-zero drain-to-source voltage while the body diode of the low-side MOSFET is conducting, therefore invoking its reverse recovery. More hard-switching cycles may follow (see the left-hand image in *Figure 10*). These events are few but potentially hazardous: they could cause the destruction of both MOSFETs, should the resulting dv/dt across the low-side MOSFET exceed its maximum rating (see *Section 9: Capacitive-mode detection function* for more details).

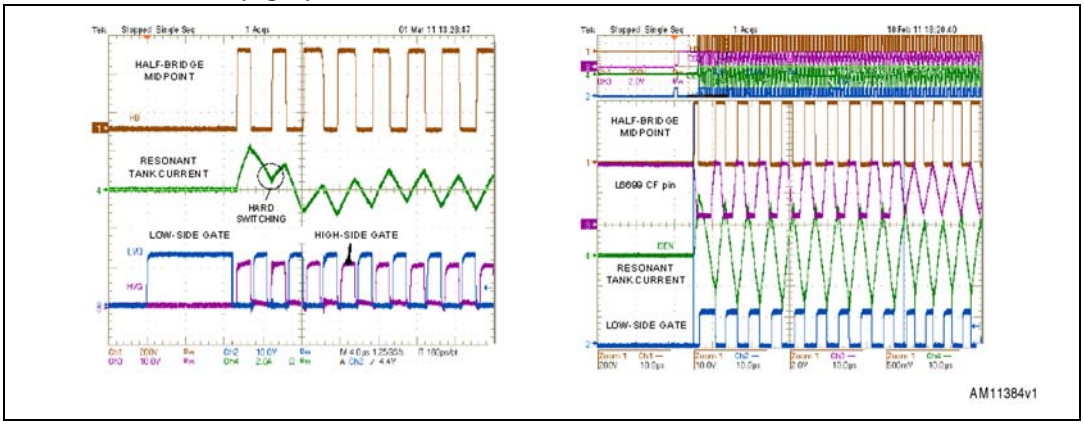
To prevent this hard-switching cycle(s) with body diode reverse recovery, the L6699 waits about 50 µs after the pre-charge time before starting switching (see the right-hand image in *Figure 10*). This idle time is normally long enough to let the tank current decay to essentially zero in case of an initially charged resonant capacitor. On the other hand, it is too short for the bootstrap capacitor to be significantly discharged.

To understand the origin of transformer flux imbalance it is worth remembering that the half bridge is driven with 50% duty cycle, so that under steady-state conditions the voltage across the resonant capacitor Cr has a DC component equal to Vin/2. Consequently, the transformer's primary winding is symmetrically driven by a ± Vin/2 square wave.

At startup, however, the voltage across Cr is often quite different from Vin/2, so it takes some time for its DC component to reach the steady-state value Vin/2. During this transient, the transformer is not driven symmetrically and, then, there is a significant V·s imbalance in two consecutive half-cycles. If this imbalance is large, there is a significant difference in the up and down slopes of the tank current and, the duration of the two half-cycles being the same, the current may not reverse in a switching half-cycle, as shown in the left-hand image in *Figure 11*. Once again, one MOSFET can be turned on while the body diode of the other is conducting and this may happen for a few cycles.

To prevent this, the L6699 is provided with a proprietary circuit that modifies the normal operation of the oscillator during the initial switching cycles, so that the initial V·s unbalance is nearly eliminated. Its operation is such that current reversal in every switching half-cycle and, then, soft-switching is ensured.

Figure 11. Comparison of initial cycles after startup: traditional controller (left), with L6699 (right)



It goes without saying that when either MOSFET is turned on for the very first time, this occurs with a non-zero drain-to-source voltage. Therefore, strictly speaking, hard-switching is still there. However, this type of one-shot hard-switching, where the body diode of the other MOSFET is not reverse recovered, is of little concern. In fact, the related capacitive power loss is thermally insignificant and, with a proper gate-drive circuit, spurious turn-on of the other MOSFET through Cgd injection is easily prevented.

The timing diagrams of *Figure 11* compare the startup behavior of a resonant converter driven by a traditional resonant controller with that of a converter driven by the L6699. During the initial phase, the ramps of the oscillator are synchronized to the zero-crossings of the tank current, so that a trapezoidal waveform appears across CF. As a result, the duty cycle of the half bridge is initially considerably less than 50% and the tank current changes its sign every half-cycle. The device goes to normal operation after approximately 50 µs from the first switching cycle. If the timing capacitor CF is selected according to *Table 6*, this transition is nearly seamless and just a small perturbation of the tank current can be observed.

Using capacitor values significantly different from those provided in *Table 6* might cause large perturbations during the transition. This might bring the half bridge close to losing soft-switching with a consequent activation of the capacitive-mode detection function.

With the L6699 the soft-start function is easily realized with the addition of an R-C series circuit from pin 4 (RF_{min}) to ground (see *Figure 13*).

Initially, the capacitor C_{SS} is totally discharged, so that the series resistor R_{SS} is effectively parallel with RF_{min} and the resulting initial frequency is determined by R_{SS} and RF_{min} only, as the optocoupler's phototransistor is cut off (as long as the output voltage is not too far away from the regulated value):

Equation 4

$$f_{start} = \frac{1}{3 \cdot CF \cdot \left(RF_{min} // R_{SS} \right)}$$

The C_{SS} capacitor is progressively charged until its voltage reaches the reference voltage (2 V) and, consequently, the current through R_{SS} goes to zero. This conventionally takes 5 times the constants $R_{SS} \cdot C_{SS}$, however, the soft-start phase really ends when the output voltage has got close to the regulated value and the feedback loop has taken over, so that

the operating frequency is essentially determined by the current sunk by the optocoupler's phototransistor.

During this frequency sweep phase the operating frequency decays following the exponential charge of C_{SS}: then, it initially changes relatively quickly but the rate of change gets slower and slower. This counteracts the non-linear frequency dependence of the tank circuit that makes the converter's input impedance change little as frequency is away from resonance and change very quickly as frequency approaches resonance frequency (see *Figure 13*).

Figure 12. Soft-start circuit

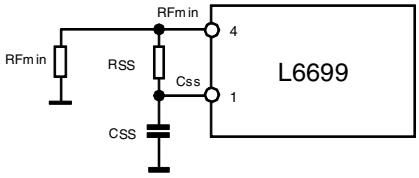
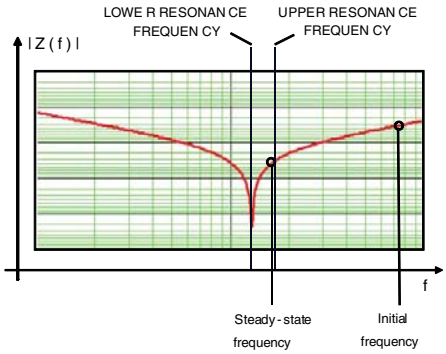


Figure 13. Input impedance vs. frequency curve in an LLC resonant half bridge



As a result, the DC input current smoothly increases, without the peaking that occurs with linear frequency sweep, and the output voltage reaches the regulated value with almost no overshoot.

Typically, R_{SS} and C_{SS} is selected based on the following relationships:

Equation 5

$$R_{SS} = \frac{RF_{min}}{\frac{f_{start}}{f_{min}} - 1} \quad ; \quad C_{SS} = \frac{3 \cdot 10^{-3}}{R_{SS}}$$

where f_{start} is recommended to not be over 300 kHz. Please refer to the timing diagram of *Figure 20* to see some significant signals during the soft-start phase.

7 Operation at no load or very light load

When the resonant half bridge is lightly loaded or totally unloaded, its switching frequency reaches its maximum value. To keep the output voltage under control and avoid losing soft-switching in these conditions, there must be some current flowing through the transformer's magnetizing inductance. This current can be kept relatively low because of the adaptive deadtime function; however, it produces power losses that prevent the converter's no load consumption from achieving very low values anyhow.

To overcome this issue, the L6699 enables the user to make the converter operate intermittently (burst-mode operation), with a series of a few switching cycles spaced out by long idle periods where both MOSFETs are in the OFF-state, so that the average switching frequency can be substantially reduced. As a result, the average value of the residual magnetizing current and the associated losses is considerably cut down, therefore facilitating the converter to comply with energy saving specifications.

The L6699 can be operated in burst-mode by using pin 5 (STBY): if the voltage applied to this pin falls below 1.26 V, the IC enters an idle state where both gate-drive outputs are low, the oscillator is stopped, the soft-start capacitor C_{SS} keeps its charge and only the 2V reference at the RF_{min} pin stays alive to minimize IC consumption and V_{CC} capacitor discharge. The IC resumes normal operation as the voltage on the pin exceeds 1.26 V by 30 mV.

In the L6699, the half bridge stops and restarts during burst-mode are more accurately controlled with respect to its predecessors: the last cycle before stopping and the first cycle after restarting are such that the DC voltage across the resonant capacitor Cr always stays close to its steady-state value Vin/2. In this way, the anomalous current peaks due to V·s unbalance in the transformer are minimized.

To implement burst-mode operation, the voltage applied to the STBY pin needs to be related to the feedback loop. *Figure 14* shows the simplest implementation, suitable to a narrow input voltage range (e.g. when there is a PFC front-end).

Figure 14. Narrow input voltage range

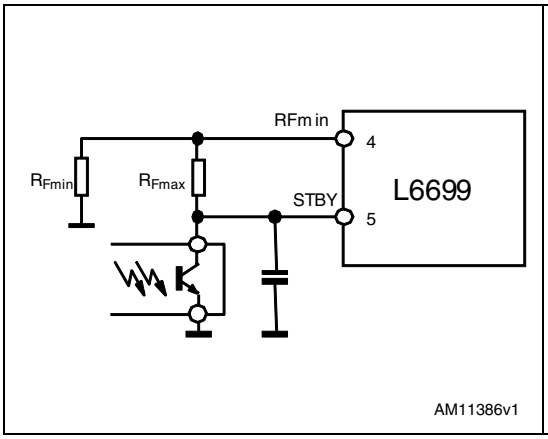
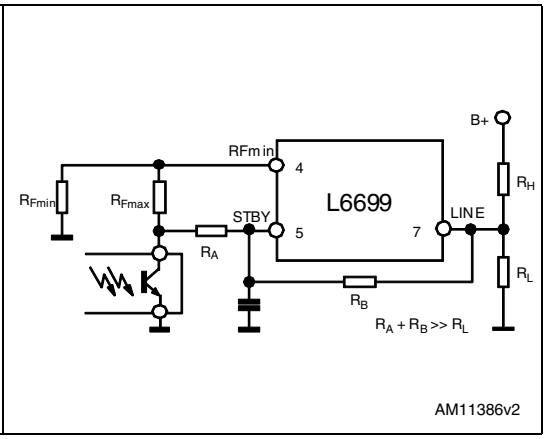


Figure 15. Wide input voltage range



Essentially, RF_{max} defines the switching frequency f_{max} above which the L6699 enters burst-mode operation. Once f_{max} is fixed, RF_{max} is found from the relationship:

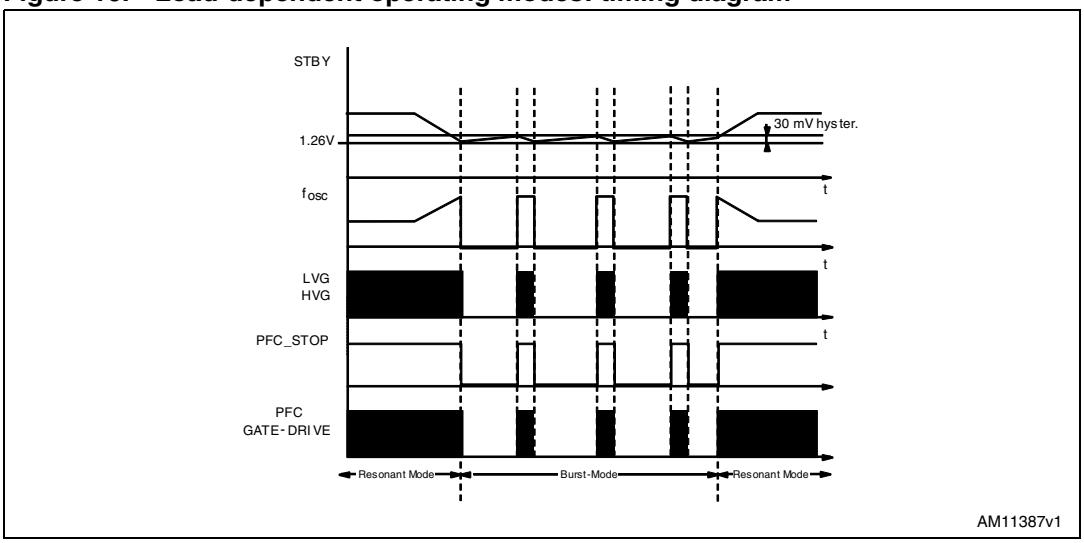
Equation 6

$$RF_{max} = \frac{3}{8} \cdot \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

Note that, unlike the f_{max} considered in the *Section 6.1: Oscillator*, here f_{max} is associated to some load $Pout_B$ greater than the minimum one. $Pout_B$ is normally such that the transformer's peak currents are low enough not to cause audible noise.

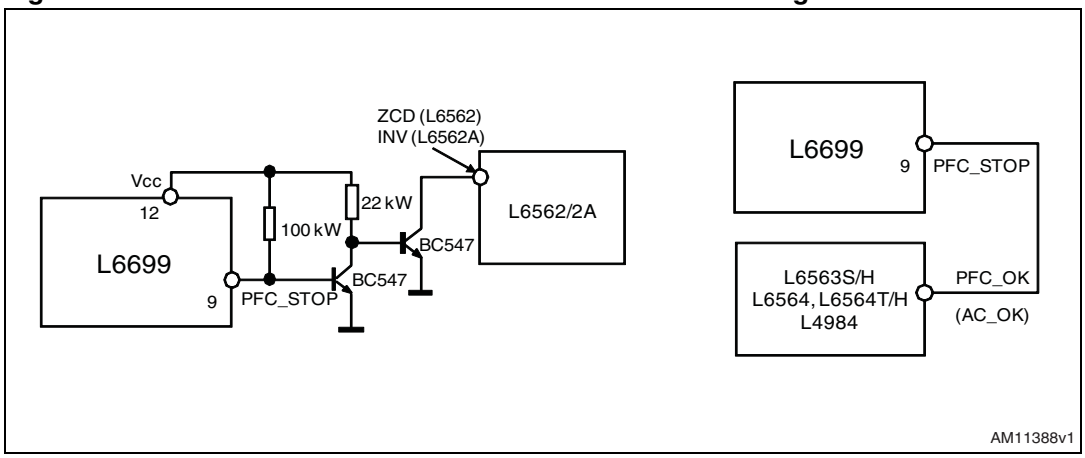
The resonant converter's switching frequency, however, depends also on the input voltage; so, in case there is quite a large input voltage range, with the circuit of *Figure 14* the value of $Pout_B$ would change considerably. In this case it is recommended to use the arrangement shown in *Figure 15*, where the information on the converter's input voltage is added to the voltage applied to the STBY pin. Due to the strongly non-linear relationship between switching frequency and input voltage, it is more practical to find empirically the right amount of correction R_A / (R_A + R_B) needed to minimize the change in $Pout_B$. Take care in choosing the total value R_A + R_B much greater than R_L to minimize the effect on the LINE pin voltage (see *Section 10: Line sensing function*).

Figure 16. Load-dependent operating modes: timing diagram



Whichever circuit is in use, its operation can be described as follows. As the load falls below the value $Pout_B$ the frequency tries to exceed the maximum programmed value f_{max} and the voltage on the STBY pin (V_{STBY}) goes below 1.26 V. The IC then stops with both gate-drive outputs low, so that both MOSFETs of the half bridge leg are in the OFF-state. The voltage V_{STBY} now increases as a result of the feedback reaction to the energy delivery stop and, as it exceeds 1.29 V, the IC restarts switching. After a while, V_{STBY} goes down again in response to the energy burst and stops the IC. In this way the converter works in a burst-mode fashion with a nearly constant switching frequency. A further load decrease then increases the time between consecutive bursts and/or reduces the duration of each burst. This reduces the average switching frequency, which can go down even to few hundred hertz. The timing diagram of *Figure 16* illustrates this kind of operation, showing the most significant signals. A small capacitor (typically in the hundred pF) from the STBY pin to ground, placed as close to the IC as possible to reduce switching noise pick-up, helps obtain clean operation.

Figure 17. How the L6699 can switch off a PFC controller at light load



To help the user meet energy saving requirements even in power-factor-corrected systems, where a PFC pre-regulator precedes the DC-DC converter, the L6699 allows that the PFC pre-regulator can be turned off during burst-mode operation, therefore eliminating the no load consumption of this stage (0.5 - 1 W). There is no compliance issue in that, because EMC regulations on low-frequency harmonic emissions refer to nominal load, no limit is envisaged when the converter operates with light or no load.

To do so, the L6699 provides pin 8 (PFC_STOP): it is an open drain output, normally open, that is asserted low when the IC is idle during burst-mode operation. This signal is externally used for switching off the PFC controller and the pre-regulator as shown in *Figure 17*. When the L6699 is in UVLO the pin is kept open to allow the PFC controller to start first.

The PFC_STOP pin is also used by some protection functions (OCP, OLP and latched shutdown). Please refer to the relevant sections for more information.

8 Current sensing, OCP and OLP

In the L6699 the current sense input ISEN (pin 6) senses the current flowing in the resonant tank to perform multiple tasks:

1. Primary overcurrent protection (OCP function).
2. Hard-switching cycles prevention at startup (see *Section 6.3: Safe-start procedure*).
3. Capacitive-mode detection during operation (see *Section 9: Capacitive-mode detection function*).

In this section the discussion is concentrated on the OCP function.

Unlike PWM-controlled converters, where energy flow is controlled by the duty cycle of the primary switch (or switches), in a resonant half bridge the duty cycle is fixed and energy flow is controlled by its switching frequency. This has an impact on the way current limitation can be realized. While in PWM-controlled converters energy flow can be limited simply by terminating switch conduction in advance when the sensed current exceeds a preset threshold (cycle-by-cycle limitation), in a resonant half bridge the most efficient way to reduce an excessive current level is to increase the switching frequency, i.e. the oscillator frequency.

In *Figure 18* and *19* a couple of current sensing methods are illustrated.

Figure 18. Current sensing techniques with sense resistor

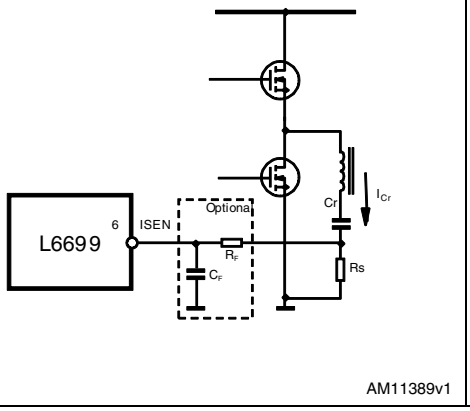
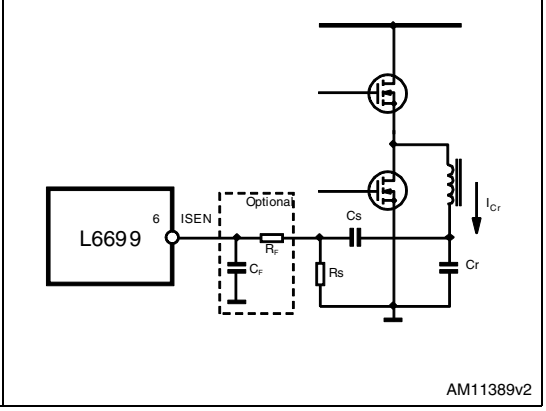


Figure 19. Current sensing techniques “lossless”, with capacitive shunt



Note: The L6699 must sense the instantaneous tank current for proper operation of the smooth startup function and the capacitive-mode detection circuit. Therefore, if a smoothing RC circuit (the one shown in the dashed box) is used to reduce the noise level on the ISEN pin, its time constant RF CF should be in the range of 100 - 200 ns. With slightly longer time constants it is recommended that converter operation close to the capacitive-mode boundary and during short-circuit, as well as at the end of the smooth-start phase, be checked for possible hard-switching cycles. With considerably longer time constants (> 200 ns) hard-switching under the above mentioned conditions becomes very likely.

The ISEN pin, which is also able to withstand negative voltages, is internally connected to the input of a first comparator, referenced to V_{ISENx} (0.8 V typ. 0.76 V min.), and to that of a second comparator referenced to 1.5 V. The operation of the second comparator is described later.

If the voltage externally applied to the pin by either circuit in *Figure 18* and *19* exceeds 0.8 V the first comparator is tripped and this causes an internal switch to be turned on for 5 µs and discharges the soft-start capacitor C_{SS} (see *Section 6.3: Safe-start procedure*). This quickly increases the oscillator frequency and thereby limits energy transfer. Under output short-circuit conditions, this operation results in a peak primary current that periodically oscillates below the maximum value allowed by the sense resistor Rs.

In the circuit shown in *Figure 18*, Rs is placed directly in series to the resonant tank. Its value can be determined using the equation:

Equation 7

$$Rs = \frac{0.76}{I_{Crpkx}}$$

where I_{Crpkx} is the maximum expected peak current flowing through the resonant capacitor and the primary winding of the transformer, which is related to the maximum load and the minimum input voltage. The power dissipation in Rs can be approximately found with:

Equation 8

$$P_{Rs} \approx 0.4 \cdot I_{Crpkx}$$

The circuit shown in *Figure 19* operates as a capacitive current divider; Cs is typically selected equal to Cr/100 or less and is a low-loss type, and the sense resistor Rs is selected as:

Equation 9

$$Rs = \frac{0.77}{I_{Crpkx}} \cdot \left(1 + \frac{C_r}{Cs}\right)$$

and the associated power dissipation is reduced by a factor (1+Cr/Cs). This circuit is then recommended when the efficiency target is very high.

This OCP is effective in limiting primary-to-secondary energy flow in case of an overload or an output short-circuit, but the output current through the secondary winding and rectifiers under these conditions may be so high that it endangers converter safety if continuously flowing. To prevent any damage it is customary to force the converter to work intermittently, which brings the average output current to values such that the thermal stress for the transformer and the rectifiers can be easily handled.

If intermittent operation upon overload or short-circuit is desired, the designer can program externally the maximum time T_{SH} that the converter is allowed to run under these conditions. Overloads or short-circuits lasting less than T_{SH} do not cause any other action,

therefore providing the system with immunity to short duration phenomena. If, instead, T_{SH} is exceeded, an overload protection (OLP) procedure is activated that shuts down the L6699 and, in case of continuous overload/short-circuit, results in continuous intermittent operation with a user-defined duty cycle.

This function is realized on pin 2 (DELAY), with a capacitor C_{Delay} and a parallel resistor R_{Delay} connected to ground. As the voltage on the ISEN pin exceeds 0.8 V, the first OCP comparator, in addition to turning on the switch that discharges C_{SS}, turns on a current generator that sources 350 µA for 50 µs from the DELAY pin and charges C_{Delay}. During an overload/short-circuit the OCP comparator and the internal current source is repeatedly activated and C_{Delay} is charged with an average current depending essentially on C_{SS}, R_{SS}, the characteristics of the resonant circuit, and the short-circuit impedance; the discharge due to R_{Delay} is negligible because the associated time constant is typically much longer.

This operation continues until the voltage on C_{Delay}, V(DELAY), reaches 2 V, which defines the time T_{SH}, or until the overload/short-circuit disappears, whichever occurs first. There is not a simple relationship that links T_{SH} to C_{Delay}, so it is more practical to determine C_{Delay} experimentally. As a rough indication, using 1 µF for C_{Delay}, T_{SH} should be around 100 ms in case of a dead short on the output.

In the case of an overload lasting less than T_{SH}, C_{Delay} is no longer charged, so its voltage decays with the time constant $C_{Delay} \cdot R_{Delay}$. Note that the value of T_{SH} for the next overload is shorter if this occurs before C_{Delay} is totally discharged. If, on the other hand, it is charged up to 2 V, the internal switch that discharges C_{SS} is continuously turned on, the PFC_STOP pin is pulled low, and the 350 µA current source is forced continuously on until V(DELAY) reaches 3.5 V. This phase lasts:

Equation 10

$$T_{MP} \approx 4.3 \cdot C_{Delay}$$

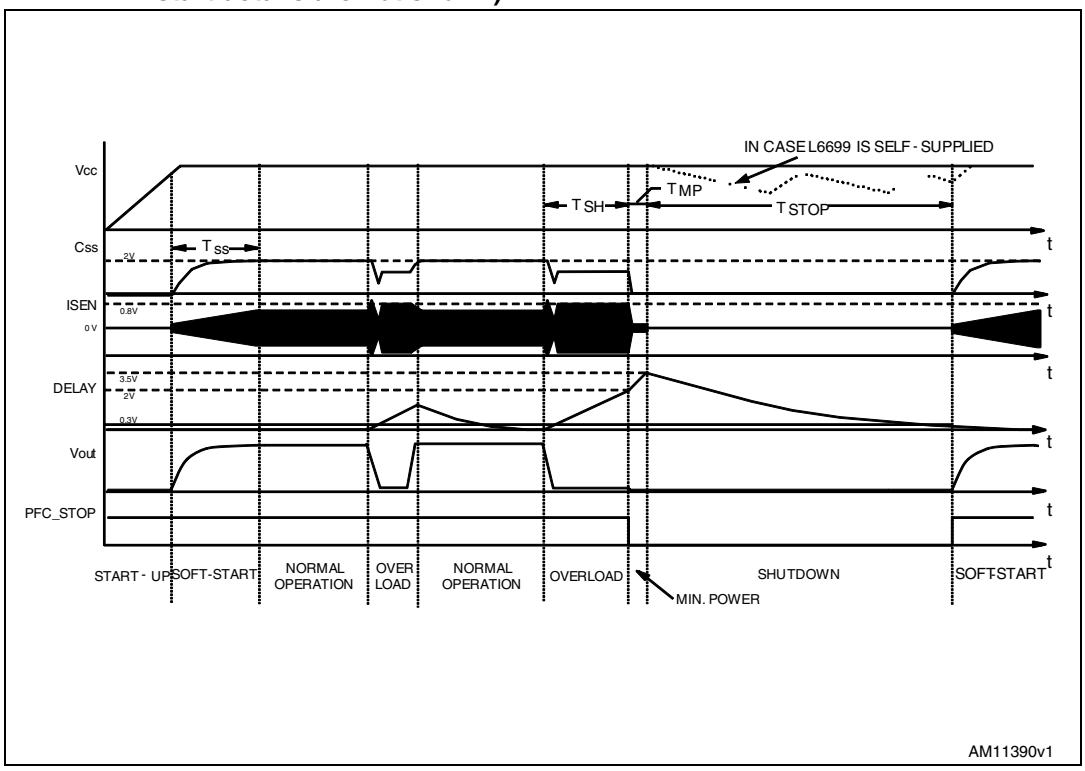
with T_{MP} expressed in ms and C_{Delay} in µF. During this time the L6699 runs at a frequency close to f_{start} (see *Section 6.3: Safe-start procedure*) to minimize the energy inside the resonant circuit. As V(DELAY) equals 3.5 V, the L6699 stops switching and the internal 350 µA generator is turned off, so that C_{Delay} is slowly discharged by R_{Delay}. The IC restarts when V(DELAY) falls below 0.3 V, which takes:

Equation 11

$$T_{STOP} = R_{Delay} \cdot C_{Delay} \cdot \ln \frac{3.5}{0.33} \approx 2.4 \cdot R_{Delay} \cdot C_{Delay}$$

The timing diagram of *Figure 20* shows this operation. Note that if during TSTOP the supply voltage of the L6699 (V_{CC}) falls below the UVLO threshold the IC records the event and does not restart immediately after V_{CC} exceeds the startup threshold, if V(DELAY) is still higher than 0.3 V. Also the PFC_STOP pin stays low as long as V(DELAY) is greater than 0.3 V.

Figure 20. Soft-start and delayed shutdown upon overcurrent timing diagram (safe-start details are not shown)



In applications where continuous operation of the converter is needed even under overload conditions, the delayed shutdown function can be disabled by simply grounding the DELAY pin.

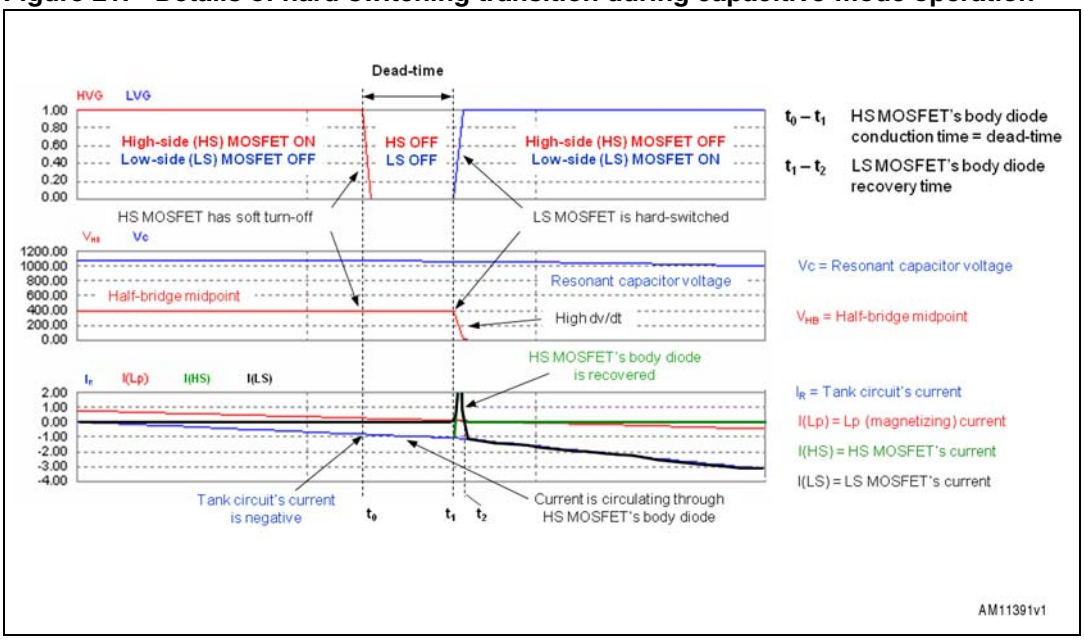
If the voltage on the ISEN pin reaches 1.5 V, the second comparator is triggered. Switching is stopped immediately and both the internal switch that discharges C_{SS} and the 350 µA current source on the DELAY pin are forced continuously on. As V(DELAY) equals 3.5 V the 350 µA generator is turned off, so that C_{Delay} is slowly discharged by R_{Delay}. The L6699 restarts when V(DELAY) falls below 0.3 V.

9 Capacitive-mode detection function

Normally, the resonant half bridge converter operates with the resonant tank current lagging behind the square-wave voltage applied by the half bridge leg, like a circuit having a reactance of an inductive nature. In this way the applied voltage and the resonant current have the same sign at every transition of the half bridge, which is a necessary condition in order for soft-switching to occur (zero-voltage switching, ZVS at turn-on for both MOSFETs). Therefore, should the phase relationship reverse, i.e. the resonant tank current anticipates the applied voltage, like in circuits having a capacitive reactance, soft-switching would be lost. This is termed capacitive-mode operation and must be avoided because of its significant drawbacks:

1. Both MOSFETs feature hard-switching at turn-on, like in conventional PWM-controlled converters (see *Figure 21*). The associated capacitive losses may be considerably higher than the total power normally dissipated under “soft-switching” conditions and this may easily lead to their overheating, since heatsinking is not usually sized to handle this abnormal condition.
2. The body diode of the MOSFET just switched off conducts current during deadtime and its voltage is abruptly reversed by the other MOSFET turned on (see *Figure 21*). Therefore, once reverse-biased, the conducting body diode keeps its low impedance until it recovers, therefore creating a condition equivalent to a shoot-through of the half bridge leg. This is a potentially destructive condition (see next point) and causes additional power dissipation due to the current and voltage of the conducting body diode simultaneously high during part of its recovery.
3. There is an extremely high reverse dv/dt (many tens of V/ns!) experienced by the conducting body diode at the end of its recovery with the other MOSFET turned on. This dv/dt may exceed the rating of the MOSFET and lead to an immediate failure because of the second breakdown of the parasitic BJT intrinsic in its structure. If a MOSFET is hot, the turn-on threshold of its parasitic BJT is lower, and dv/dt-induced failure is much more likely. The L6699 may be also damaged if its OUT pin is subject to a dv/dt exceeding the AMR (50 V/ns).

Figure 21. Details of hard-switching transition during capacitive-mode operation



4. When either MOSFET is turned on, the other one can be parasitically turned on too, if the current injected through its Cgd and flowing through the gate driver's pull-down is large enough to raise the gate voltage close to the turn-on threshold This would be a lethal shoot-through condition for the half bridge leg.
5. The recovery of the body diodes generates large and energetic negative voltage spikes because of the unavoidable parasitic inductance of the PCB subject to its di/dt. These are coupled to the OUT pin and may damage the L6699.
6. There is a large common-mode EMI generation that adversely affects EMC.

Resonant converters work in capacitive mode when their switching frequency falls below a critical value that depends on the loading conditions and the input-to-output voltage ratio. They are especially prone to enter capacitive-mode when the input voltage is lower than the minimum specified and/or the output is overloaded or short-circuited. Designing a converter so that it never works in capacitive-mode, even under abnormal operating conditions, is definitely possible but this may pose unacceptable design constraints in some cases.

To prevent the severe drawbacks of capacitive-mode operation, while enabling a design that needs to ensure inductive-mode operation only in the specified operating range, neglecting abnormal operating conditions, the L6699 provides the capacitive-mode detection function.

The IC monitors the phase relationship between the tank current circuit sensed on the ISEN pin and the voltage applied to the tank circuit by the half bridge, checking that the former lags behind the latter (inductive-mode operation). If the phase-shift approaches zero, which is indicative of impending capacitive-mode operation, the monitoring circuit activates the OCP procedure (see *Section 8: Current sensing, OCP and OLP*) so that the resulting frequency rise keeps the converter away from that dangerous condition. Also in this case the DELAY pin is activated, so that the OLP function, if used, is eventually tripped after a time T_{SH} causing intermittent operation and reducing thermal stress.

If the phase relationship reverses abruptly (which may happen in case of dead short at the converter's output), the L6699 is stopped immediately, the soft-start capacitor C_{SS} is totally discharged and a new soft-start cycle is initiated after 50 µs idle time. During this idle period the PFC_STOP pin is pulled low to stop the PFC stage as well.

10 Line sensing function

This function basically stops the IC as the input voltage to the converter falls below the specified range and lets it restart as the voltage goes back within the range. The sensed voltage can be either the rectified and filtered mains voltage, in which case the function acts as a brownout protection, or, in systems with a PFC pre-regulator front-end, the output voltage of the PFC stage, in which case the function serves as a power-on and power-off sequencing.

L6699 shutdown upon input undervoltage is accomplished by means of an internal comparator, as shown in the block diagram of *Figure 22*, whose non-inverting input is available at pin 7 (LINE). The comparator is internally referenced to 1.22 V and disables the IC if the voltage applied at the LINE pin is below the internal reference. Under these conditions the soft-start is discharged, the PFC_STOP pin is open and the consumption of the IC is reduced. PWM operation is re-enabled as the voltage on the pin is above the reference. The comparator is provided with current hysteresis instead of a more usual voltage hysteresis: an internal 13 µA current sink is ON as long as the voltage applied at the LINE pin is below the reference and is OFF if the voltage is above the reference.

This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With voltage hysteresis, on the other hand, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

With reference to *Figure 22*, the following relationships can be established for the ON (Vin_{ON}) and OFF (Vin_{OFF}) thresholds of the input voltage:

Equation 12

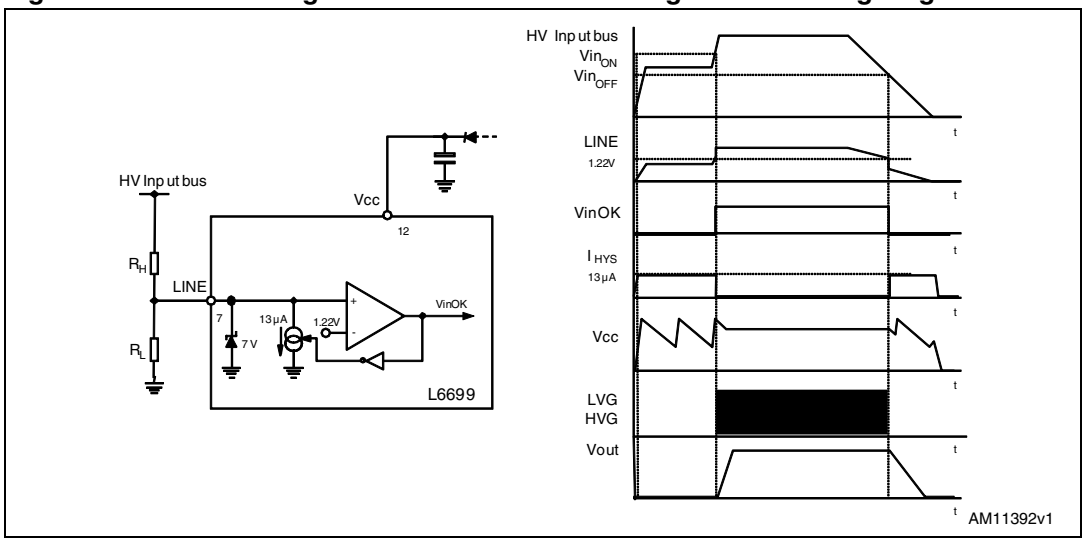
$$\frac{Vin_{ON} - 1.25}{R_H} = 13 \cdot 10^{-6} + \frac{1.25}{R_L} \quad ; \quad \frac{Vin_{OFF} - 1.25}{R_H} = \frac{1.25}{R_L}$$

which, solved for R_H and R_L, yields:

Equation 13

$$R_H = \frac{Vin_{ON} - Vin_{OFF}}{13 \cdot 10^{6}} \quad ; \quad R_L = R_H \frac{1.25}{Vin_{OFF} - 1.25}$$

Figure 22. Line sensing function: internal block diagram and timing diagram



While the line undervoltage is active there is no switching activity, therefore the V_{CC} voltage (if not supplied by another source) continuously oscillates between the startup and the UVLO thresholds, as shown in the timing diagram of *Figure 22*.

The LINE pin, while the device is operating, is a high impedance input connected to high value resistors, so it is prone to pick-up noise,. This might alter Vin_{OFF} or give rise to undesired switch-off of the IC during ESD tests. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

If the function is not used the pin can be pulled high by connecting it to V_{CC} through a resistor in the hundred kΩ

11 Latched shutdown

The L6699 is equipped with a comparator having the non-inverting input externally available on pin 8 (DIS) and with the inverting input internally referenced to 1.85 V. As the voltage on the pin exceeds the internal threshold, the IC is immediately shut down, the PFC_STOP pin is asserted low and the quiescent consumption reduced to a low value. The information is latched and it is necessary to let the voltage on the V_{CC} pin go below the UVLO threshold to reset the latch, de-assert the pin PFC_STOP, and restart the IC.

This function is useful to implement a latched overtemperature protection very easily by biasing the pin with a divider from an external reference voltage (e.g. pin 4, RF_{min}), where the upper resistor is an NTC physically located close to a heating element like the MOSFET, or a secondary diode or the transformer.

An OVP can be implemented as well, e.g. by sensing the output voltage and transferring an overvoltage condition via an optocoupler. A latch-mode OCP protection can be implemented by connecting this pin to DELAY (pin 2).

12 Bootstrap section

The supply of the floating high-side section is obtained by means of a bootstrap circuitry. This solution normally requires a high voltage fast-recovery diode (D_{BOOT}, *Figure 23*) to charge the bootstrap capacitor C_{BOOT}. In the L6699 a patented integrated structure, replaces this external diode. It is realized by means of a high voltage DMOS, working in the third quadrant and driven synchronously with the low-side driver (LVG), with a diode in series to the source, as shown in *Figure 24*.

The diode prevents that any current can flow from the V_{BOOT} pin back to V_{CC} if the supply is quickly turned off when the internal capacitor of the pump is not fully discharged. To drive the synchronous DMOS, a voltage higher than the supply voltage V_{CC} is necessary. This voltage is obtained by means of an internal charge pump (*Figure 24*).

The bootstrap structure introduces a voltage drop while recharging C_{BOOT} (i.e. when the low side driver is on), which increases with the operating frequency and with the size of the external Power MOSFET. It is the sum of the drop across the $R_{DS(on)}$ and the forward drop across the series diode. At low frequency this drop is very small and can be neglected but, as the operating frequency increases, it must be taken into account. In fact, the drop reduces the amplitude of the driving signal and can significantly increase the $R_{DS(on)}$ of the external high-side MOSFET and then its conductive loss.

Figure 23. Bootstrap supply: standard circuit

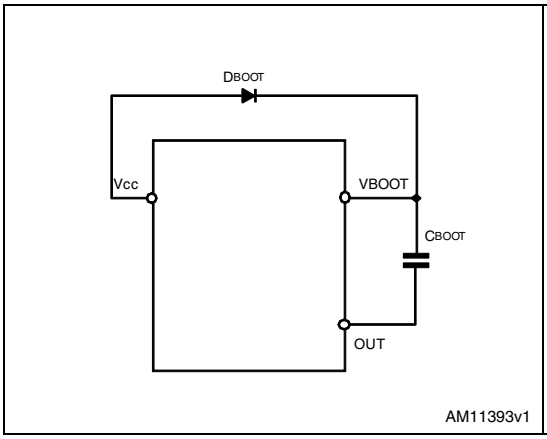
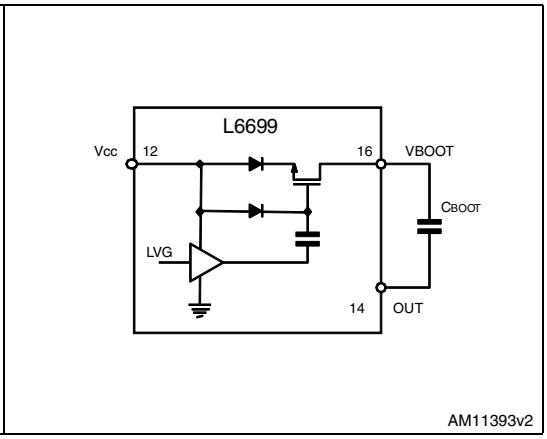


Figure 24. Bootstrap supply: internal bootstrap synchronous diode



This concern applies to converters designed with a high resonance frequency (indicatively, > 150 kHz), so that they run at high frequency also at full load. Otherwise, the converter runs at high frequency at light load, where the current flowing in the MOSFETs of the half bridge leg is low, so that, generally, a slight $R_{DS(on)}$ rise is not an issue. However, it is wise to check this point anyway and the following equation is useful to estimate the drop on the bootstrap driver:

Equation 14

$$V_{Drop} = I_{charge} R_{(DS)on} + V_F = \frac{Q_g}{T_{charge}} R_{(DS)on} + V_F$$

where Qg is the gate charge of the external Power MOSFET, $R_{DS(on)}$ is the ON-resistance of the bootstrap DMOS (150 Ω typ.) and T_{charge} is the ON-time of the bootstrap driver, which equals about half the switching period minus the deadtime T_D. For example, using a MOSFET with a total gate charge of 30 nC, the drop on the bootstrap driver is about 3 V at a switching frequency of 200 kHz and with a deadtime of 300 ns:

Equation 15

$$V_{Drop} = \frac{30 \cdot 10^{-9}}{2.5 \cdot 10^{-6} - 0.3 \cdot 10^{-6}} 150 + 0.6 = 2.6\ V$$

If a significant drop on the bootstrap driver is an issue, an external ultra-fast diode can be used, therefore saving the drop on the $R_{DS(on)}$ of the internal DMOS. In this case it is also recommended to add a small resistor (in the ten Ω) in series to the diode to prevent the bootstrap capacitor from being charged to a voltage exceeding the absolute maximum rating (18 V), in case of significant negative spikes on the half bridge midpoint when the high-side MOSFET turns off.

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 25. SO16N dimensions

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 26. Package drawing

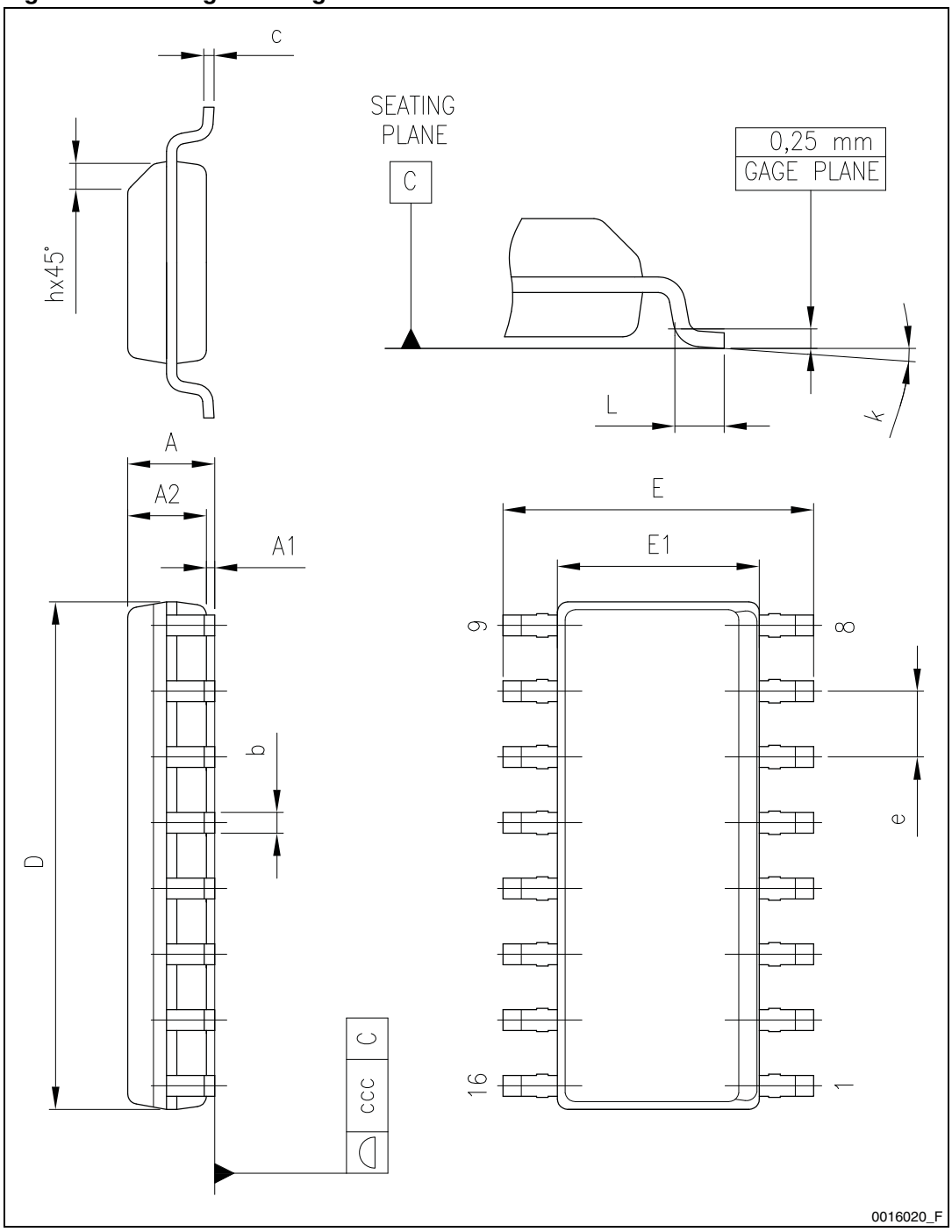
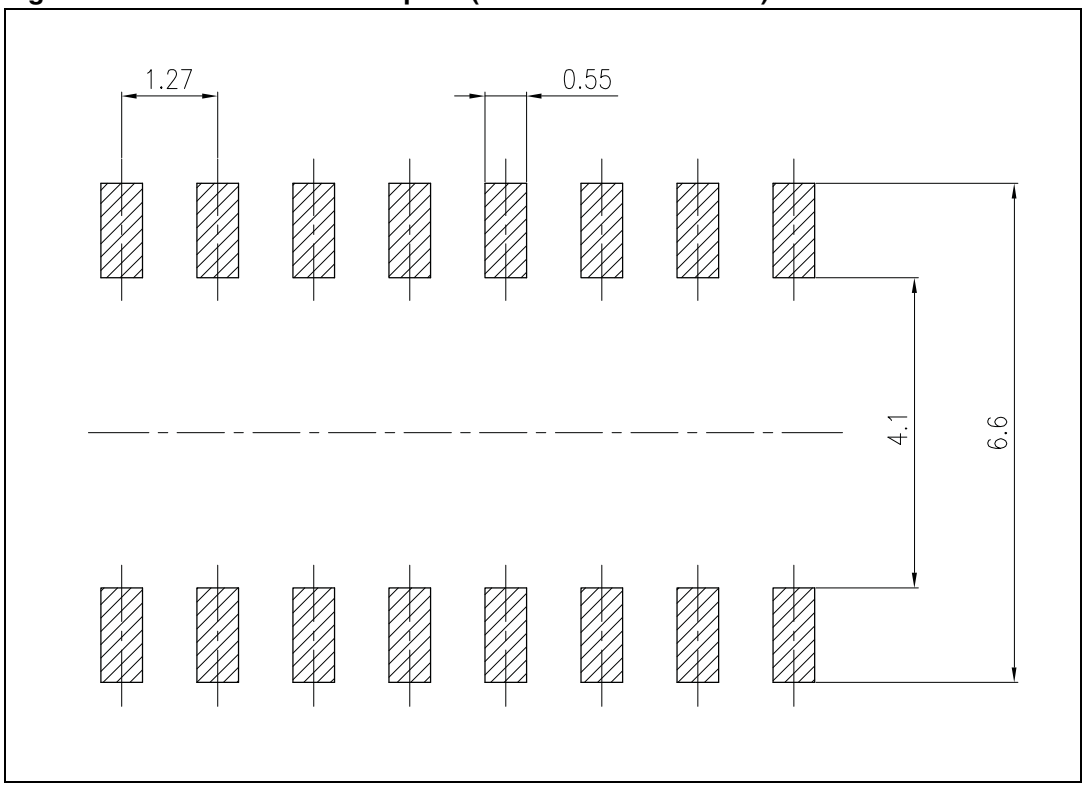


Figure 27. Recommended footprint (dimensions are in mm)



14 Revision history

Table 7. Document revision history

Date	Revision	Changes
12-Apr-2012	1	Initial release.
16-Jan-2013	2	Updated *Table 2: Absolute maximum ratings on page 5*.

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