BGS14MA11

MIPI 2.0 SP4T switch for LTE diversity, Tx and LAA applications

Key Features

- 0.1 to 6.0 GHz coverage for LTE and LAA application
- LTE TX power handling capabilities
- Ultra low insertion loss: 0.3dB for band 41 and 0.85dB for LTE U/ LAA
- Small form factor 1.15mm x 1.55mm
- Fully compatible with MIPI 2.0 RFFE standard
- Select pin for USID allows two devices per MIPI RFFE bus
- No decoupling capacitors required (Unless DC applied on RF lines)

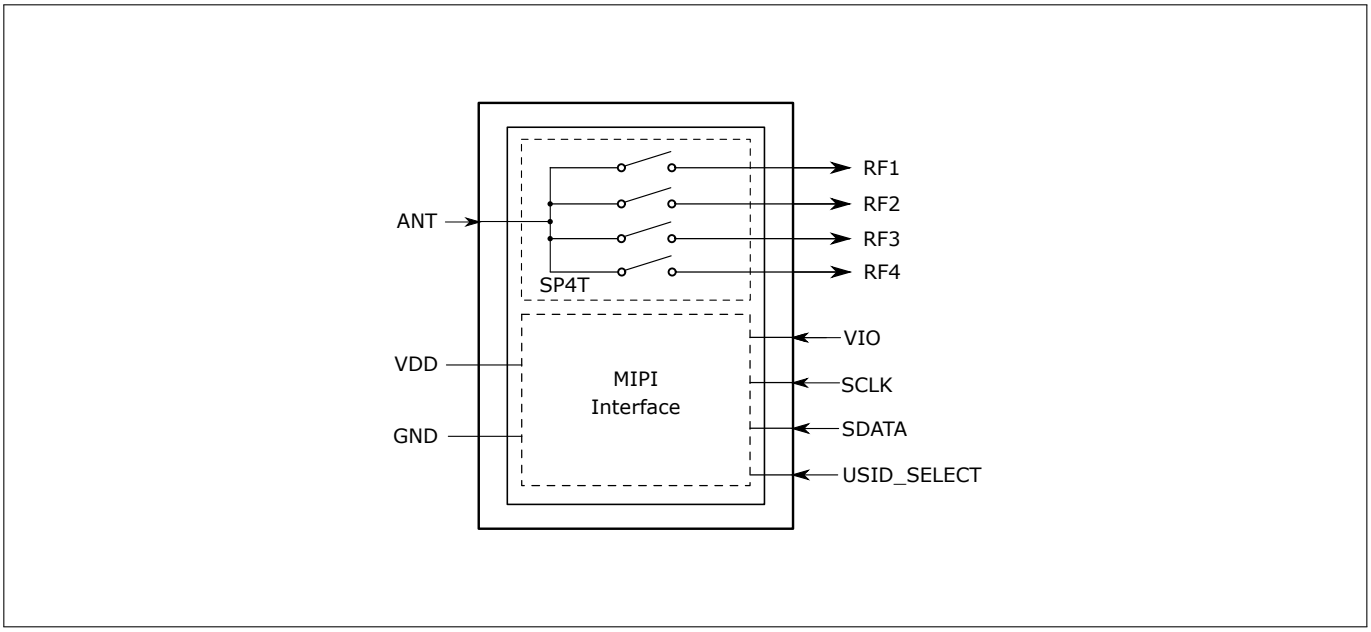
Applications

The SP4T switch is a band selection switch for LTE applications. With LTE TX power handling capability it's suitable for both LTE diversity path and LTE uplink Tx applications. The switch covers up to 6GHz so it supports Band 42, Band 43 and also LAA.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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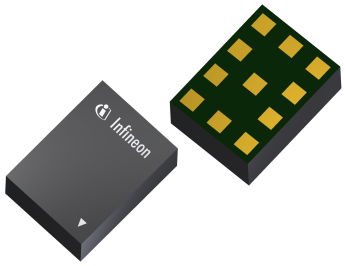
1 Features



- Ultra low insertion loss 0.3dB for band 41 and 0.85dB for LTE U/ LAA
- LTE TX Power Handling Capabilities
- 0.1 to 6.0 GHz coverage for LTE and LAA application
- Low harmonic generation
- High port-to-port-isolation
- Suitable for C2K / LTE / WCDMA Applications
- On chip control logic including ESD protection
- Fully compatible with MIPI 2.0 RFFE standard
- Software programmable MIPI RFFE USID
- USID swap feature
- Small form factor 1.15mm x 1.55mm
- No power supply blocking required
- Select pin for USID allows two devices per MIPI RFFE bus
- No decoupling capacitors required (Unless DC applied on RF lines)
- High EMI robustness
- RoHS and WEEE compliant package

RoHS

Description

This SP4T RF switch is a perfect solution for multimode handsets based on LTE and WCDMA. It is based on Infineon's proprietary technology and has excellent RF performance. The ultra-low insertion loss helps customers to achieve high system sensitivity, the coverage of LTE Tx power and 6GHz enables very broad application. It features DC-free RF ports, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Its on chip MIPI RFFE 2.0 controller is fully compatible with industry standard, with external USID_SEL pin it can support two devices per MIPI RFFE bus.

Product Name	Marking	Package
BGS14MA11	A1	ATSLP-11

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	6.0	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power at all TRx ports	P_{RF_max}	–	–	35	dBm	short momentary / 50Ω
ESD capability, CDM [3]	$V_{ESD_{CDM}}$	-500	–	+500	V	
ESD capability, HBM [4]	$V_{ESD_{HBM}}$	-1	–	+1	kV	
ESD capability, system level (RF port) [5]	$V_{ESD_{ANT}}$	-8	–	+8	kV	ANT vs system GND, with 27 nH shunt inductor
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider potential ripple voltages on top of V_{DD}. Including RF ripple, V_{DD} must not exceed the maximum ratings: $V_{DD} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 2: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	–	62	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports

3 Operation range

Table 3: Operation range at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.7	1.8	3.4	V	–
Supply Current	I_{DD}	–	60	125	µA	–
Supply Current in Standby mode	I_{DD_SB}	–	0.5	1	µA	VIO=low or MIPI lowpower mode
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	2	–	µA	Idle State

[1]SCLK and SDATA

Table 4: RF input power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power on TRX ports	P_{RF}	–	–	34	dBm	CW / VSWR 1:1 / 25 °C
RF input power on TRX ports	P_{RF}	–	–	29	dBm	CW / VSWR 6:1 / 85 °C

4 RF Characteristics

Table 5: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 1.7...3.4V, unless otherwise specified. Open ports are terminated with 50 Ω.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All TRx Ports	IL	–	0.20	0.40	dB	698–960 MHz
		–	0.23	0.45	dB	1428–1920 MHz
		–	0.25	0.45	dB	1990–2170 MHz
		–	0.26	0.50	dB	2170–2690 MHz
		–	0.40	0.60	dB	3400–3600 MHz
		–	0.42	0.70	dB	3600–3800 MHz
		–	0.85	1.50	dB	5000–6000 MHz
Return Loss[1]						
All TRx Ports	RL	23	27	–	dB	698–960 MHz
		19	21	–	dB	1428–1920 MHz
		18	20	–	dB	1990–2170 MHz
		17	19	–	dB	2170–2690 MHz
		14	16	–	dB	3400–3600 MHz
		14	15	–	dB	3600–3800 MHz
		10	11	–	dB	5000–6000 MHz
Isolation[1] [2]						
All TRx Ports	ISO	36	40	–	dB	698–960 MHz
		30	35	–	dB	1428–1920 MHz
		28	32	–	dB	1990–2170 MHz
		26	28	–	dB	2170–2690 MHz
		22	26	–	dB	3400–3600 MHz
		21	25	–	dB	3600–3800 MHz
		14	18	–	dB	5000–6000 MHz
Harmonic Generation (UMTS Band 1, Band 5)[1]						
2nd harmonic generation	P_{H2}	–	-72	-66	dBm	25 dBm, 50 Ω, CW mode
3rd harmonic generation	P_{H3}	–	-74	-71	dBm	25 dBm, 50 Ω, CW mode
Intermodulation Distortion (UMTS Band 1, Band 5)[1]						
2nd order intermodulation	IMD2 low	–	–	-110	dBm	IMT, US Cell (see Tab. 7)
3rd order intermodulation	IMD3	–	–	-110	dBm	IMT, US Cell (see Tab. 8)
2nd order intermodulation	IMD2 high	–	–	-110	dBm	IMT, US Cell (see Tab. 7)

[1] On application board without any matching components.
[2] Isolation to inactive ports when one path is active (port to port isolation).

Table 6: Switching Time at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 1.7...3.4V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
RF Rise Time	t_{RT}	–	–	2	µs	10 % to 90 % RF signal
Switching Time	t_{ST}	–	3	4.5	µs	50% last SCLK falling edge to 90% RF signal, see Fig. 1
Power Up Settling Time	t_{Pup}	–	10	25	µs	After power down mode

[1] Don't change switch state during first 10µs of power-up.

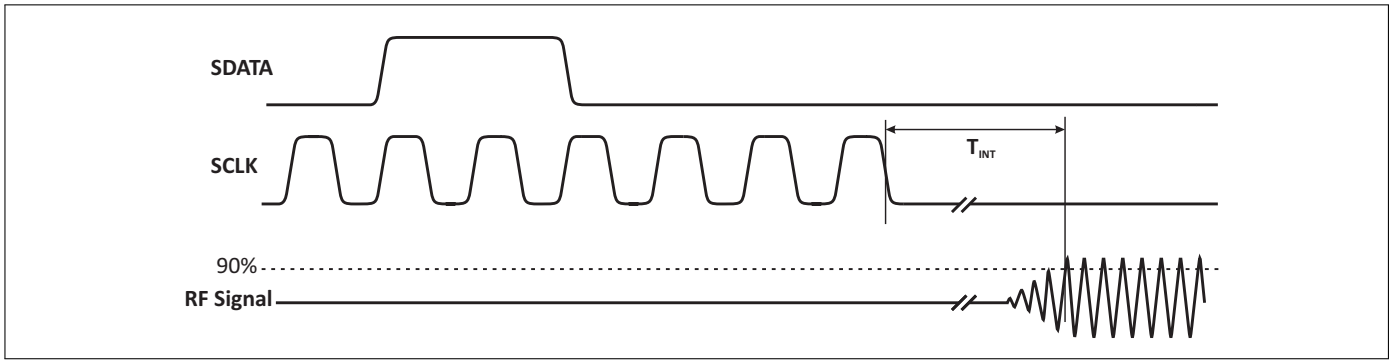


Figure 1: MIPI to RF time

Table 7: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	15	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	15	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 8: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

5 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0 - 25. September 2014.

Table 9: MIPI Features

Feature	Supported	Comment
MIPI RFFE 1.10 and 2.0 standards	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write[1)]
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register[1)]
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin to provide 2 USIDs. See Tab. 10

[1)] only supported by MIPI 2.0 Standard

Table 10: MIPI USID Selection

Selection Pin Level [1]	Default Connection
USID_SEL= GND	USID= 0xD
USID_SEL= VIO	USID= 0x1

[1] No unspecified voltage levels including floating are allowed.

Table 11: Startup Behavior

Feature	State	Comment
Power status	Power down mode	Power down mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 12: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	SW_CTRL0	6:0	SW_CTRL0	RF Switch Control	0	No	Yes	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	33	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	0x1A	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 10	No	No	R/W

Table 13: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PROD_ID[1)]	7:0	EXT_PRODUCT_ID		0x00	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0x4	No	No	R/W
		3:0	SUB_REVISION		0x0			
0x22	GSID[1)]	7:4	GSID0[3:0]	Primary Group Slave ID.	0x0	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0x0			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM[1)]	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PAR_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_ PAR_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PAR_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

[1)] Only supported by MIPI 2.0 Standard

Table 14: Modes of Operation (Truth Table, Register_0)

State	Value (Bin.)	Mode
1	00000000	ALL OFF (Isolation)
2	00000001	RF1 ON
3	00000010	RF2 ON
4	00000100	RF3 ON
5	00001000	RF4 ON
6	00000011	RF1 and RF2 ON
7	00000101	RF1 and RF3 ON
8	00001001	RF1 and RF4 ON
9	00000110	RF2 and RF3 ON
10	00001010	RF2 and RF4 ON
11	00001100	RF3 and RF4 ON
12	00000111	RF1 and RF2 and RF3 ON
13	00001011	RF1 and RF2 and RF4 ON
14	00001101	RF1 and RF3 and RF4 ON
15	00001110	RF2 and RF3 and RF4 ON
16	00001111	RF1 and RF2 and RF3 and RF4 ON
17	00XX0000	ALL OFF (Isolation)

[1] Reserved

6 Package related information

The switch has a package size of 1150 µm in x-dimension and 1550 µm in y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 16.

Table 15: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-Dimension	X	1150 ± 50	µm
Package Y-Dimension	Y	1550 ± 50	µm
Package Height	H	0.65 max	µm

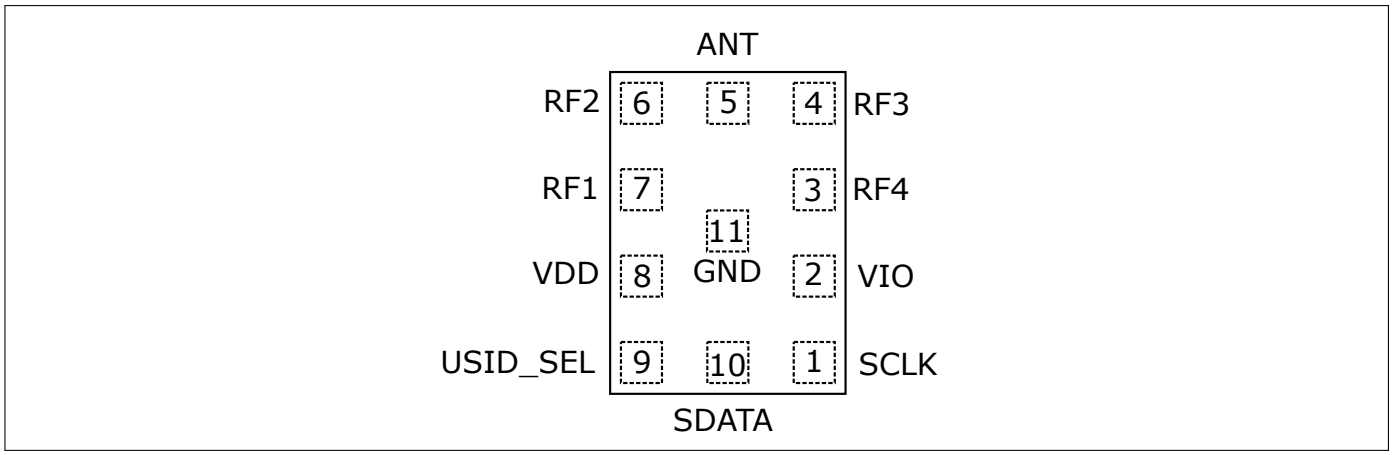


Figure 2: Footprint, top view

Table 16: Pin Definition

No.	Name	Pin Type	Function
1	SCLK	I/O	MIPI RFFE Clock (Input)
2	VIO	Power	MIPI RFFE Power Supply
3	RF4	RF	Rx port 4
4	RF3	RF	Rx port 3
5	ANT	RF	RF Input port
6	RF2	RF	Rx port 2
7	RF1	RF	Rx port 1
8	VDD	Power	Power supply
9	USID-SEL	I/O	User ID selection pin
10	SDATA	I/O	MIPI RFFE Data
11	GND	Ground	Ground

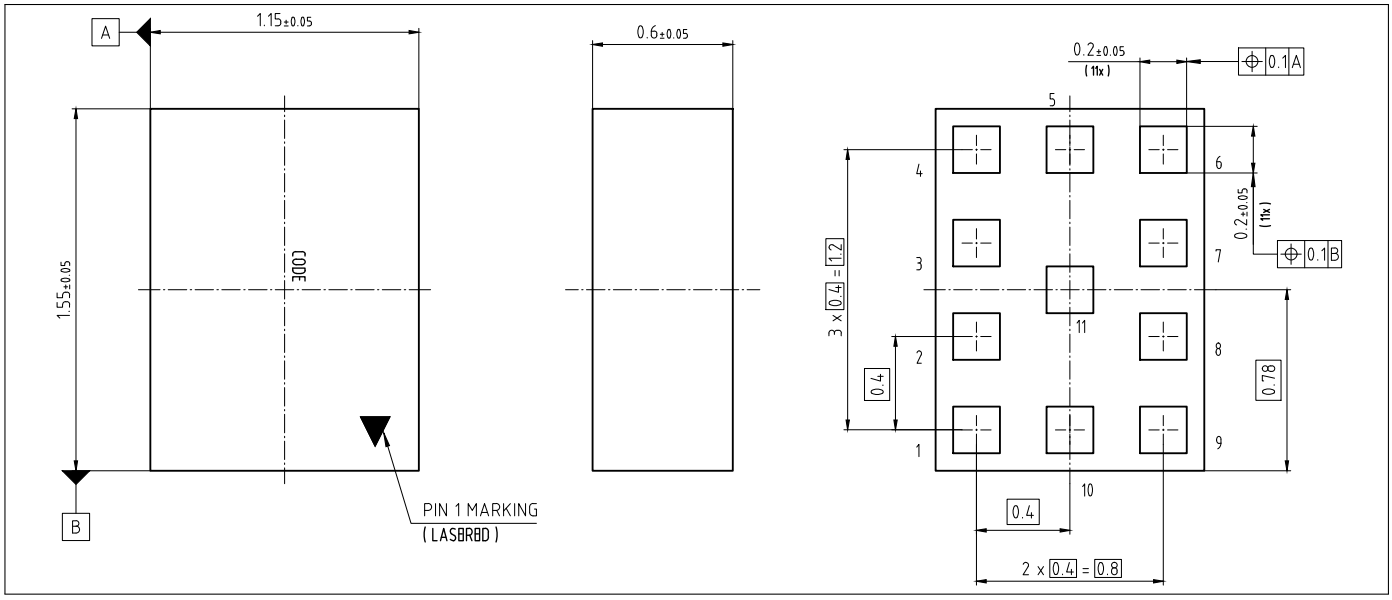


Figure 3: Package Outline Drawing (top, side and bottom views)

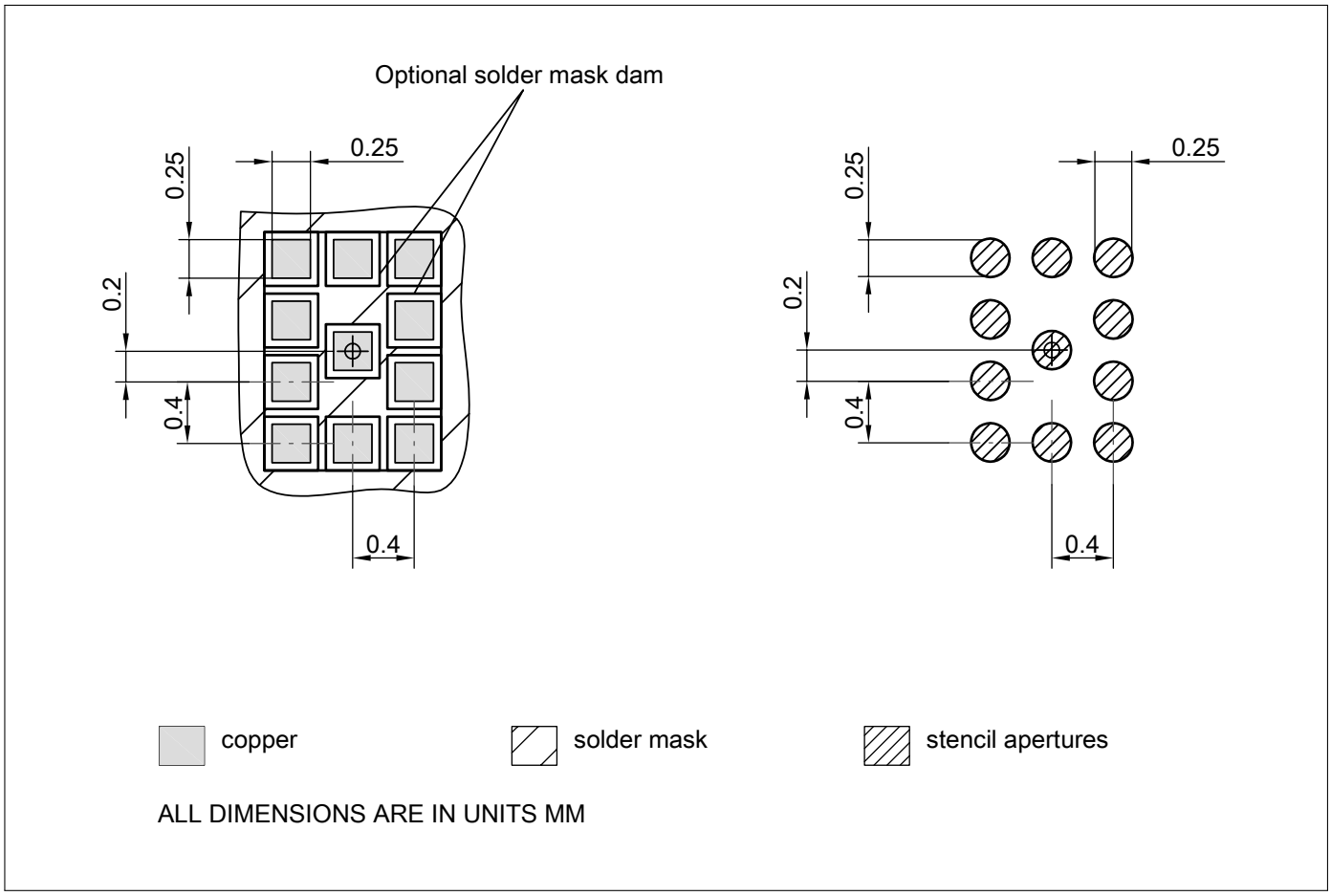


Figure 4: Land Pattern Drawing

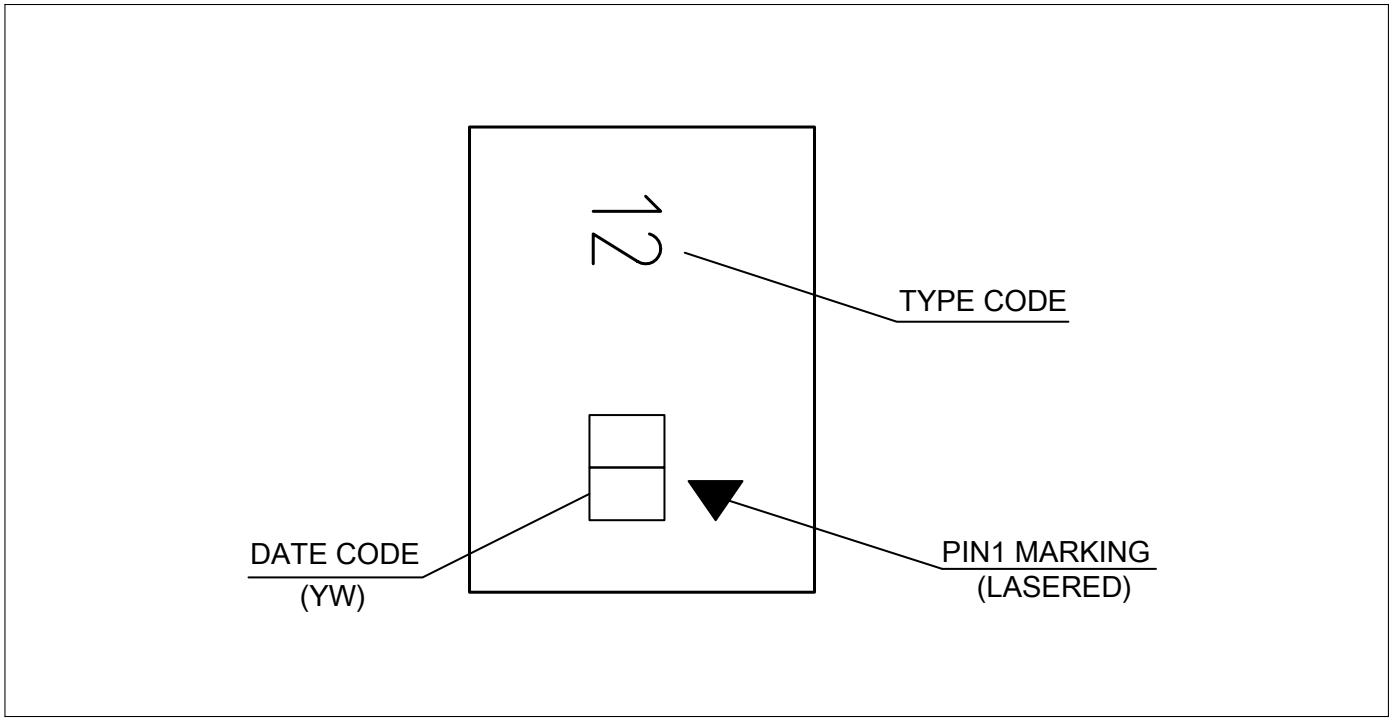


Figure 5: Laser marking

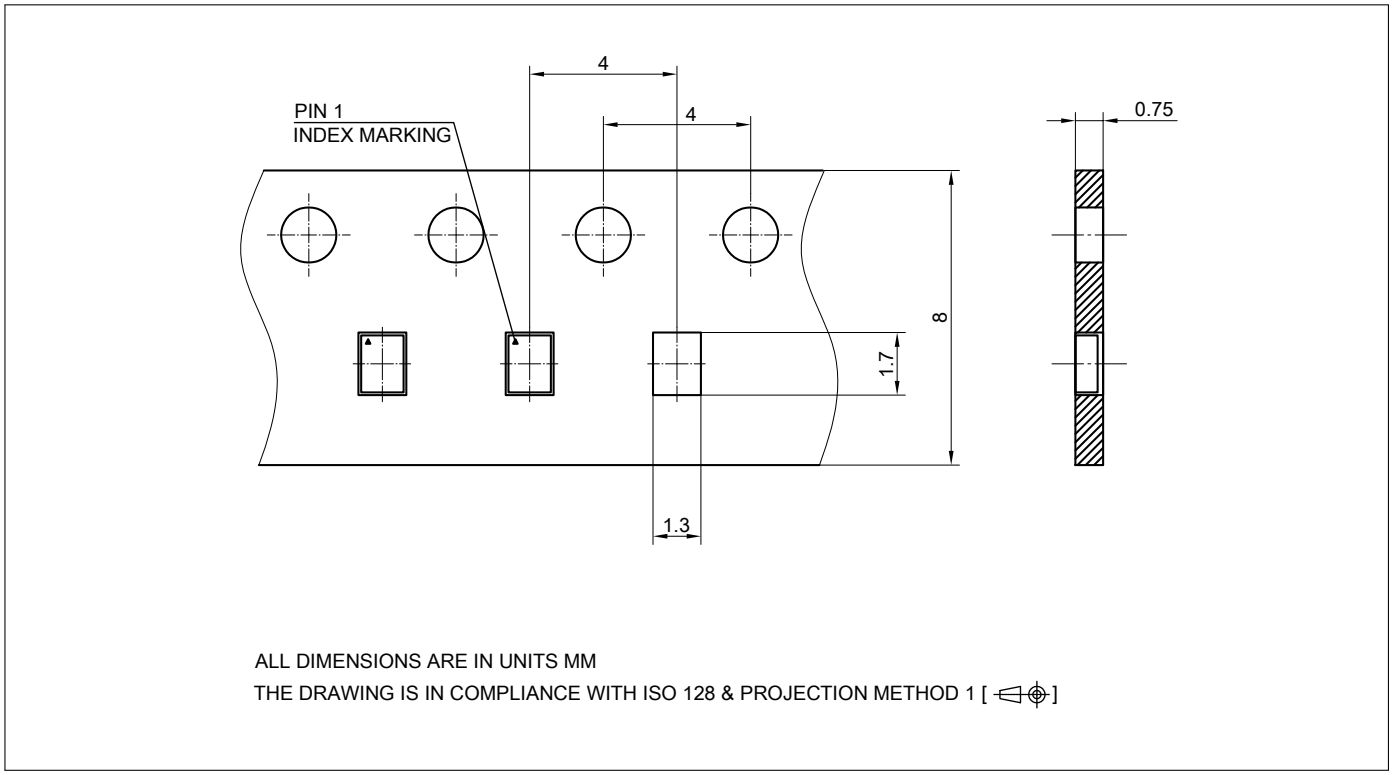


Figure 6: Carrier Tape

Table 17: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 18: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
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1	´NDA Required´ removed

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