



CAN BUS ESD PROTECTION DIODE

Product Summary

V _{BR(MIN)}	I _{PP(MAX)}	C _{T(TYP)}
36V & 13.3V	4A & 11A	32pF

Features

- 240W & 330W Peak Power Dissipation per Line (8/20µs Waveform)
- Provides ESD Protection per IEC 61000-4-2 Standard: Air ±30kV, Contact ±30kV
- 2 Channels of ESD Protection
- Low Channel Input Capacitance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Description and Applications

This DESD3512SO is a next generation ESD and surge protection device packaged in a small footprint surface mount package. It is qualified to AEC-Q101, supported by a PPAP and is designed to protect two data lines of the Controller Area Network (CAN) in an automotive.

- CAN Bus Protection
- Industrial Control Network

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208@3
- Weight: 0.009 grams (Approximate)

SOT23



Bottom View



Device Schematic

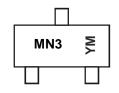
Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DESD3512SO-7	Commercial	MN3	7	8	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



MN3 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: E = 2017) M = Month (ex: 9 = September)

Date Code Key

	Year	201	4	2015		2016	20	17	2018		2019	2	2020
	Code	В		С		D		E	F		G		Н
Ī	Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ſ	Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Condition
Peak Pulse Power Dissipation	P _{PP}	240 & 330	W	8/20µs, per Figure 3
Peak Pulse Current	I _{PP}	4 & 11	Α	8/20µs, per Figure 3
ESD Protection – Contact Discharge	V _{ESD_} CONTACT	±30	kV	IEC61000-4-2 Standard
ESD Protection – Air Discharge	V _{ESD_AIR}	±30	kV	IEC61000-4-2 Standard

Thermal Characteristics

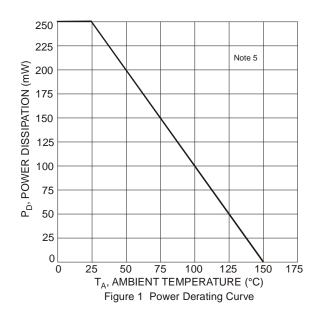
Characteristic	Symbol	Value	Unit
Package Power Dissipation (Note 5)	P_{D}	300	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ hetaJA}$	417	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

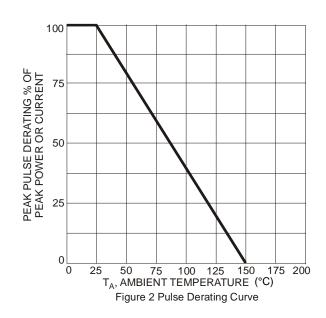
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
Reverse Standoff Voltage, from Pin 1 or Pin 2 to Pin 3	V _{RWM1}	-	-	35	V	-
Reverse Standoff Voltage, from Pin 3 to Pin 1 or Pin 2	V _{RWM2}	-	-	12	V	-
Channel Leakage Current, from Pin 1 or Pin 2 to Pin 3 (Note 6)	I _{RM1}	1	-	500	nA	V _{RWM} = 35V
Channel Leakage Current, from Pin 3 to Pin 1 or Pin 2 (Note 6)	I _{RM2}	-	-	500	nA	V _{RWM} = 12V
Breakdown Voltage, from Pin 1 or Pin 2 to Pin 3	V_{BR1}	36	-	-	V	$I_R = 1mA$
Breakdown Voltage, from Pin 3 to Pin 1 or Pin 2	V_{BR2}	13.3	-	-	V	$I_R = 1mA$
Clamping Voltage, from Pin 1 or Pin 2 to Pin 3	V _{CL1}	1	-	53	V	$I_{PP} = 1A$, $t_P = 8/20 \mu S$
Clamping Vollage, Ironi Pili i oi Pili 2 to Pili 3		-	-	60	V	$I_{PP} = 4A$, $t_P = 8/20 \mu S$
Clamping Voltage, from Pin 3 to Pin 1 or Pin 2	V _{CL2}	-	-	20	V	$I_{PP} = 1A$, $t_P = 8/20 \mu S$
Clamping Vollage, Ironi Pili 3 to Pili 1 of Pili 2		1	-	30	V	$I_{PP} = 11A$, $t_P = 8/20 \mu S$
Channel Input Capacitance	C_{T}	-	32	-	pF	$V_R = 0V$, $f = 1MHz$

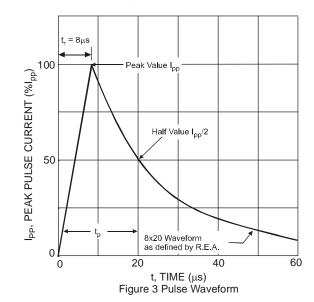
Notes:

- 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.
- 6. Short duration pulse test used to minimize self-heating effect.









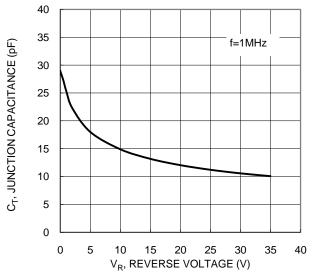
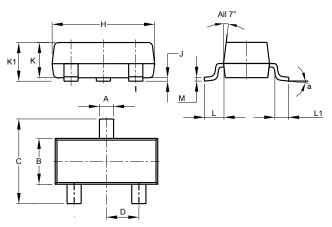


Figure 4: Typical Junction Capacitance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23



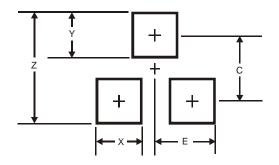
SOT23								
Dim	Min	Max	Тур					
Α	0.37	0.51	0.40					
В	1.20	1.40	1.30					
С	2.30	2.50	2.40					
D	0.89	1.03	0.915					
F	0.45	0.60	0.535					
G	1.78	2.05	1.83					
Н	2.80	3.00	2.90					
J	0.013	0.10	0.05					
K	0.890	1.00	0.975					
K1	0.903	1.10	1.025					
L	0.45	0.61	0.55					
L1	0.25	0.55	0.40					
M	0.085	0.150	0.110					
а		8°						
All	All Dimensions in mm							



Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Y	0.9
С	2.0
E	1.35

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