STB30N80K5



N-channel 800 V, 0.15 Ω typ., 24 A, MDmesh™ K5 Power MOSFET in a D²PAK package

Datasheet - production data

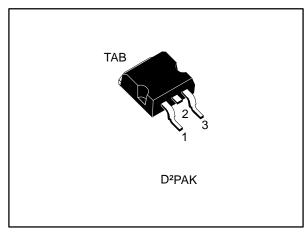
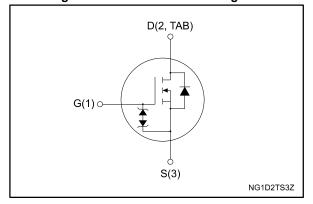


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} R _{DS(on)} max.		ΙD
STB30N80K5	800 V	0.18 Ω	24 A

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

• Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STB30N80K5	30N80K5	D²PAK	Tape and reel

Contents STB30N80K5

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STB30N80K5 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	800	V
V_{GS}	Gate-source voltage	±30	V
ID	Drain current (continuous) at T _C = 25 °C	24	Α
ID	Drain current (continuous) at T _C = 100 °C	15	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	96	Α
Ртот	Total dissipation at T _C = 25 °C	250	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
T _{stg}	Storage temperature range	55 to 150	°C
Tj	Operating junction temperature range	- 55 to 150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30	°C/W

Notes:

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax} .)	8	А
Eas	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	440	mJ

 $[\]ensuremath{^{(1)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(2)}}I_{SD}{<}~24$ A, di/dt ${<}~100$ A/ μ s, VDSpeak ${<}~V$ (BR)DSS, VDD= 80% V(BR)DSS

⁽³⁾V_{DS}= 640 V

 $^{^{(1)}}$ When mounted on FR-4 board of 1 inch², 2 oz Cu

Electrical characteristics STB30N80K5

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	800			V
	Zero gate voltage	V _G S= 0 V, V _D S = 800 V			1	μΑ
I _{DSS}	drain current	V _{GS} = 0 V, V _{DS} = 800 V, T _C = 125 °C ⁽¹⁾			50	μΑ
Igss	Gate source leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±10	μΑ
$V_{GS(th)}$	Gate threshold voltage	$V_{DD} = V_{GS}$, $I_D = 100 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 12 A		0.15	0.18	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	1530	-	pF
Coss	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$	-	145	-	pF
Crss	Reverse transfer capacitance	V _{GS} = 0 V	-	1.2	-	pF
C _{o(er)} ⁽¹⁾	Equivalent capacitance energy related	V _{GS} = 0 V,	-	91	-	pF
C _{o(tr)} ⁽²⁾	Equivalent capacitance time related	$V_{DS} = 0 \text{ to } 640 \text{ V}$	-	244	-	pF
Qg	Total gate charge	$V_{DD} = 640 \text{ V}, I_D = 24 \text{ A},$	-	43	-	nC
Qgs	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	12.8	-	nC
Q _{gd}	Gate-drain charge	(see Figure 16: "Test circuit for gate charge behavior")	-	24.2	-	nC
Rg	Gate input resistance	f =1 MHz, I _D = 0 A	-	3.5	-	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

 $^{^{(1)}}$ Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

 $^{^{(2)}}$ Time related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DS} = 400 \text{ V}, I_{D} = 12 \text{ A},$	-	21	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$	-	15	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 15: "Test circuit for	-	100	1	ns
t _f	Fall time	resistive load switching times")	-	13.5	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		ı		24	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		ı		96	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 24 A, V _{GS} = 0 V	ı		1.5	V
t _{rr}	Reverse recovery time	$I_{SD} = 24 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	ı	555		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	9.95		μC
I _{RRM}	Reverse recovery current	(see Figure 17: "Test circuit for inductive load switching and diode recovery times")	1	36		А
t _{rr}	Reverse recovery time	I _{SD} = 24 A, di/dt = 100 A/µs	-	765		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 ^{\circ}\text{C}$		13.2		μC
I _{RRM}	Reverse recovery current	(see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	34.5		А

Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)GSO} \\$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	•	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

⁽¹⁾Pulse width limited by safe operating area.

 $^{^{(2)}}$ Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area (A) Operation in this area is limited by R_{DS(on)} GIPG091215VK8LBSOA 104 t =10 µs 10¹ t =100 µs t =1 ms t =10 ms 10⁰ T_,≤150 °C 10-T_o= 25°C single pulse 10^{-2} 10° 10¹

Figure 3: Thermal impedance

K

0.2

0.1

0.05

0.02

Z_{th}= K*R_{thj-c}

0= t_p/T

Single pulse

10⁻²

10⁻³

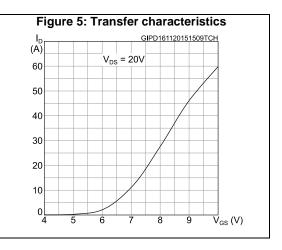
10⁻¹

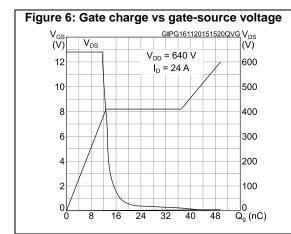
10⁻¹

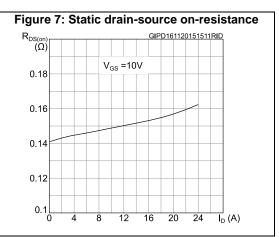
10⁻²

10⁻¹

t_p(s)







STB30N80K5 Electrical characteristics

Figure 8: Capacitance variations C (pF) GIPD161120151510CVR 10⁴ C_{ISS} 10³ 10² Coss f= 1MHz 10¹ C_{RSS} 10⁰ 10⁻¹ $\overline{V}_{DS}(V)$ 10⁻¹ 10¹

Figure 10: Normalized on-resistance vs temperature

R_{DS(on)} GIPD161120151514RON
(norm.)

2.6

2.2

1.8

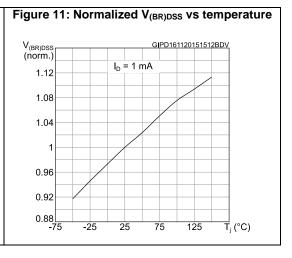
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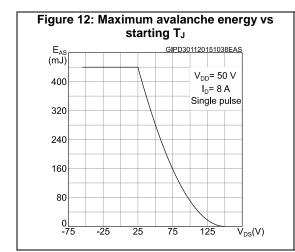
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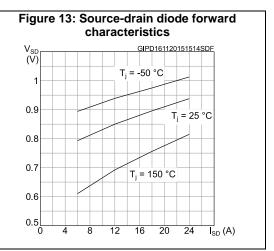
0.6

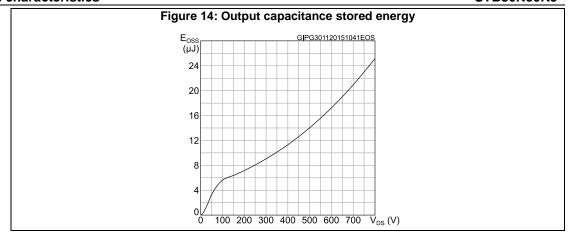
0.2

-75
-25
25
75
125
T_j (°C)









STB30N80K5 Test circuits

3 Test circuits

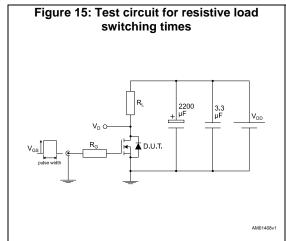


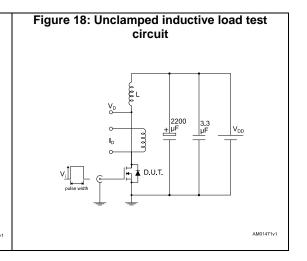
Figure 16: Test circuit for gate charge behavior

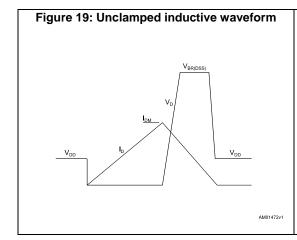
12 V 47 kΩ 100 nF D.U.T.

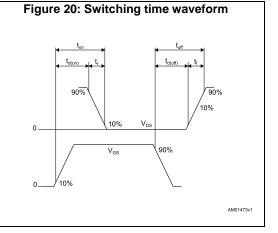
2200 PF 47 kΩ OVG

AM01466y1

Figure 17: Test circuit for inductive load switching and diode recovery times







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 21: D²PAK (TO-263) type A package outline E1 c2-L1 THERMAL PAD SEATING PLANE COPLANARITY A 1 0.25 GAUGE PLANE

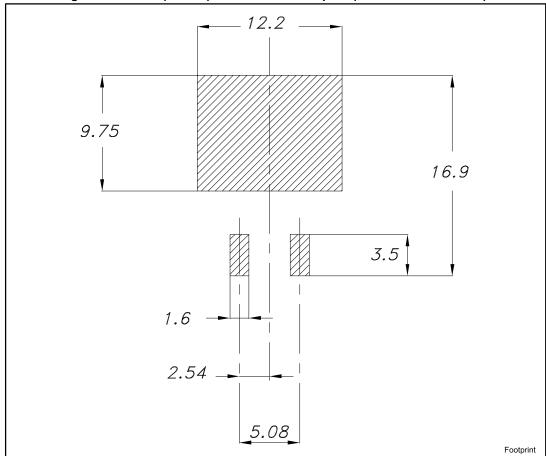
0079457_A_rev22

V2_

Table 10: D²PAK (TO-263) type A package mechanical data

Dim	mm			
Dim.	Min.	Тур.	Max.	
А	4.40		4.60	
A1	0.03		0.23	
b	0.70		0.93	
b2	1.14		1.70	
С	0.45		0.60	
c2	1.23		1.36	
D	8.95		9.35	
D1	7.50	7.75	8.00	
D2	1.10	1.30	1.50	
Е	10		10.40	
E1	8.50	8.70	8.90	
E2	6.85	7.05	7.25	
е		2.54		
e1	4.88		5.28	
Н	15		15.85	
J1	2.49		2.69	
L	2.29		2.79	
L1	1.27		1.40	
L2	1.30		1.75	
R		0.4		
V2	0°		8°	

Figure 22: D²PAK (TO-263) recommended footprint (dimensions are in mm)



STB30N80K5 Package information

D²PAK packaging information 4.2

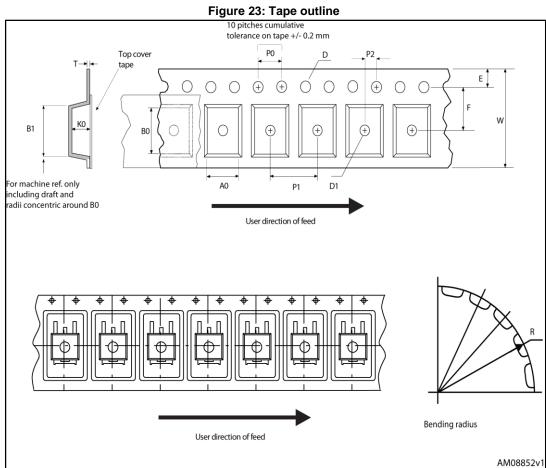


Figure 24: Reel outline

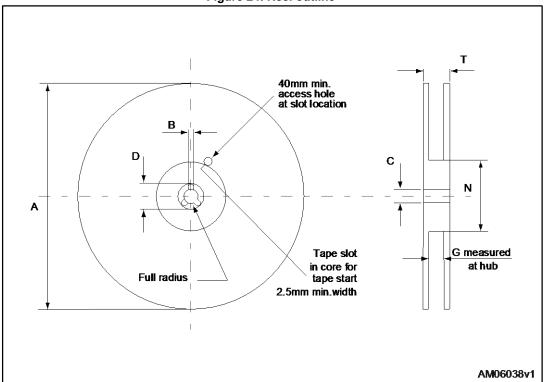


Table 11: D2PAK tape and reel mechanical data

	Tape		Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.	Diiii.	Min.	Max.
A0	10.5	10.7	А		330
В0	15.7	15.9	В	1.5	
D	1.5	1.6	С	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	Т		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity 1000		1000
P2	1.9	2.1	Bulk quantity 1000		1000
R	50				
Т	0.25	0.35			
W	23.7	24.3			

STB30N80K5 Revision history

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
14-Dec-2015	1 First release.	
	2	Modified: features in cover page.
06-Jul-2016		Added: note in Table 5: "On/off states".
00-301-2010		Modified: Figure 3: "Thermal impedance".
		Minor text changes.

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