ACS37003KMC

400 kHz Current Sensor IC with High Accuracy in Low-Resistance High-Isolation Package

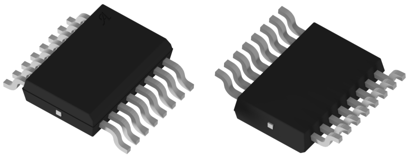
FEATURES AND BENEFITS

- Low internal primary conductor resistance (265 µΩ) for better power efficiency and low dissipation
- High operating bandwidth for fast control loops or where high-speed currents are monitored
  - 400 kHz bandwidth
  - 1.1 µs typical response time
- High accuracy
  - As low as 1% maximum sensitivity error over temperature
  - 8 mV maximum offset voltage over temperature
  - Non-ratiometric operation with V_{REF} output
  - Differential sensing robust against external magnetic fields
  - No magnetic hysteresis
- UL-certified to 62368-1, highly isolated compact SOIC16W surface mount package
  - 5 kV_{RMS} rated isolation test voltage
  - 1144 V_{RMS} / 1618 V_{DC} basic isolation voltages
  - 572 V_{RMS} / 809 V_{DC} reinforced isolation voltages
- Wide operating temperature, –40°C to 125°C
- Maximum 70 A_{RMS} continuous operating current at 85°C

PACKAGE:

16-pin SOICW
(suffix MC)

Not to scale



DESCRIPTION

The ACS37003 is a fully integrated current sensor IC that senses current flowing through the custom SOICW16 package. The current conductor has a very low (265 µΩ) resistance, ideal for low power dissipation. The sensor is factory-trimmed to provide high accuracy over the entire operating range without the need for customer programming or calibration.

The internal construction provides high isolation by magnetically coupling the field generated by current flow in the conductor to the fully monolithic Hall sensor IC. The current is sensed differentially by two Hall plates that subtract out interfering common-mode magnetic fields. The IC has no physical connection to the integrated current conductor and provides 5 kV_{RMS} isolation between the primary and secondary signal leads of the package. This high rating provides an industry-leading basic working voltage of 1140 V_{RMS} and a reinforced working voltage of 572 V_{RMS}.

The ACS37003KMC is provided in a custom SOICW16 surface mount package. The pin pitch is the same as a standard SOIC16, but the lead-frame is 2.5 times as thick to reduce the resistance. The package body is sized to achieve greater than 8.2 mm of creepage and clearance. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, making the device RoHS compliant.

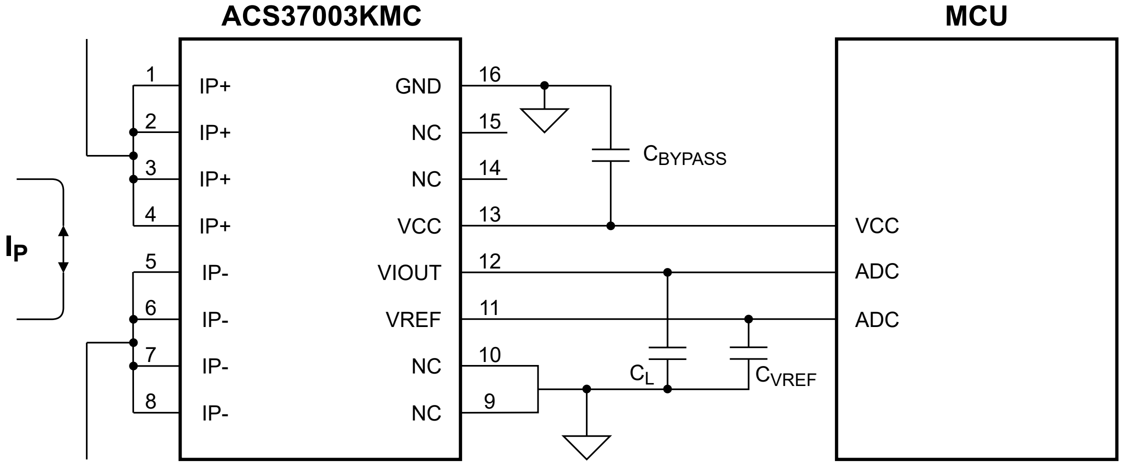
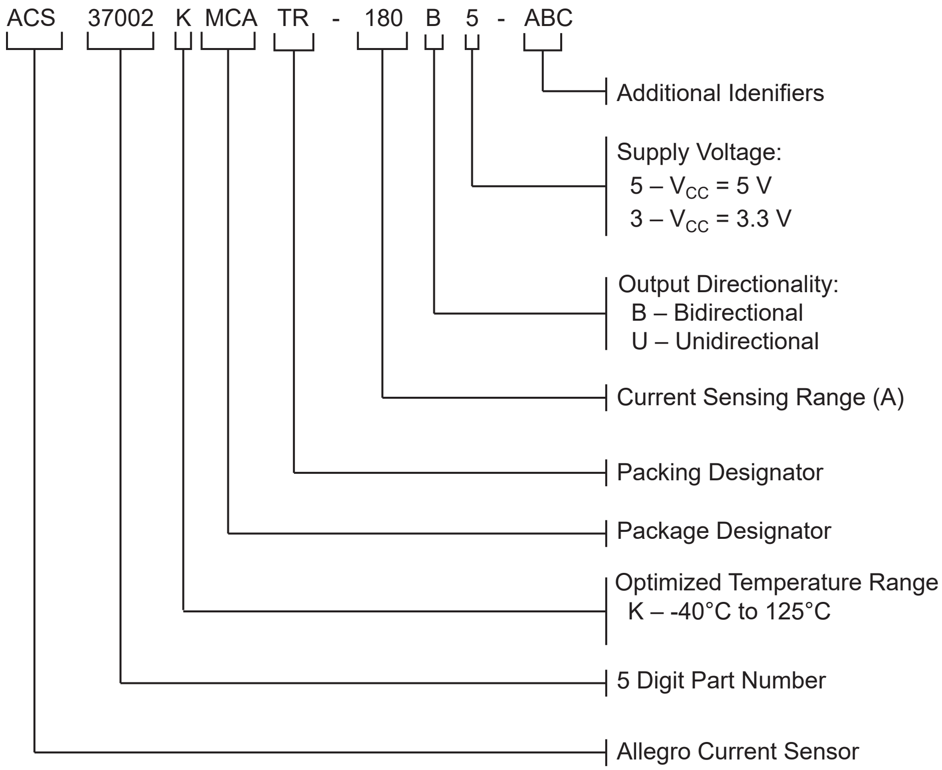


Figure 1: Typical Application Circuit

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity (mV/A)	V_{CC} (V)	$V_{IOUT(Q)}$ (V)	Temp. Range T_A (°C)	Package	Packing [1]
ACS37003KMCATR-120B3	±120	12	3.3	1.65	–40 to 125	16-pin SOIC	1000 pieces per 13-inch reel
ACS37003KMCATR-050B5	±50	40	5	2.5			
ACS37003KMCATR-85B5	±85	25					
ACS37003KMCATR-180B5	±180	12					

[1] Contact Allegro for additional options.



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6.5	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Forward Output Voltage	V_{FOUT}	Applies to V_{IOUT} and V_{REF}	$(V_{CC} + 0.7) \leq 6.5$	V
Reverse Output Voltage	V_{ROUT}	Applies to V_{IOUT} and V_{REF}	–0.5	V
Forward Input Voltage	V_{FNC}	Applies to NC pins	$(V_{CC} + 0.7) \leq 6.5$	V
Reverse Input Voltage	V_{RNC}	Applies to NC pins	–0.5	V
Maximum Continuous Current [1]	I_{CMAX}	T_A = 25°C	100	A
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

[1] Tested on the ASEK37003-Panel Evaluation Board (TED-0003314)

ISOLATION AND PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage	V_{ISO}	Agency type-tested for 60 seconds per UL 60950-1 (edition 2) and 62368-1 (edition 1). Production tested at 3125 V_{RMS} for 1 second in accordance with UL 60950-1 (edition 2) and 62368-1 (edition 1).	5000	V_{RMS}
Working Voltage for Basic Isolation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2) and 62368-1 (edition 1).	1618	V_{PK} or V_{DC}
			1144	V_{RMS}
Working Voltage for Reinforced Isolation	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 60950-1 (edition 2) and 62368-1 (edition 1).	809	V_{PK} or V_{DC}
			572	V_{RMS}
Clearance	D_{cl}	Minimum distance through air from IP leads to signal leads	8.2	mm
Creepage	D_{cr}	Minimum distance along package body from IP leads to signal leads	8.2	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	70	µm
Comparative Track Index	CTI	Material Group II	400 to 599	V
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	3	–

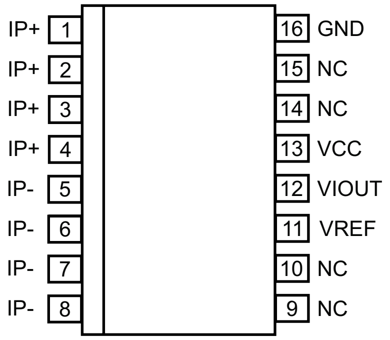


Figure 2: MC Package Pinout Diagram

Terminal List Table

Number	Name	Description
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally
5, 6, 7, 8	IP-	Terminals for current being sensed; fused internally
9	NC	Terminal can be left open or grounded
10	NC	Terminal can be left open or grounded
11	VREF	Zero current voltage reference
12	VIOUT	Analog output representing the current flowing through I_P
13	VCC	Device power supply terminal
14	NC	Terminal can be left open or grounded
15	NC	Terminal can be left open or grounded
16	GND	Device ground terminal

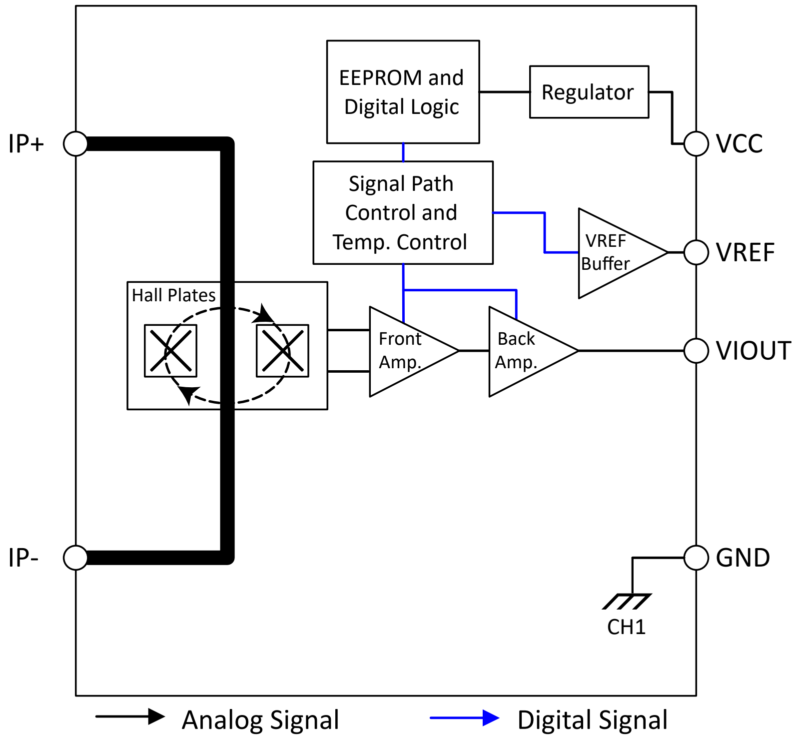


Figure 3: Functional Block Diagram

COMMON ELECTRICAL CHARACTERISTICS: **Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V or 5 V, unless otherwise specified**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	V_{CC} = 5 V	4.5	5	5.5	V
		V_{CC} = 3.3 V	3.15	3.3	3.6	V
Supply Current	I_{CC}	V_{CC} = 5 V; no load on VIOUT or VREF	–	15	18	mA
		V_{CC} = 3.3 V; no load on VIOUT or VREF	–	12	15	mA
Supply Bypass Capacitor	C_{BYPASS}	VCC to GND	0.1	–	–	µF
Primary Conductor Resistance	R_{IP}	T_A = 25°C	–	265	–	µΩ
Primary Conductor Inductance	L_{IP}		–	4.45	–	nH
Output Buffer Resistance	R_{OUT}	Internal output buffer resistance on VIOUT and VREF	–	4	–	Ω
Magnetic Coupling	B		–	4.55	–	G/A
Power-On Reset Voltage	$V_{POR(H)}$	V_{CC} rising [1]	2.6	2.9	3.1	V
	$V_{POR(L)}$	V_{CC} falling [1]	2.2	2.5	2.8	V
POR Hysteresis	$V_{POR(HYS)}$		250	–	–	mV
Power-On Time	t_{POD}	Time from V_{CC} rising ≥ $V_{POR(H)}$ after a POR event until power-on	–	100	–	µs
Overvoltage Detection (OVD) Threshold	$V_{OVD(H)}$	V_{CC} rising [1]	6.1	6.4	6.8	V
	$V_{OVD(L)}$	V_{CC} falling [1]	5.6	5.8	6.1	V
OVD Hysteresis	$V_{OVD(HYS)}$		–	660	–	mV
OVD Delay Time	$t_{dOVD(EN)}$	Time from V_{CC} rising ≥ $V_{OVD(EN)}$ until OVD asserts	60	64	120	µs
	$t_{dOVD(DIS)}$	Time from V_{CC} falling ≤ $V_{OVD(DIS)}$ until OVD clears	–	7	–	µs

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COMMON ELECTRICAL CHARACTERISTICS (continued): Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V or 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
OUTPUT SIGNAL CHARACTERISTICS (VIOUT)						
Output Resistive Load	R_L	VIOUT to GND, VIOUT to VCC	10	–	–	kΩ
Output Capacitive Load	C_L	VIOUT to GND	–	1	6	nF
Saturation Voltage	$V_{SAT(H)}$	R_L = 10 kΩ to GND	V_{CC} – 0.25	–	–	V
	$V_{SAT(L)}$	R_L = 10 kΩ to VCC	–	–	0.15	V
Output Current Limit	$I_{OUT(src)}$	VIOUT shorted to GND	–	25	–	mA
	$I_{OUT(snk)}$	VIOUT shorted to VCC	–	25	–	mA
Internal Bandwidth	BW	Small signal –3 dB, C_L = 5.7 nF	–	400	–	kHz
Rise Time	t_r	T_A = 25°C, C_L = 5.7 nF	–	0.7	–	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 5.7 nF	–	1.1	–	µs
Propagation Delay	t_{pd}	T_A = 25°C, C_L = 5.7 nF	–	0.7	–	µs
Noise Density	I_{ND}	Input-referenced noise density; T_A = 25°C, C_L = 5.7 nF; V_{CC} = 5 V	–	350	–	µA/√Hz
		Input-referenced noise density; T_A = 25°C, C_L = 5.7 nF; V_{CC} = 3.3 V	–	450	–	µA/√Hz
Noise	I_N	BW = 400 kHz; T_A = 25°C, C_L = 5.7 nF; V_{CC} = 5 V	–	277	–	mA
		BW = 400 kHz; T_A = 25°C, C_L = 5.7 nF; V_{CC} = 3.3 V	–	357	–	mA
Nonlinearity	E_{LIN}	Comparison of $I_P = I_{P(MAX)} \leq 65A$ and $I_P = I_{P(MAX)}/2 \leq 32.5$ A	–	±0.5	–	%
Power Supply Rejection Ratio Offset	$PSRR_O$	DC to 1 kHz; 100 mV pk-pk ripple on V_{CC}, I_P = 0 A, change in V_{OE} relative to $V_{CC,}$ T_A = 25°C	–	–40	–	dB
		1 to 100 kHz; 100 mV pk-pk ripple on V_{CC}, I_P = 0 A, change in V_{OE} relative to $V_{CC,}$ T_A = 25°C	–	–30	–	dB
Power Supply Rejection Ratio Sens	$PSRR_S$	DC to 1kHz; 100 mV pk-pk ripple on V_{CC}, I_P = 0 A, change in E_{SENS} relative to $V_{CC,}$ T_A = 25°C	–	–15	–	dB
		1 to 100 kHz; 100 mV pk-pk ripple on V_{CC}, I_P = 0 A, change in E_{SENS} relative to $V_{CC,}$ T_A = 25°C	–	–6	–	dB
Power Supply Offset Error	$V_{OE(PS)}$	Additional V_{OE} at $V_{CC} = V_{CC(min)}$ or $V_{CC(max)}$ from V_{OE} at $V_{CC,}$ T_A = 25°C	–15	±1	15	mV
Power Supply Sensitivity Error	$E_{SENS(PS)}$	Additional E_{SENS} at $V_{CC} = V_{CC(min)}$ or $V_{CC(max)}$ from E_{SENS} at $V_{CC,}$ T_A = 25°C	–1.5	±0.3	1.5	%
Common-Mode Field Rejection	CMFR	Input-referred error due to a common-mode field	–	4	–	mA/G

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COMMON ELECTRICAL CHARACTERISTICS (continued): Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V or 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
REFERENCE OUTPUT CHARACTERISTICS (VREF)						
Zero Current Reference Voltage	V_{REF}	Bidirectional; V_{CC} = 5 V	2.49	2.5	2.51	V
		Bidirectional; V_{CC} = 3.3 V	1.64	1.65	1.66	V
		Unidirectional; V_{CC} = 5 V	0.49	0.5	0.51	V
		Unidirectional; V_{CC} = 3.3 V	0.32	0.33	0.34	V
Reference Resistive Load	R_{VREF}	VREF to GND; VREF to VCC	10	–	–	kΩ
Reference Capacitive Load	C_{VREF}	VREF to GND	–	–	6	nF
Reference Source Current Limit	$I_{REF(SRC)}$	Max. current VREF can passively source	–	25	–	mA
	$I_{REF(SNK)}$	Max. current VREF can passively sink	–	–25	–	mA

[1] V_{CC} rate +1 V/ms, for best accuracy.

ACS37003KMCATR-120B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ. [1]	Max.[1]	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–120	–	120	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	12	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Ideal Voltage of V_{REF} and $V_{IOUT(Q)}$	–	1.65	–	V
TOTAL ERROR ($V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)} \times I_{PR} + V_{REF}$)) / ($Sens_{(IDEAL)} \times I_{PR}$) × 100 AND TOTAL ERROR COMPONENTS						
Total Error	E_{TOT}	Measured at I_P = ±65 A, T_A = 25°C	–0.9	–	0.9	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.1	–	1.1	%
Sensitivity Error	E_{SENS}	Measured at I_P = ±65 A, T_A = 25°C	–0.9	–	0.9	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.1	–	1.1	%
Reference Error	V_{RE}	$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV
Offset Error	V_{OE}	$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = 25°C	–5	–	5	mV
		$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = –40°C to 125°C	–5	–	5	mV
QVO Error	V_{QE}	$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

ACS37003KMCATR-050B5 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ. [1]	Max.[1]	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–50	–	50	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	40	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Ideal Voltage of V_{REF} and $V_{IOUT(Q)}$	–	2.5	–	V
TOTAL ERROR ($V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)} \times I_{PR} + V_{REF}$)) / ($Sens_{(IDEAL)} \times I_{PR}$) × 100 AND TOTAL ERROR COMPONENTS						
Total Error	E_{TOT}	Measured at $I_P = \pm I_{PR(max)}$, T_A = 25°C	–0.7	–	0.7	%
		Measured at $I_P = \pm I_{PR(max)}$, T_A = –40°C to 125°C	–1.3	–	1.3	%
Sensitivity Error	E_{SENS}	Measured at $I_P = \pm I_{PR(max)}$, T_A = 25°C	–0.7	–	0.7	%
		Measured at $I_P = \pm I_{PR(max)}$, T_A = –40°C to 125°C	–1.3	–	1.3	%
Reference Error	V_{RE}	$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV
Offset Error	V_{OE}	$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = 25°C	–5	–	5	mV
		$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = –40°C to 125°C	–5	–	5	mV
QVO Error	V_{QE}	$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

ACS37003KMCATR-085B5 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ. [1]	Max.[1]	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–85	–	85	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	25	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Ideal Voltage of V_{REF} and $V_{IOUT(Q)}$	–	2.5	–	V
TOTAL ERROR ($V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)} \times I_{PR} + V_{REF}$)) / ($Sens_{(IDEAL)} \times I_{PR}$) × 100 AND TOTAL ERROR COMPONENTS						
Total Error	E_{TOT}	Measured at I_P = ±65 A, T_A = 25°C	–0.9	–	0.9	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.3	–	1.3	%
Sensitivity Error	E_{SENS}	Measured at I_P = ±65 A, T_A = 25°C	–0.9	–	0.9	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.3	–	1.3	%
Reference Error	V_{RE}	$V_{REFactual} – V_{REFideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{REFactual} – V_{REFideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV
Offset Error	V_{OE}	$V_{IOUT(Q)} – V_{REF}$, I_P = 0 A, T_A = 25°C	–5	–	5	mV
		$V_{IOUT(Q)} – V_{REF}$, I_P = 0 A, T_A = –40°C to 125°C	–5	–	5	mV
QVO Error	V_{QE}	$V_{IOUT(Q)} – V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{IOUT(Q)} – V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV

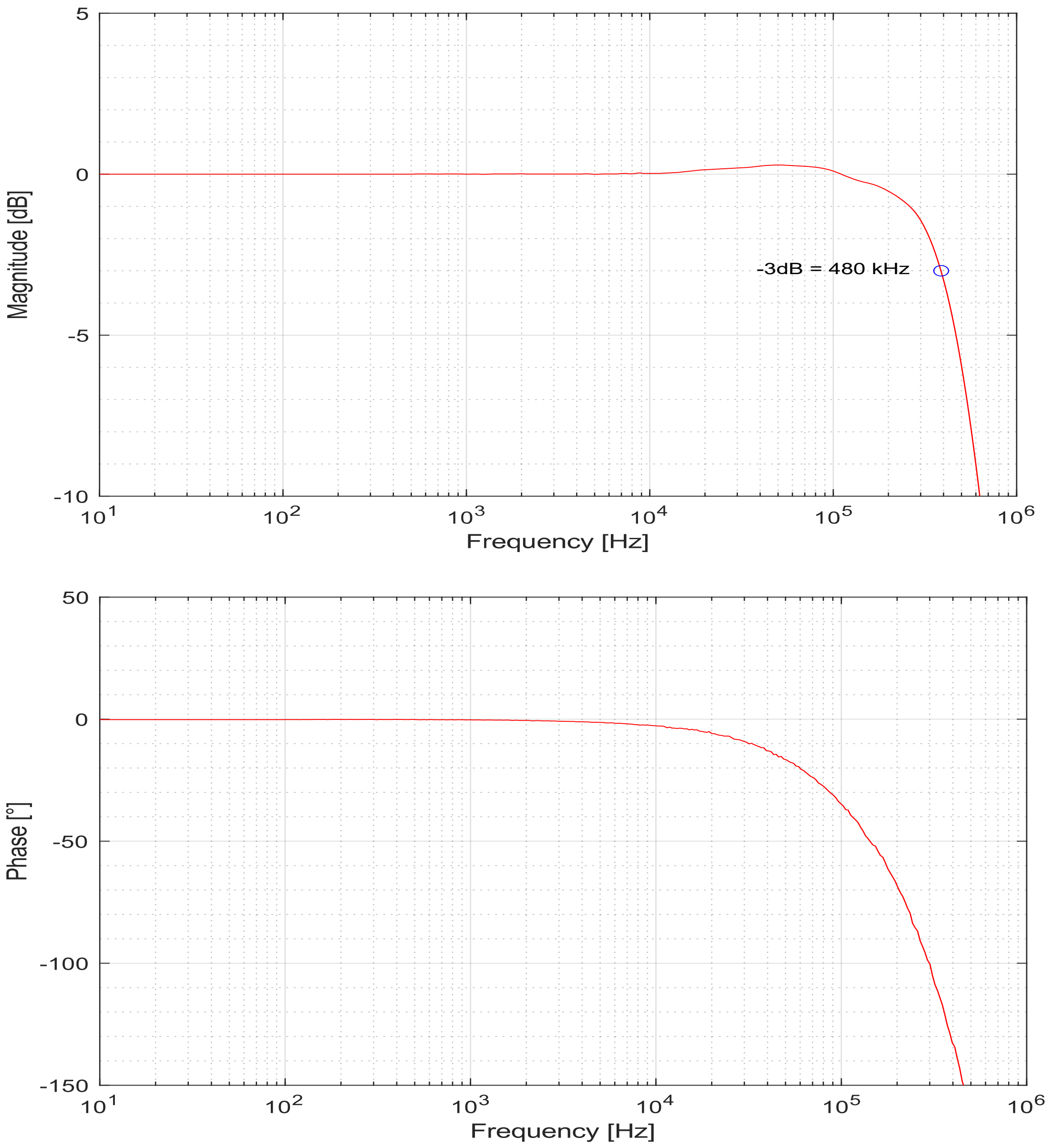
[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

ACS37003KMCATR-180B5 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ. [1]	Max.[1]	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–180	–	180	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	12	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Ideal Voltage of V_{REF} and $V_{IOUT(Q)}$	–	2.5	–	V
TOTAL ERROR ($V_{IOUT(ACTUAL)}$ – ($Sens_{(IDEAL)} \times I_{PR} + V_{REF}$)) / ($Sens_{(IDEAL)} \times I_{PR}$) × 100 AND TOTAL ERROR COMPONENTS						
Total Error	E_{TOT}	Measured at I_P = ±65 A, T_A = 25°C	–0.8	–	0.8	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.1	–	1.1	%
Sensitivity Error	E_{SENS}	Measured at I_P = ±65 A, T_A = 25°C	–0.8	–	0.8	%
		Measured at I_P = ±65 A, T_A = –40°C to 125°C	–1.2	–	1.2	%
Reference Error	V_{RE}	$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{REFactual} - V_{REFideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV
Offset Error	V_{OE}	$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = 25°C	–5	–	5	mV
		$V_{IOUT(Q)} - V_{REF}$, I_P = 0 A, T_A = –40°C to 125°C	–5	–	5	mV
QVO Error	V_{QE}	$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = 25°C	–10	–	10	mV
		$V_{IOUT(Q)} - V_{IOUT(Q)ideal}$, I_P = 0 A, T_A = –40°C to 125°C	–10	–	10	mV

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

CHARACTERISTIC PERFORMANCE
ACS37003 TYPICAL FREQUENCY RESPONSE



For information regarding bandwidth characterization methods used for the ACS37003, see the "Characterizing System Bandwidth" application note (https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an-effective-method-for-characterizing-system-bandwidth-an296169) on the Allegro website.

FUNCTIONAL DESCRIPTION

Power-On Reset Operation

The provided graphs in this section show V_{IOUT} moving with V_{CC}. The voltage of V_{IOUT} during a high-impedance state will be most consistent with a known load (R_L,C_L). Figure 4, Figure 5, and Figure 6 all use the same labeling scheme for different power thresholds. References in brackets "[ ]" are valid for each of these plots.

POWER-ON/POWER-OFF

As V_{CC} ramps up, the V_{IOUT} and V_{REF} outputs are high impedance until V_{CC} reaches and passes $V_{POR(H)}$ [1] in Figure 4. V_{REF} and V_{IOUT} will continue to report until V_{CC} is less than $V_{POR(L)}$ [5] in Figure 4, at which point they will go high Z. Note that the time it takes the output to reach a steady state will depend on the external circuitry used.

POWER-ON DELAY (t_{POD})

When the supply is ramped to $V_{POR(H)}$ [2] in Figure 4, the device will require a finite time to power its internal components before the outputs are released from high Z and can respond to an input magnetic field. Power-On Time, t_{POD}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, which can be seen as the time from [1] to [A] in Figure 5. After this delay, the output will quickly approach $V_{IOUT(IP)} = \text{Sens} \times \text{IP} + V_{REF}$.

Overvoltage Detection (OVD)

To ensure that the device output is reporting accurately, the device contains an overvoltage flag. This flag on V_{IOUT} can be used to alert the system that the supply voltage is outside of the operational limits. When V_{CC} raises above $V_{OVD(H)}$ [3] in Figure 4, V_{IOUT} will go high Z and be pulled by the load resistor to V_{CC} or GND. V_{REF} continues to output normally.

There is hysteresis between OVD enable and disable thresholds to reducing nuisance flagging and clears. There is approximately 1 V of hysteresis seen between [3] and [4] in Figure 4.

The enable time for OVD, $t_{OVD(E)}$, is the time from $V_{OVD(H)}$ [4] to OVD flag [B] in Figure 6. The enable flag for OVD has a counter to reduce transients faster than 64 µs from triggering nuisance flags. The disable time for OVD, $t_{OVD(D)}$, is the time from $V_{OVD(L)}$ [5] until the device returns to normal operation [C] in Figure 6. The OVD disable time does not have a counter.

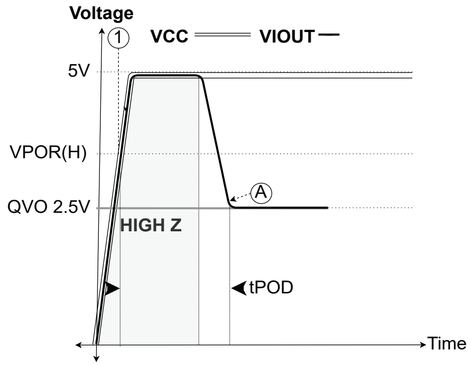


Figure 5: t_{POD}, R_L = Pull-Up

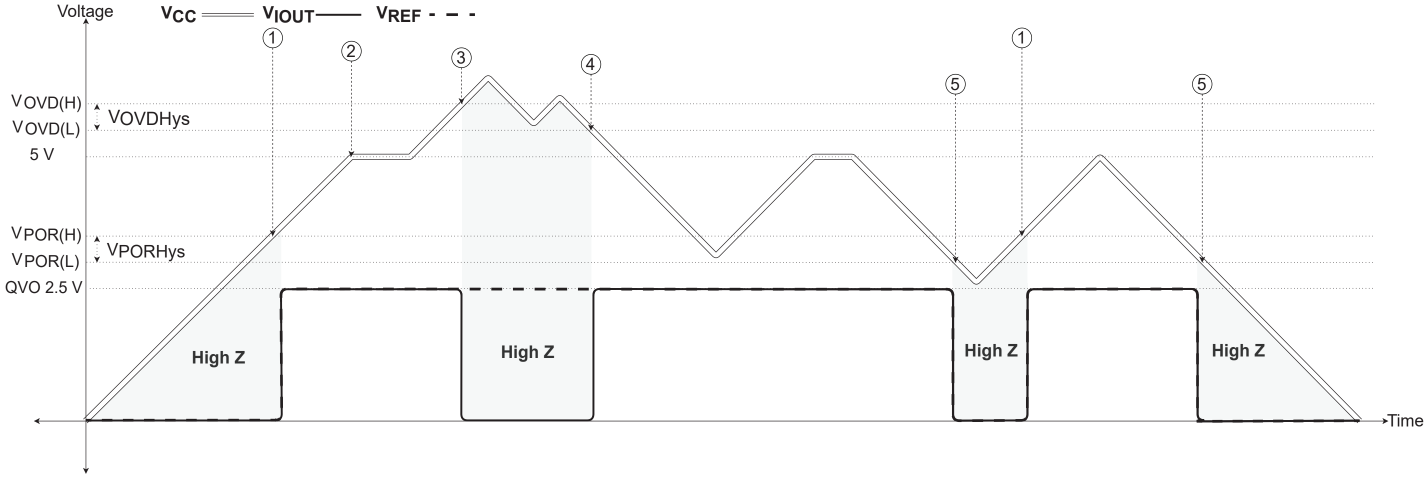


Figure 4: Power States Thresholds with V_{IOUT} Behavior for a 5 V Device, R_L = Pull-Down

Absolute Maximum Ratings

These are the maximum application or environmental conditions that the device can be subjected before damage may occur.

SUPPLY ZENER CLAMP VOLTAGES

If the voltage applied to the device continues to increase past overvoltage detection, there is a point when the Zener diodes will turn on. These internal diodes are in place to protect the device from short high voltage or ESD events and should NOT be used as a feature to reduce the voltage on a line. Continued exposure to voltages higher than normal operating voltage, $V_{CC,}$ can weaken or damage the Zener diodes, which will potentially damage the part.

FORWARD AND REVERSE SUPPLY VOLTAGE

This is the greatest voltage that can be supplied to V_{CC} from GND during programing or transient switching. This voltage should not be used as a DC voltage bias for an extended time.

FORWARD AND REVERSE OUTPUT VOLTAGE

The Forward Output Voltage, $V_{FOUT,}$ should be no greater than V_{CC} + 0.5 up to 6.5 V. This is the greatest voltage that the output and reference output can be biased with from GND during programming or transient switching. The Reverse Output Voltage, $V_{ROUT,}$ should not drop below –0.5 V during programming or transient switching. These voltages should not be used as a DC voltage bias for an extended time.

These voltage levels apply to the no connect pins as well.

OUTPUT SOURCE AND SINK CURRENT

This is the maximum current that V_{IOUT} can passively sink or source before damage may occur.

AMBIENT TEMPERATURE (T_A)

This is the ambient temperature of the device. The Operating Ambient Temperature Range is the ambient temperature range in which the Common Electricals and Common Performance Characteristics limits are valid. ACS37003 devices have optimized performance in the –40°C to 125°C (“K” temperature) range.

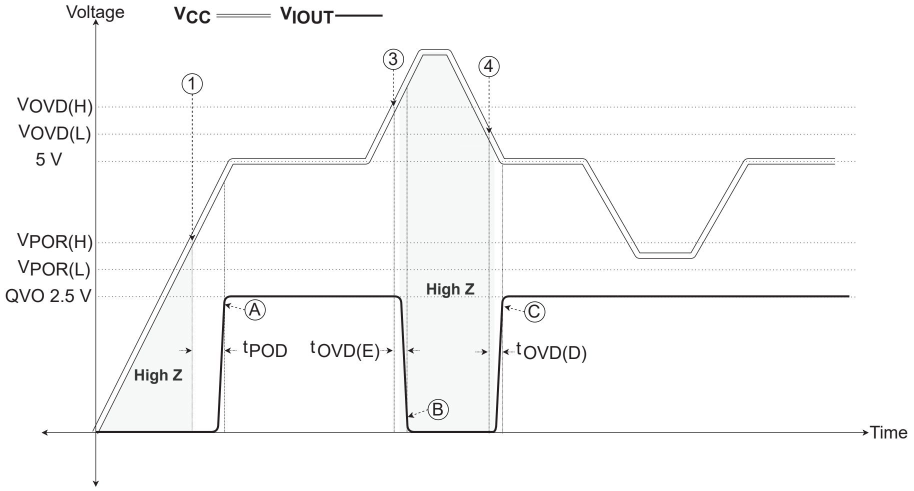


Figure 6: t_{POD}, and $t_{OVD(E/D)}$ with R_L = Pull-Up

DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Zero Current Voltage Output ($V_{IOUT(Q)}$, QVO)

Zero Current Voltage Output, $V_{IOUT(Q)}$ (also called QVO), is defined as the voltage on the output, V_{IOUT}, when no current is applied through I_P.

QVO Temperature Drift (V_{QE})

QVO Temperature Drift, V_{QE}, is defined as the drift of QVO from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively). To improve over temperature performance, the temperature drift is compensated with Allegro factory trim to remain within the limits across temperature.

Reference Voltage (V_{REF})

There is a Voltage Reference Output, V_{REF}, on the ACS37003. This output reports the zero current voltage for the output channel allowing for differential measurement.

Reference Voltage Temperature Drift (V_{RE})

Reference Voltage Temperature Drift, V_{RE}, is defined as the drift of V_{REF} from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively).

Offset Voltage (V_{OE})

Offset Voltage, V_{OE}, is defined as the difference between QVO and V_{REF} (see Figure 7). V_{OE} includes the drift of QVO minus V_{REF} from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively).

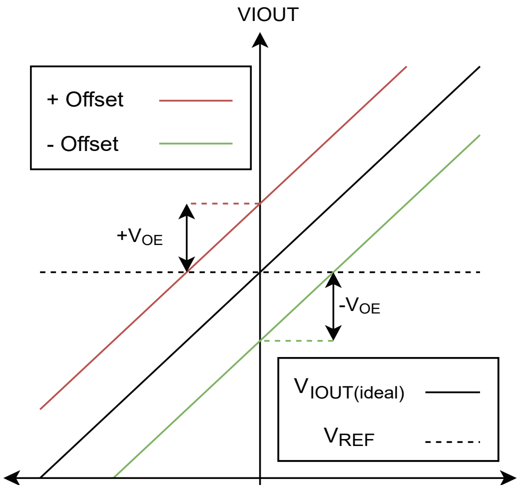


Figure 7: Offset (V_{OE}) Between V_{IOUT} and V_{REF}

Output Saturation Voltage ($V_{SAT(HIGH/LOW)}$)

Output Saturation Voltage, V_{SAT}, is defined as the voltage that V_{IOUT} does not pass as a result to an increasing magnitude of current. $V_{SAT(HIGH)}$ is the highest voltage the output can drive to while, $V_{SAT(LOW)}$ is the lowest. This can be seen in Figure 8. Note that changing the sensitivity does not change the V_{SAT} points.

OUTPUT VOLTAGE OPERATING RANGE (V_{OOR})

The Output Voltage Operating Range, or V_{OOR}, is the functional range for linear performance of V_{IOUT} and its related datasheet parameters. This can be seen in Figure 8. The V_{OOR} is the output region that the performance accuracy parameters are valid. It is possible for the output to report beyond these voltages until V_{SAT}, but operation cannot be guaranteed. The output performance is demonstrated in Figure 8 through and beyond the V_{OOR}.

Voltage Output Operating Range for V_{CC} and Output Modes, $V_{OOR(Vcc, Mode)}$		
V_{CC} (V)	Bidirectional	Unidirectional
3.3	±1.32	+2.64
5	±2	+4

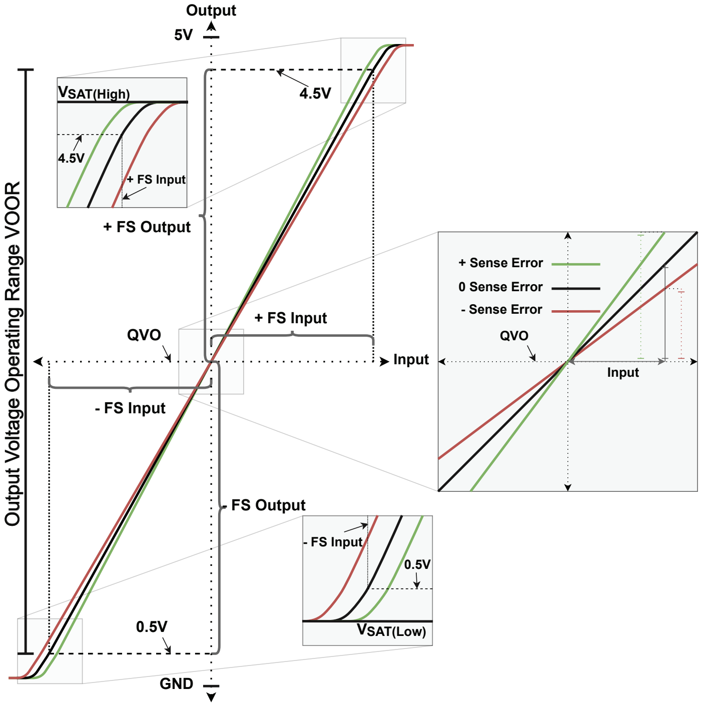


Figure 8: V_{OOR}, V_{SAT} and SENS with Full Scale

Sensitivity (Sens)

Sensitivity, or Sens, is the ratio of the output swing versus the applied current through the primary conductor, I_P. This current causes a voltage deviation away from QVO on the V_{IOUT} output until V_{SAT}. The magnitude and direction of the output voltage swing is proportional to the magnitude and direction of the applied current. This proportional relationship between output and input is Sensitivity and is defined as:

$$Sens = \frac{V_{IOUT(I1)} - V_{IOUT(I2)}}{I_1 - I_2}$$

where I_1 and I_2 are two different currents, and $V_{IOUT(I1)}$ and $V_{IOUT(I2)}$ are the voltages of the device with the applied currents. One of these measurement points can be with no current applied.

Sensitivity Error (E_{sens})

Sensitivity Temperature Drift, or $E_{sens,}$ is defined as the drift of Sens from room to hot or room to cold (25°C to 125°C or 25°C to –40°C, respectively). No trimming/programming is needed as temperature drift is compensated with Allegro factory trim to remain within the datasheet limits across temperature.

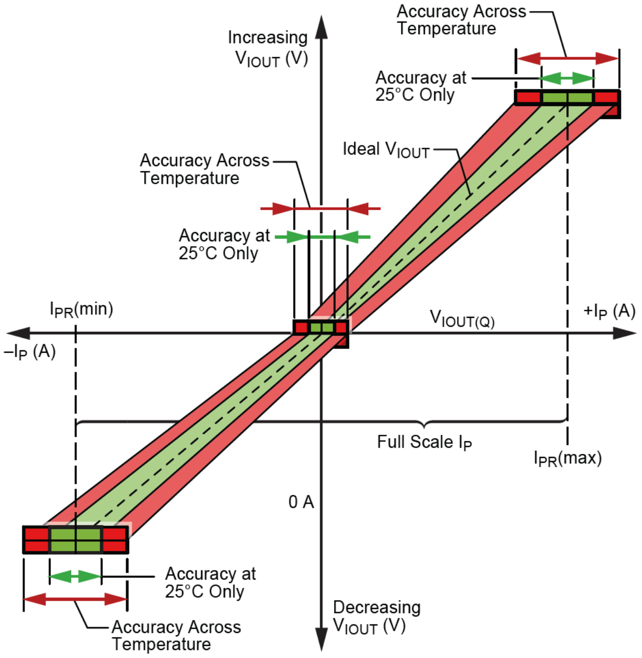


Figure 9: Output Accuracy Pocket for Room and Across Temperature

Full Scale (FS)

Full Scale, or FS, is a method to relate an input and/or output to the maximum input and/or output of the device. For example, 50%FS of a 10 A sensor is 5 A, or 50% of its maximum input current. The 50% input of 5 A will cause the output to move 50%, or 50%FS. FS is used to interchangeably refer to input and output deviations when discussing input steps and relating input to output performance. FS_{INPUT} is the input bias that results in FS_{OUTPUT} and these two are directly related by the device sensitivity. Both polarities of FS can be seen in Figure 8, labeled as positive or negative FS input and FS output. The equation for input referred FS for a 5 V bidirectional device is:

$$\mathrm{FS} = \frac{\mathrm{V_{OOR(5V,Bi)}}}{\mathrm{Sens_{Actual}}} = \pm\frac{2\mathrm{V}}{\mathrm{Sens_{Actual}}}$$

Note: a percentage change in FS_{INPUT} is equivalent to a resultant percentage change of FS_{OUTPUT} and visa versa.

Nonlinearity (E_{LIN})

As the amount of current applied to the part changes, the sensitivity of the device can also change slightly. This is referred to as Linearity Error or E_{LIN} (see Figure 10). Consider two currents, I_1(1/2 FS) and I_2(FS). Ideally, the sensitivity of the device is the same for both currents. Linearity Error is calculated as the percent change in sensitivity from one current to another. Error is calculated separately for positive ($E_{LIN(+)}$) and negative ($E_{LIN(-)}$) currents, and the percent errors are defined as:

$$\mathrm{E_{LIN(\pm)}} = \left(1 - \frac{\mathrm{Sense_{I2\pm}}}{\mathrm{Sens_{I1\pm}}}\right) \times 100\%$$

where the sensitivities are defined as:

$$\mathrm{Sens_{IX+}} = \frac{\mathrm{V_{IOUT(IX+)}} - \mathrm{V_{REF}}}{\mathrm{I_{X+}}}$$

$$\mathrm{Sens_{IX-}} = \frac{\mathrm{V_{IOUT(IX-)}} - \mathrm{V_{REF}}}{\mathrm{I_{X-}}}$$

I_X are positive and negative currents through I_P such that:

$$\mathrm{I_{2+}} = 2 \times \mathrm{I_{1+}}$$

$$\mathrm{I_{2-}} = 2 \times \mathrm{I_{1-}}$$

Linearity error is the maximum of the positive and negative linearity error.

Total Output Error (E_{TOT})

Total Output Error is the current measurement error from the sensor IC as a percentage of the actual applied current. This is equivalent to the difference between the ideal output voltage and the actual output voltage, divided by the ideal sensitivity, relative to the current applied to the device, or simplified to:

$$E_{TOT} = \frac{V_{IOUT(ACTUAL)} - (Sens_{(IDEAL)} \times I_{PR} + V_{REF})}{(Sens_{(IDEAL)} \times I_{PR})} \times 100$$

Total Output Error incorporates all sources of error and is a function of current. At relatively high currents Sensitivity Error will be the largest contributor to Total Output Error. At relatively low inputs, Offset Voltage, V_{OE}, will be the largest contributor to Total Output Error. At I = 0 A, Total Output Error approaches infinity due to the offset. An example of total error at FS can be seen in Figure 10.

Note: Total Output Error goes to infinity as the amount of applied field approaches 0 A.

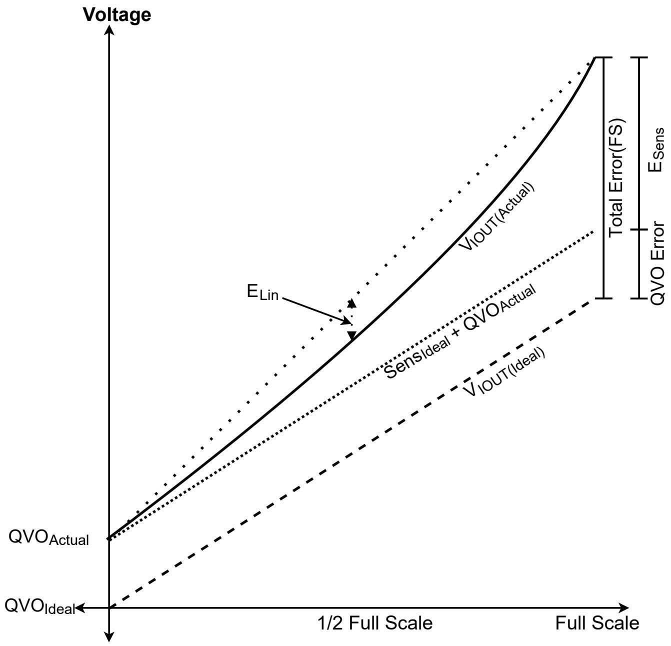


Figure 10: Accuracy Error

Power Supply Offset Error ($V_{OE(PS)}$)

Power Supply Offset Error, $V_{OE(PS)}$, is defined as the difference in offset error when V_{CC} is at the nominal and V_{CC} is 10% high or low. For a 5 V device, this is 5 to 4.5 V and 5 to 5.5 V. For a 3.3 V device, this is 3.3 to 3 V and 3.3 to 3.6 V.

Offset Power Supply Rejection Ratio ($PSRR_O$)

The Offset Power Supply Rejection Ratio, $PSRR_{O,}$ is an AC test of the $V_{OE(PS)}$ parameter. A 100 mV peak AC signal is added on top of the nominal supply voltage. Any AC impact on the output offset of the sensor is measured and recorded as $PSRR_{O.}$ The equation used to calculate $PSRR_O$ shown below:

$$PSRR_O = 20 \times \log\left(\frac{\Delta QVO}{\Delta V_{CC}}\right)$$

Power Supply Sensitivity Error ($E_{SENS(PS)}$)

Power Supply Sensitivity Error, or $E_{SENS((PS),}$ is defined as the percent sensitivity error measured between V_{CC} and V_{CC} ±10%. For a 5 V device, this is 5 to 4.5 V and 5 to 5.5 V. For a 3.3 V device, this is 3.3 to 3 V and 3.3 to 3.6 V.

Sensitivity Power Supply Rejection Ratio ($PSRR_S$)

The Sensitivity Power Supply Rejection Ratio or $PSRR_S$ is defined as 20 × log of the ratio of the % change the sensitivity over the % change in V_{CC} (±100 mV variable AC V_{CC} centered at 5 V) reported as dB in a specified frequency range. This is the AC version of the $E_{SENS(PS)}$ parameter. The equation is shown below:

$$PSRR_S = 20 \times \log\left(\frac{\Delta \%Sens}{\Delta V_{CC}}\right)$$

DYNAMIC RESPONSE PARAMETERS

The descriptions in this section assume an ambient temperature of 25°C and output loads within limits provided in the Common Electricals table. The step applied is a input step that corresponds to 1 V deviation on the output, unless otherwise stated.

Propagation Time (t_{pd})

The time interval between a) when the sensed current reaches 10% of its stable value, and b) when the sensor output reaches 10% of its stable value for a step input. See Figure 11.

Rise Time (t_R)

The time interval between a) when the sensor reaches 10% of its stable value, and b) when it reaches 90% of the stable value for a step input. See Figure 11.

Response Time ($t_{RESPONSE}$)

The time interval between a) when the sensed current reaches 90% of its stable value, and b) when the sensor output reaches 90% of its stable value. See Figure 11.

Temperature Compensation

To help compensate for the effects temperature has on performance, the ACS37003 has an integrated internal temperature sensor. This sensor and compensation algorithms help to standardize device performance over the full range of optimized temperatures. This allows for room temperature system calibration and validation of end-of-line modules.

Temperature Compensation Update Rate

There is an 8 ms update time that is required to maintain a valid temperature compensated output; that is, temperature compensations are calculated and applied every 8 ms.

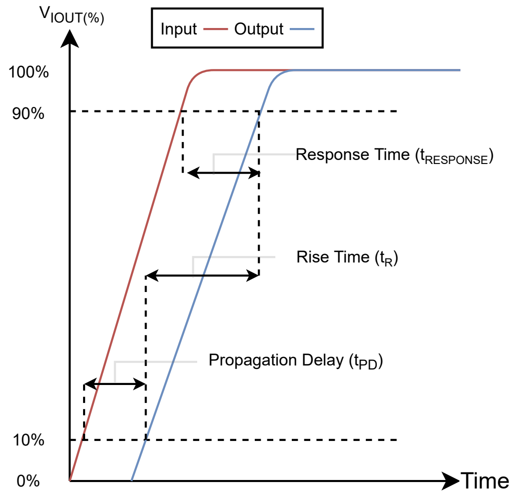


Figure 11: Dynamic Response Parameters

APPLICATION INFORMATION

Thermal Rise vs. Primary Current

Self-heating due to the flow of current should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current, current "on-time", and duty cycle. While the data presented in this section was collected with direct current (DC), these numbers may be used to approximate thermal response for both AC signals and current pulses.

The plot in Figure 12 shows the measured rise in steady-state die temperature of the ACS37003KMC versus continuous current at an ambient temperature, T_A, of 25 °C. The thermal offset curves may be directly applied to other values of T_A. Conversely, Figure 13 shows the maximum continuous current at a given T_A. Surges beyond the maximum current listed in Figure 13 are allowed given the maximum junction temperature, $T_{J(MAX)}$ (165°C), is not exceeded.

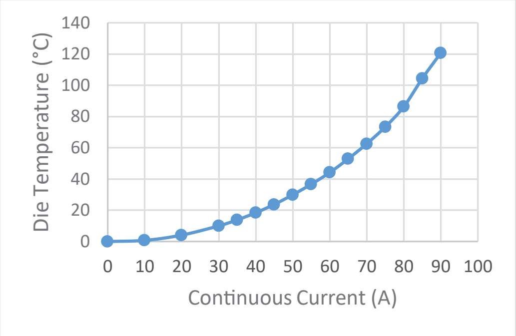


Figure 12: Self-heating in the MC package due to current flow

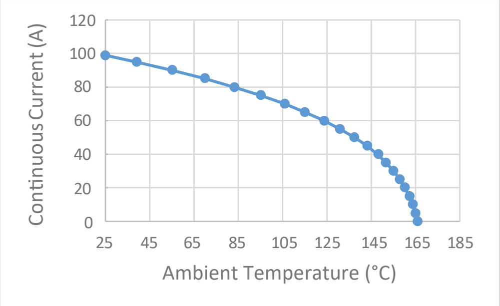


Figure 13: Maximum continuous current at a given T_A

The thermal capacity of the ACS37003KMC should be verified by the end user in the application's specific conditions. The maximum junction temperature, $T_{J(MAX)}$, should not be exceeded. Further information on this application testing is available in the "DC and Transient Current Capability" application note [1] on the Allegro website.

ASEK37003-Panel Evaluation Board Layout

Thermal data shown in Figure 12 and Figure 13 was collected using the ASEK37003-Panel Evaluation Board (TED-0003314). This board includes 750 mm^2 of 4 oz. (0.1388 mm) copper connected to pins 1 through 4, and to pins 5 through 8, with thermal vias connecting the layers. Top and bottom layers of the PCB are shown below in Figure 14.

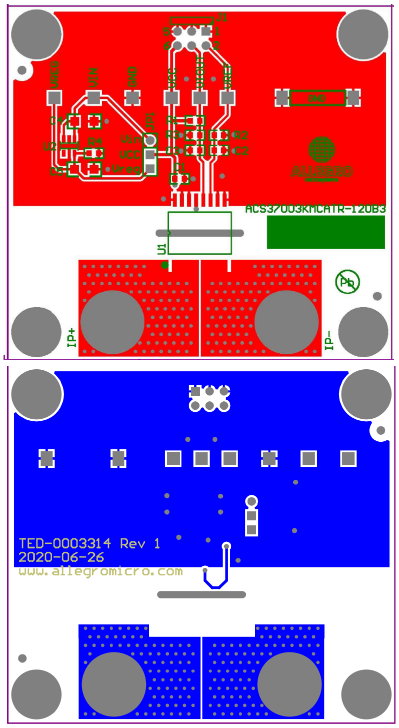


Figure 14: Top and bottom layers for ASEK37003-Panel evaluation board

Gerber files for the ASEK37003-Panel evaluation board are available for download from the Allegro website. See the technical documents section of the ACS37003KMC device webpage [2].

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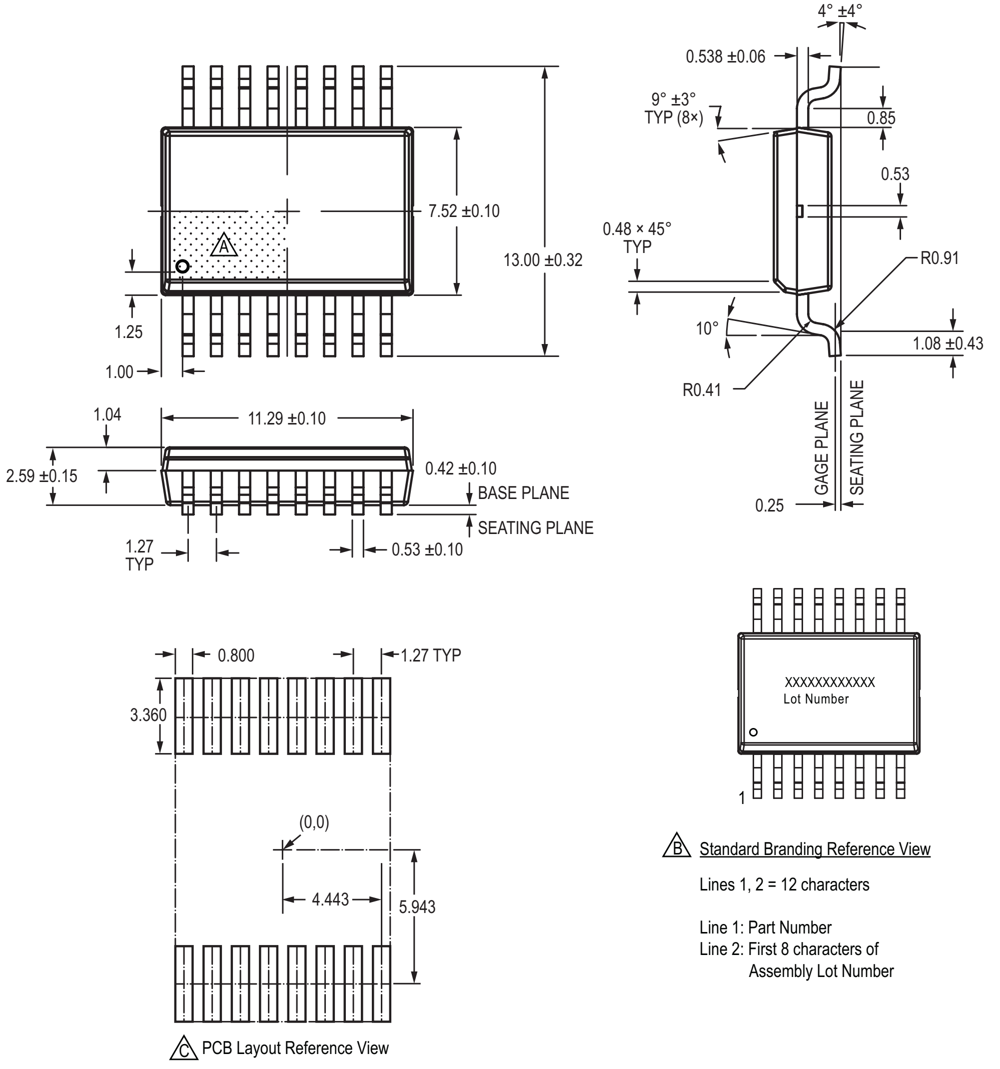
[1] http://www.allegromicro.com/en/Design-Center/Technical-Documents/Hall-Effect-Sensor-IC-Publications/DC-and-Transient-Current-Capability-Fuse-Characteristics.aspx

[2] https://www.allegromicro.com/en/products/sense/current-sensor-ics/zero-to-fifty-amp-integrated-conductor-sensor-ics/acs37003

PACKAGE OUTLINE DRAWING

For Reference Only; Not for Tooling Use

(reference DWG-0000714, Rev. 2)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Lines 1, 2 = 12 characters

Line 1: Part Number
Line 2: First 8 characters of
Assembly Lot Number

△A Terminal #1 mark area
△B Branding scale and appearance at supplier discretion
△C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 15: Package MC, 16-Pin SOICW

Revision History

Number	Date	Description
–	December 16, 2020	Initial Release
1	April 6, 2021	Addition of RoHS and Pb free symbols on page 2. Update to Total Error and Total Error Components tables and footnote on pages 8-11. Added Output Buffer Resistance characteristic to page 5. Editorial updates to all pages.
2	May 13, 2021	Updated sections of Performance Characteristics tables: Reference Error, Offset Error, and QVO Error minumum and maximum values, pages 8-11
3	July 23, 2021	Added bullet to Features and Benefits (page 1)
4	November 15, 2021	Updated Total Output Error equation (page 17); removed RoHS and Pb free symbols (page 2)
5	January 11, 2022	Updated package drawing (page 20)

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