

# EC200T

# Reference Design

**LTE Standard Module Series**

Rev. EC200T\_Reference\_Design\_V1.0

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# About the Document

## History

Revision	Date	Author	Description
1.0	2019-09-30	Jaye SANG/ Woody WU	Initial

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# 1 Reference Design

## 1.1. Introduction

This document provides the reference design for Quectel EC200T module. And the reference design includes power-on/off and reset scenarios, block diagrams, power supply, UART interfaces, (U)SIM interface, audio interfaces, etc.

## 1.2. Power-on/off and Reset Scenarios

### 1.2.1. Power-on Scenario

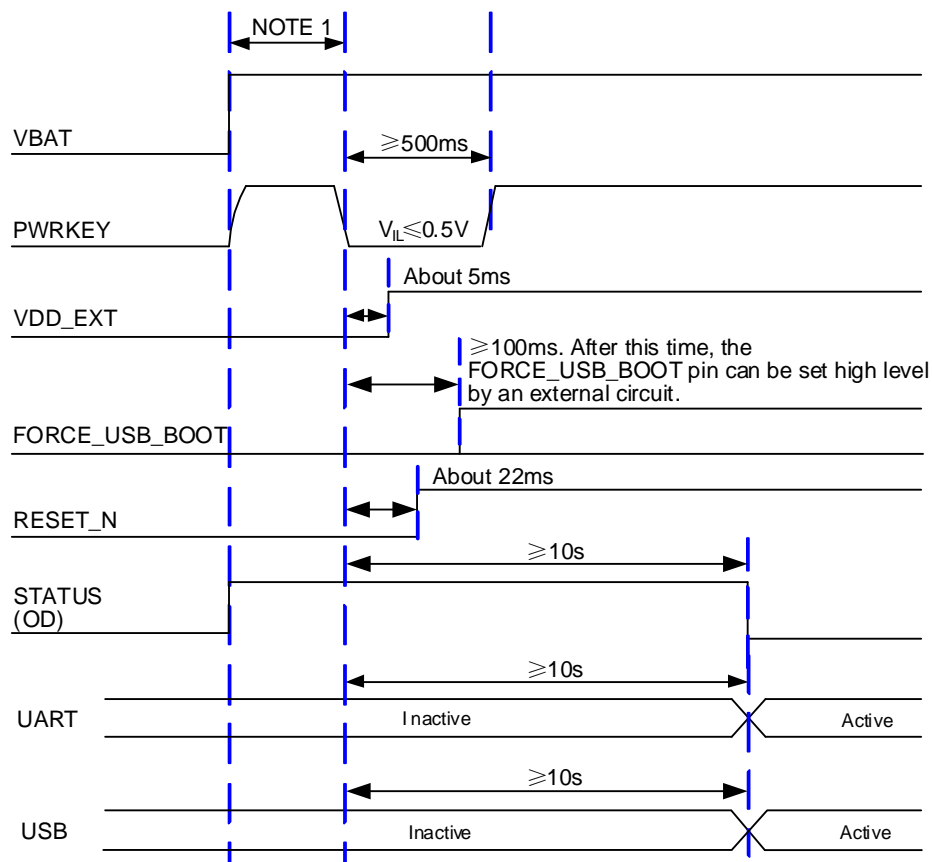


Figure 1: Timing of Turning on Module

## NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

### 1.2.2. Power-off Scenario

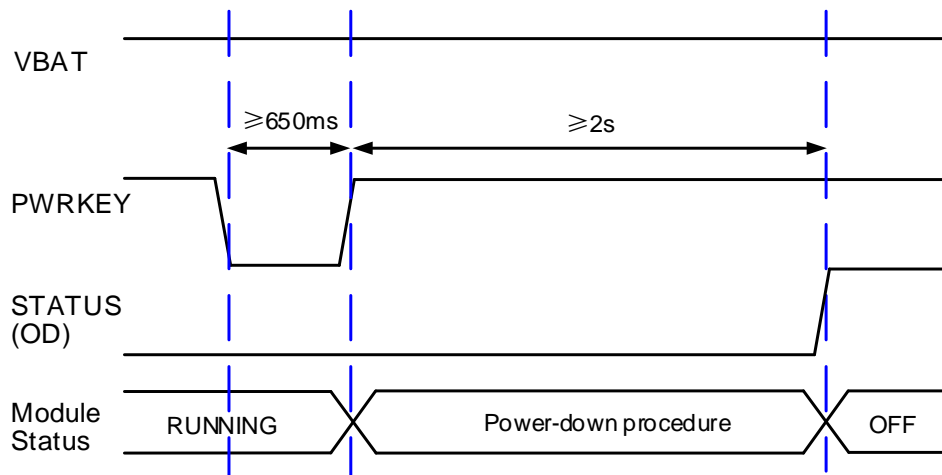
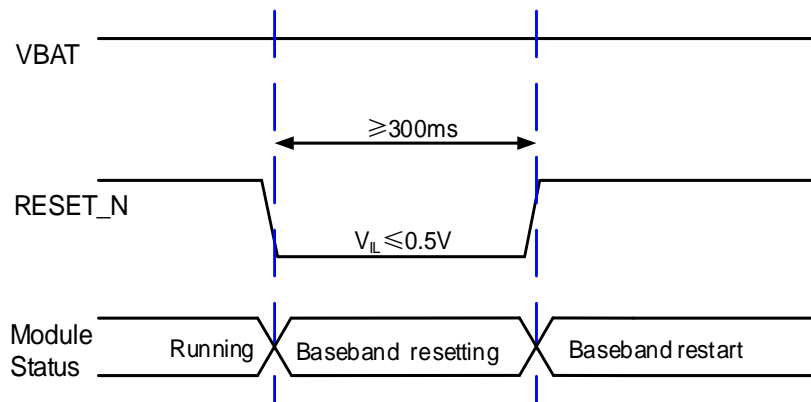


Figure 2: Timing of Turning off Module

## NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with the AT command, please keep PWRKEY at a high level after the execution of the command. Otherwise, the module will turn itself back on after being shut down.

### 1.2.3. Reset Scenario



**Figure 3: Timing of Resetting Module**

#### NOTES

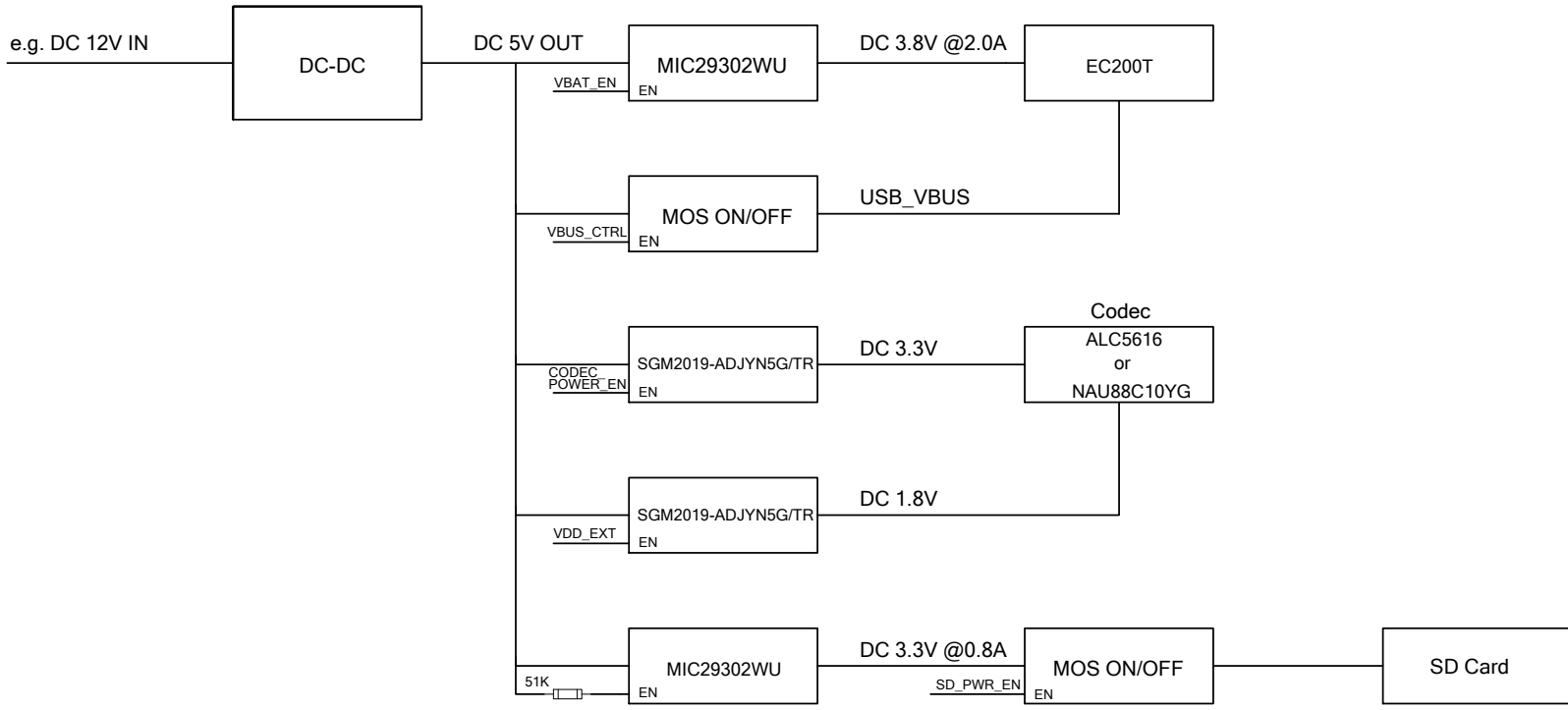
1. Please ensure that there is no large capacitance with the max value exceeding 10nF on PWRKEY and RESET\_N pins.
2. RESET\_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. It is recommended to use RESET\_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

### 1.3. Schematics

The schematics illustrated in the following pages are provided for your reference only.

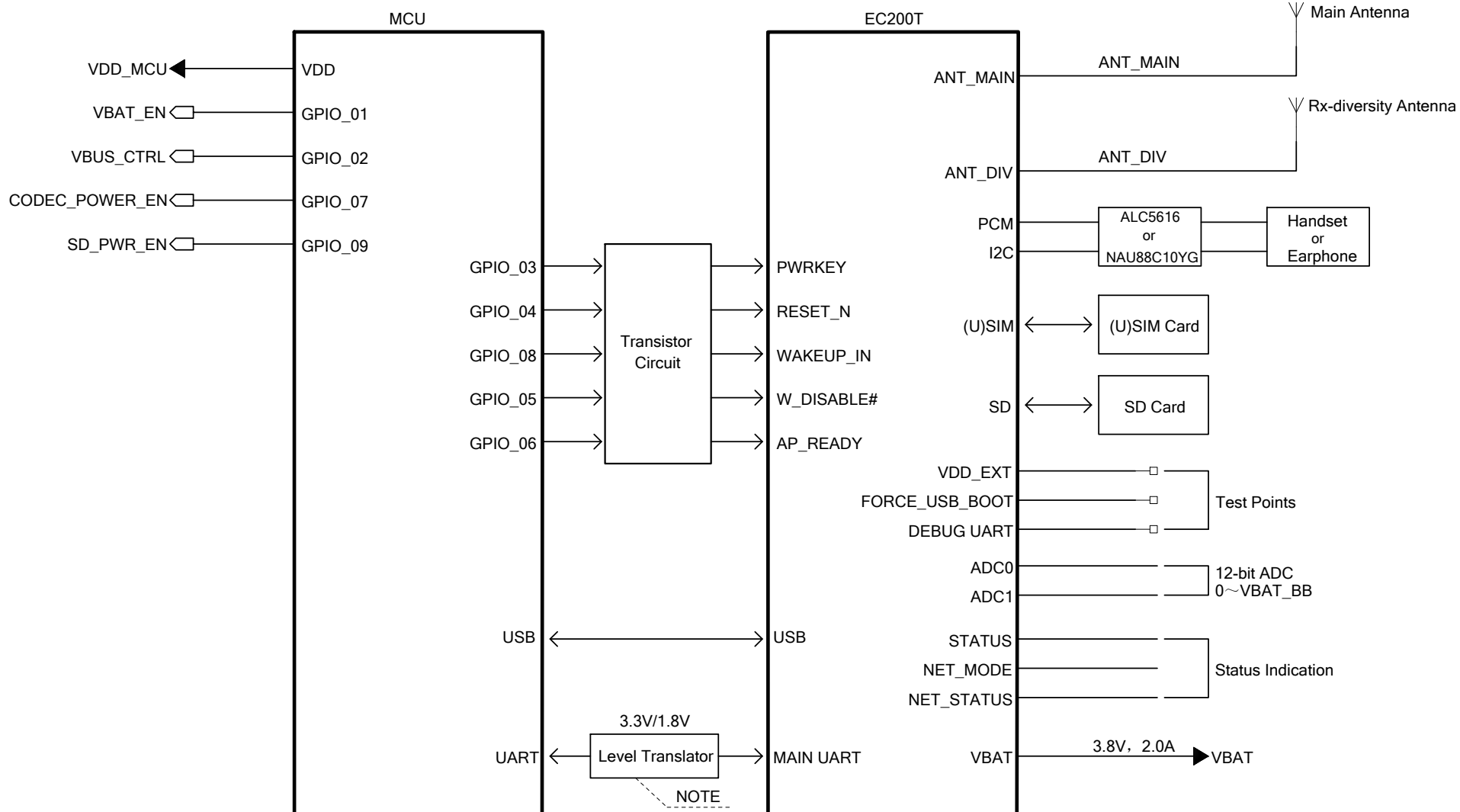


# Power Supply Block Diagram



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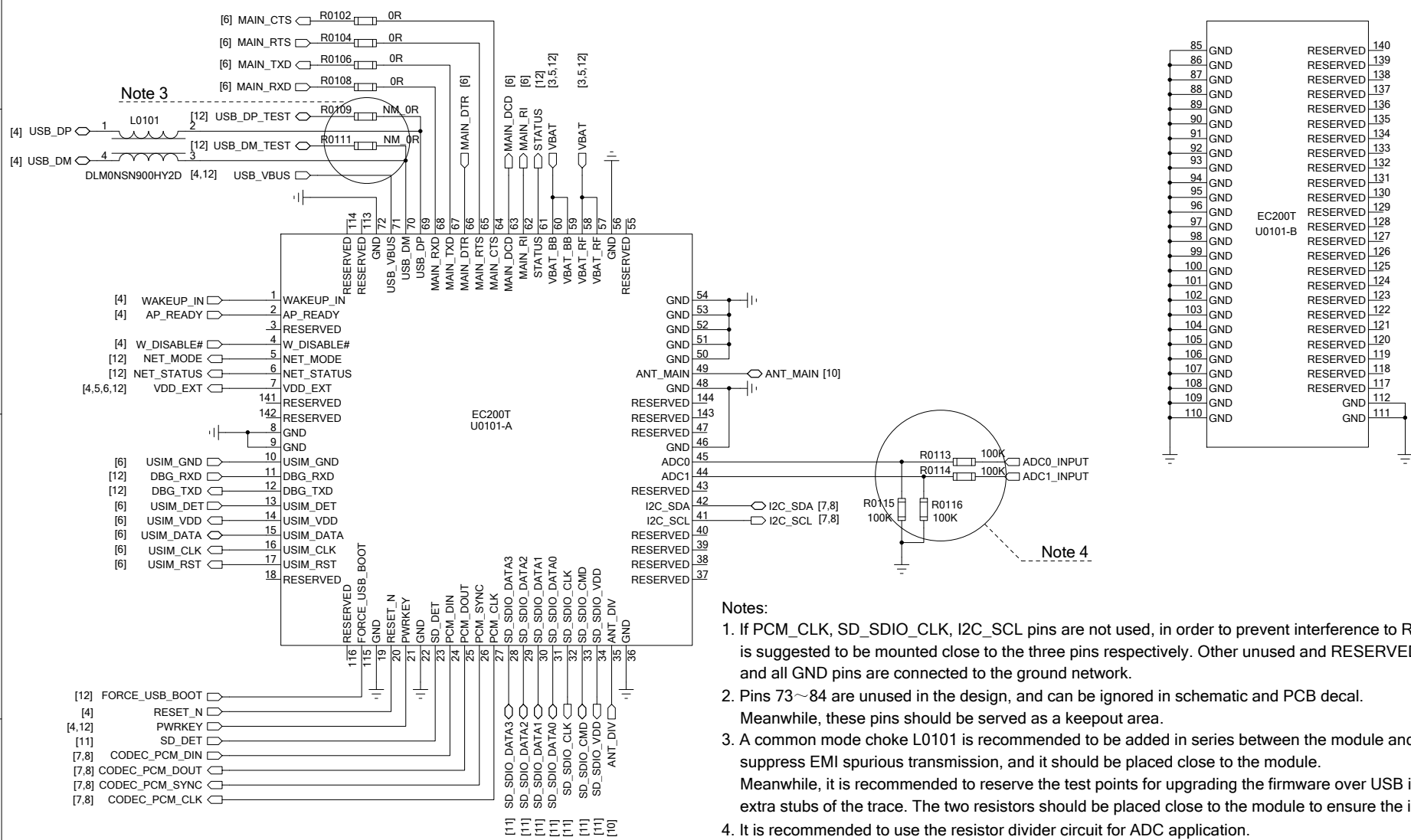
# Reference Design Block Diagram



NOTE:  
A transistor translation circuit or a level translator TXS0108EPWR provided by Texas Instruments is recommended.

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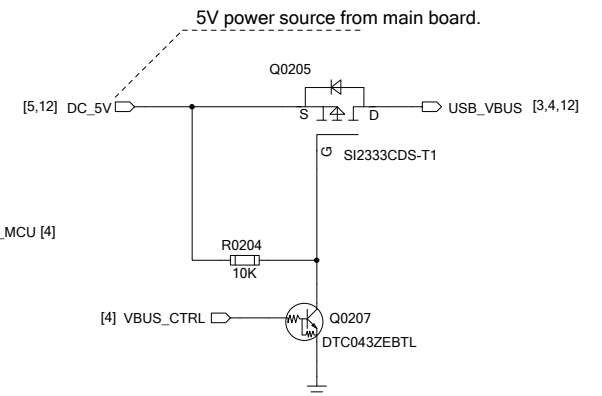
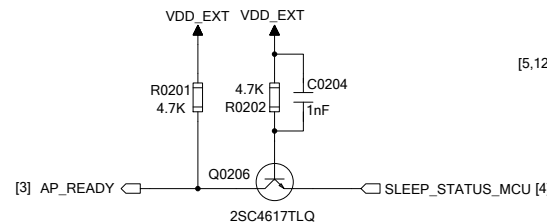
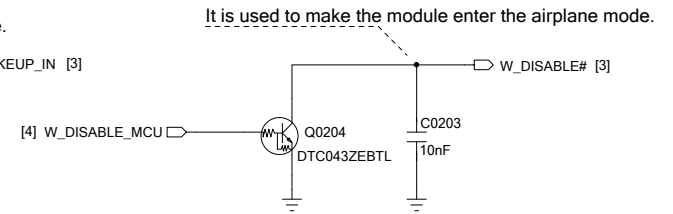
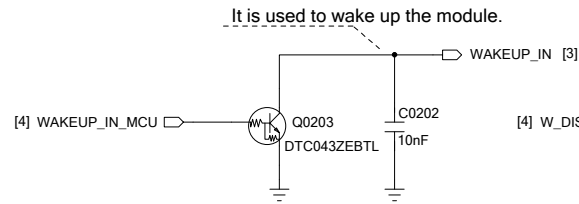
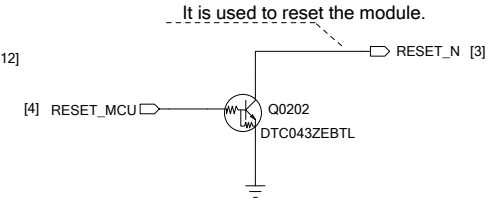
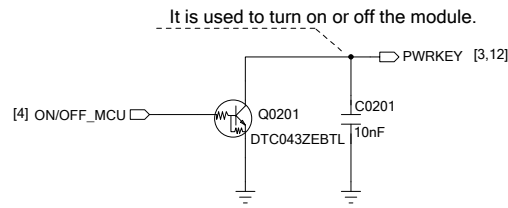
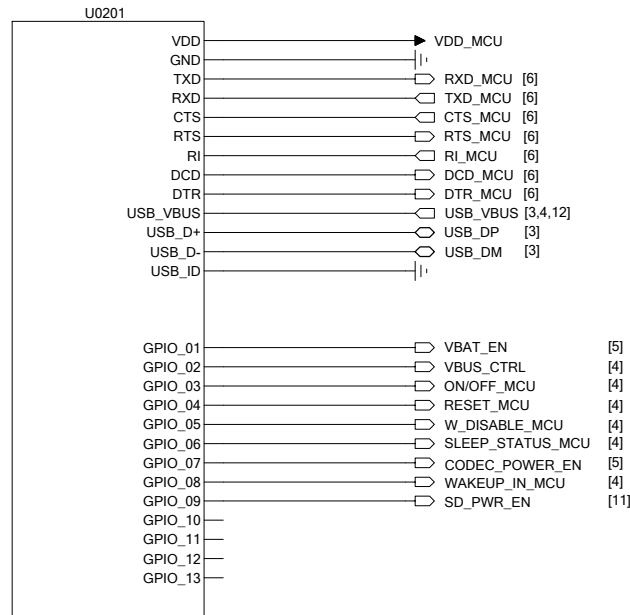
# Module Interface



- Notes:**
1. If PCM\_CLK, SD\_SDIO\_CLK, I2C\_SCL pins are not used, in order to prevent interference to RF, a 33pF capacitor is suggested to be mounted close to the three pins respectively. Other unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.
  2. Pins 73~84 are unused in the design, and can be ignored in schematic and PCB decal. Meanwhile, these pins should be served as a keepout area.
  3. A common mode choke L0101 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module. Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module to ensure the integrity of USB signal.
  4. It is recommended to use the resistor divider circuit for ADC application.

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# MCU Interface



**Notes:**

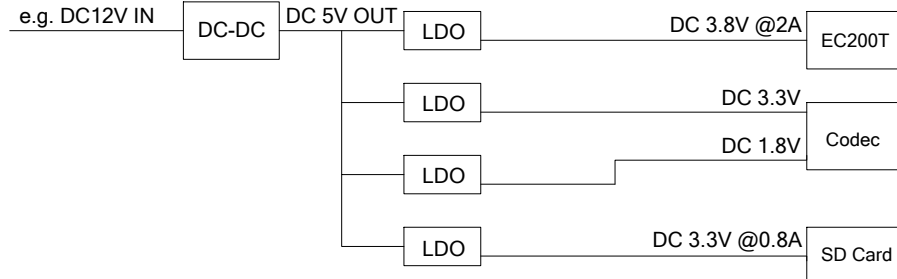
- U0201 represents customer's MCU. The power domain of GPIO interfaces of EC200T module is 1.8V; if the GPIO interfaces of U0201 share the same power domain, then the related level translation circuit can be omitted.
- The USB interface of EC200T can only serves as a slave device and supports Full-speed and High-speed modes. To communicate with the USB interface, MCU needs to support USB host or OTG function. The USB\_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS\_CTRL is used to turn on/off the USB\_VBUS power supply.
- It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET\_N of the module. Please ensure that there is no large load capacitance with the max value exceeding 10nF on PWRKEY and RESET\_N pins.

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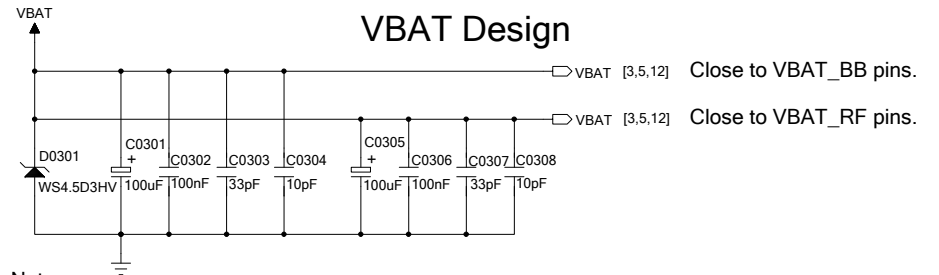
# Power Supply Design

## DC-DC Application

It is used when the input voltage is above 7.0V. Use a DC-DC converter to convert a high input voltage into a 5.0V output, and then the LDOs will generate 3.8V, 3.3V and 1.8V typical voltages.



## VBAT Design

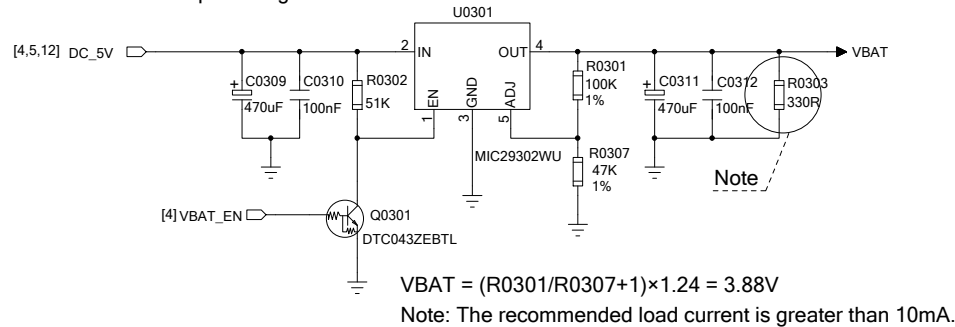


Notes:

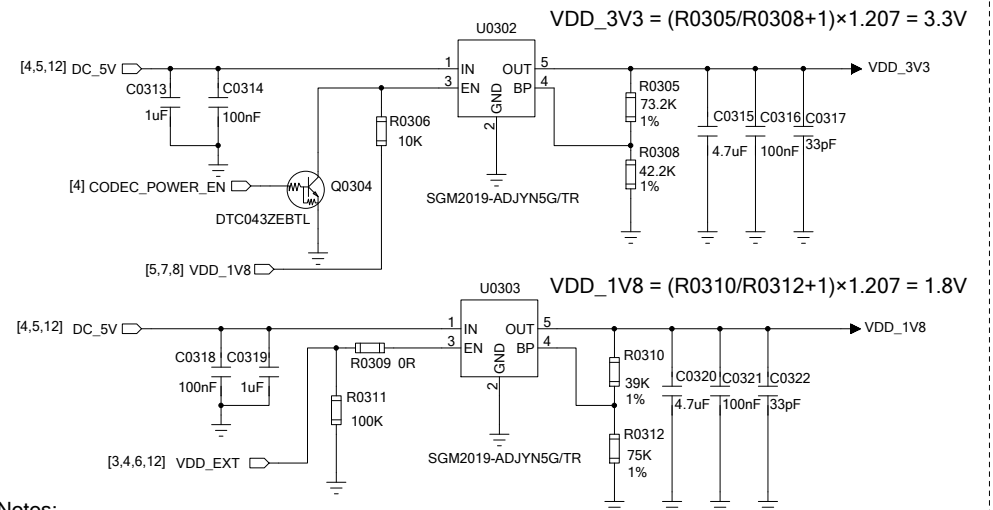
1. The power supply must be able to provide sufficient current up to 2.0A or more.
2. VBAT should be routed in star mode to VBAT\_BB and VBAT\_RF pins.
3. The recommended operating voltage of VBAT is 3.4V~4.5V.

## LDO Application

It is used when the input voltage is below 7.0V.



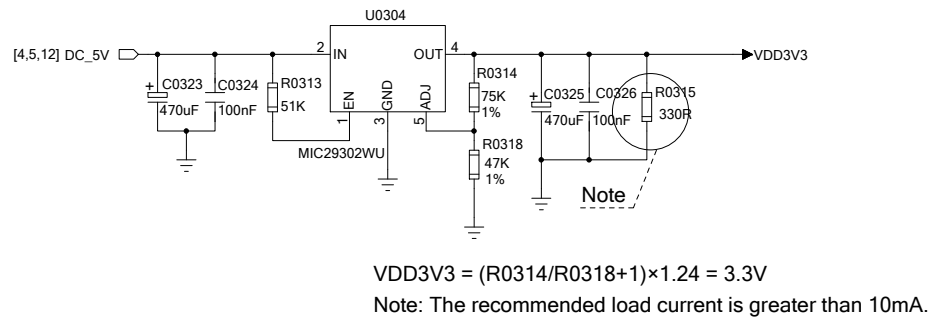
## Power Supply for PCM Codec



Notes:

1. CODEC\_POWER\_EN must be at a low level in order to ensure the normal output voltage of VDD\_3V3. If VDD\_3V3 power supply needs to be switched off, please keep CODEC\_POWER\_EN at a high level.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.  
Power-on Sequence: power on VDD\_1V8 first, then VDD\_3V3.  
Power-off Sequence: power off VDD\_3V3 first, then VDD\_1V8.

## Power Supply for SD Card

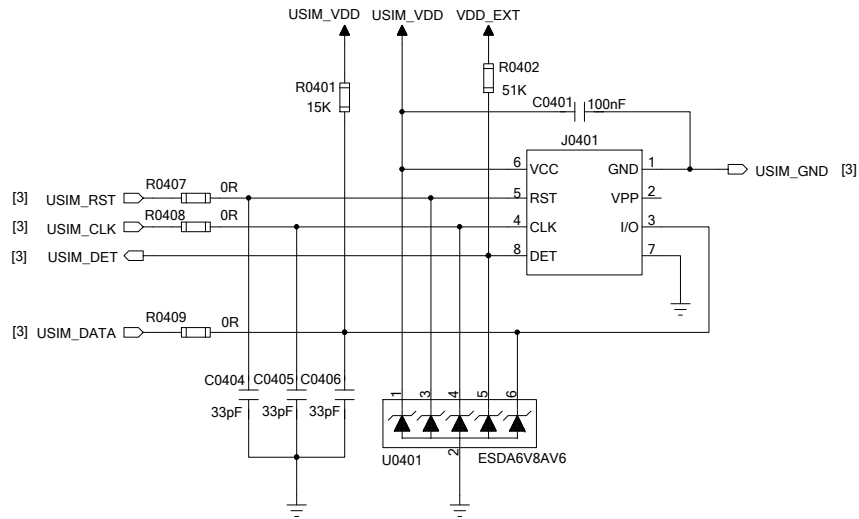


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# (U)SIM and UART Designs

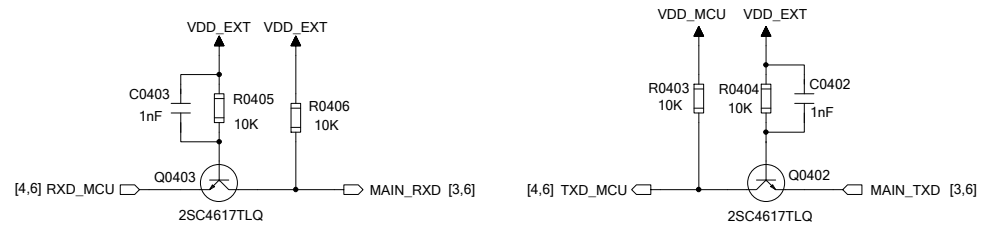
## (U)SIM Interface



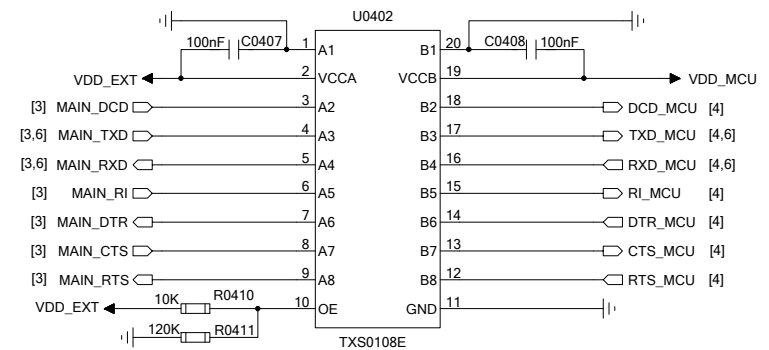
### Notes:

1. U401 is recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15pF.
2. The GND of the (U)SIM card connector is recommended to be connected to the module's USIM\_GND. In addition, it can be connected to the GND of customers' PCB directly if the PCB's GND is complete.
3. The pull-up resistor R0401 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
4. R0407~R0409 are used for debugging, and C0404~C0406 are used for filtering interference of EGSM900.
5. C0401's capacitance should be less than 1uF and it should be placed close to the (U)SIM card connector.
6. For more information about the layout of (U)SIM interface, please refer to *Quectel\_EC200T\_Hardware\_Design*.

## UART Translation - Transistor Solution



## UART Translation - IC Solution



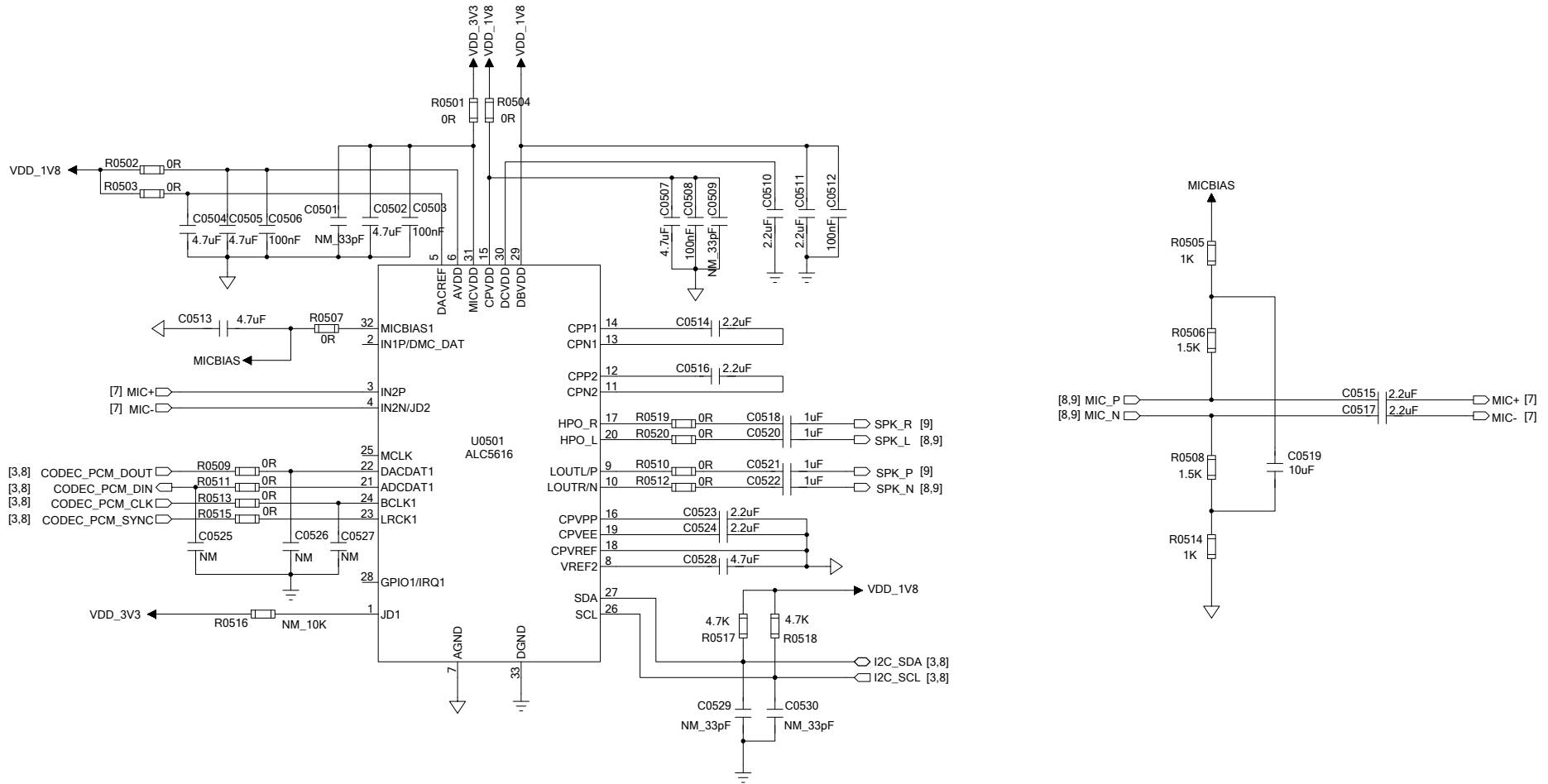
### Notes:

1. There are two translation solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0108E's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet from TI.
3. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps. The capacitors C0402 and C0403 of 1nF can improve the signal quality.
4. The RTS and DTR transistor circuits are similar to that of the RXD interface. The CTS, RI and DCD transistor circuits are similar to that of the TXD interface.

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# Audio Codec Design (ALC5616)



## Notes:

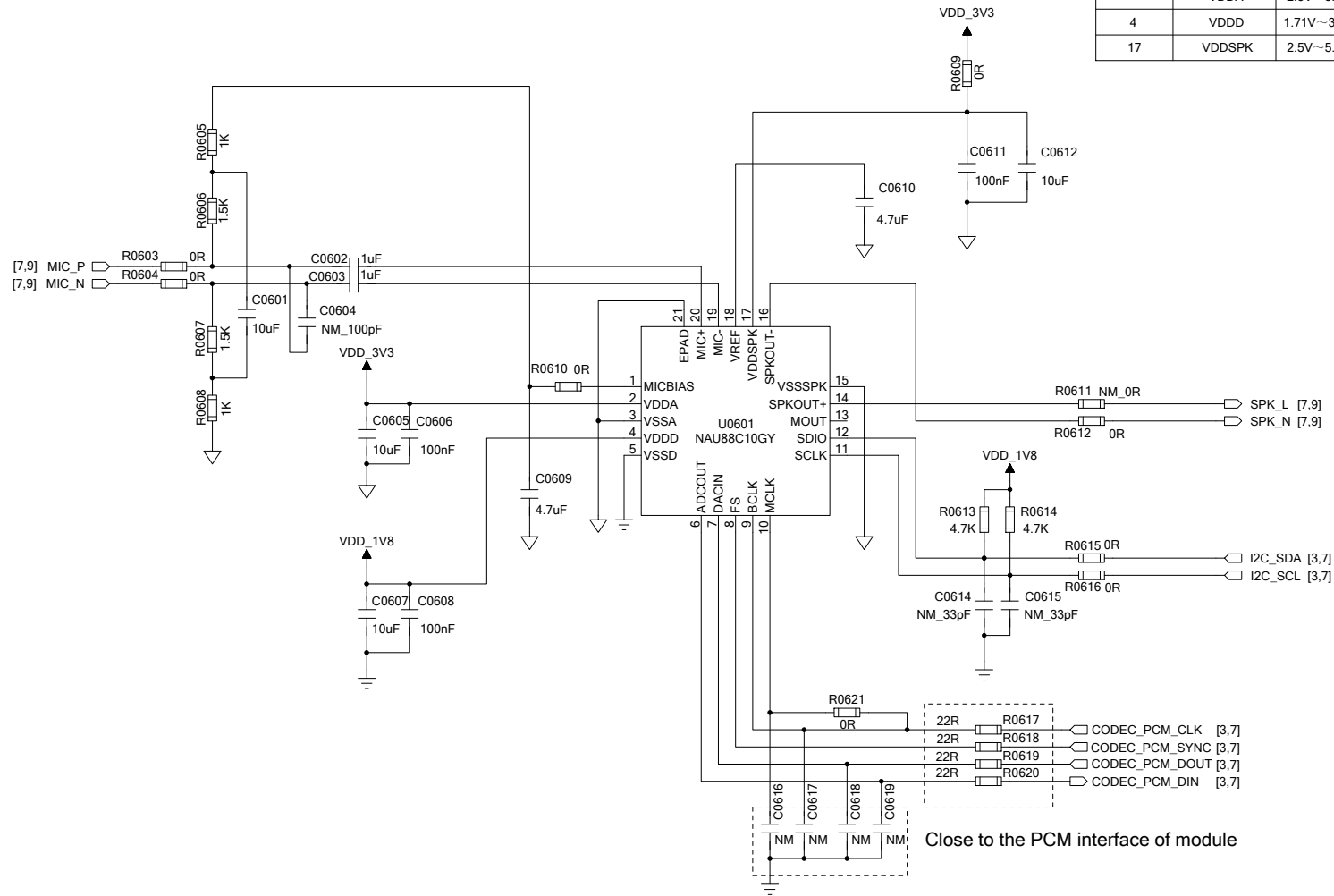
1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.
2. ALC5616 power-off sequence: disable codec function by software-> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. Module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.
4. The analog ground and digital ground need to be connected with a 0Ω resistor packaged as 0805. For more details, please refer to Sheet "Audio Interface Design".

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# Audio Codec Design (NAU88C10GY)

Pin No.	Pin Name	Voltage	Description
2	VDDA	2.5V~3.6V	Analog VDD
4	VDDD	1.71V~3.6V	Digital VDD
17	VDDSPK	2.5V~5.5V	Speaker power supply



**Notes:**

1. The codec part should be away from interference sources such as RF and power supply, and the codec audio signal should be surrounded with ground as much as possible.
2. The voltage of VDDA pin must always be no lower than that of VDDD.
3. The analog ground and digital ground need to be connected with a 0Ω resistor packaged as 0805. For more details, please refer to Sheet "Audio Interface Design".

Close to the PCM interface of module

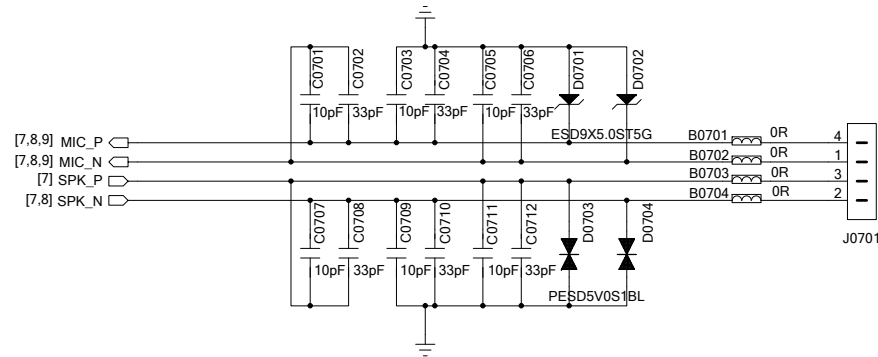
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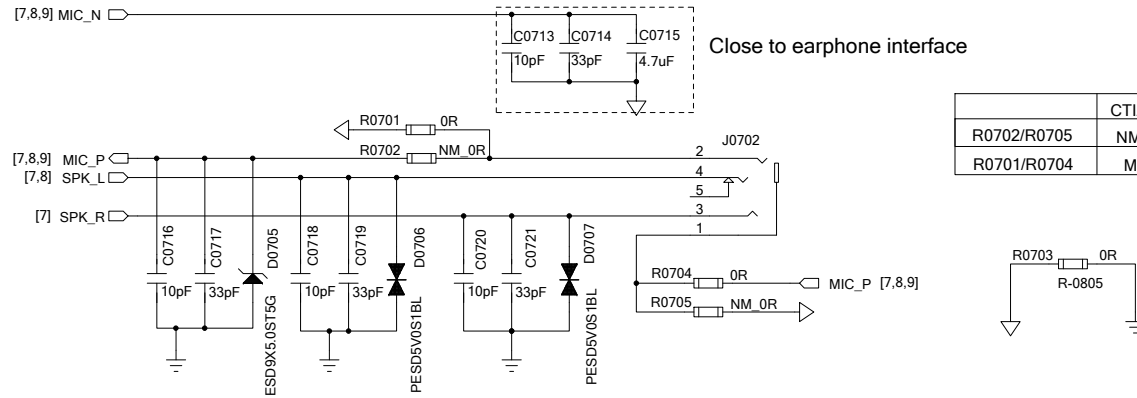


# Audio Interface Design

## Handset Application



## Earphone Application



### Notes:

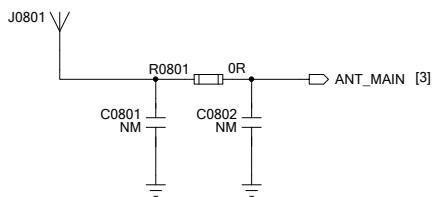
1. The analog output only drives earphone and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In earphone application, the MIC signal traces need to be routed as differential pairs.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noise such as clock and DC-DC signals, etc.
5. ALC5616 and NAU88C10GY cannot be used simultaneously in audio codec design.

## Quectel Wireless Solutions

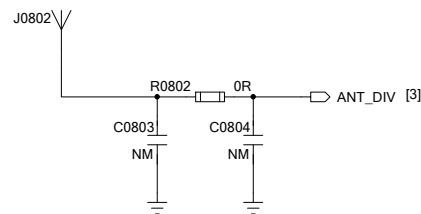
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# RF Design

## Main Antenna Circuit



## Rx-diversity Antenna Circuit



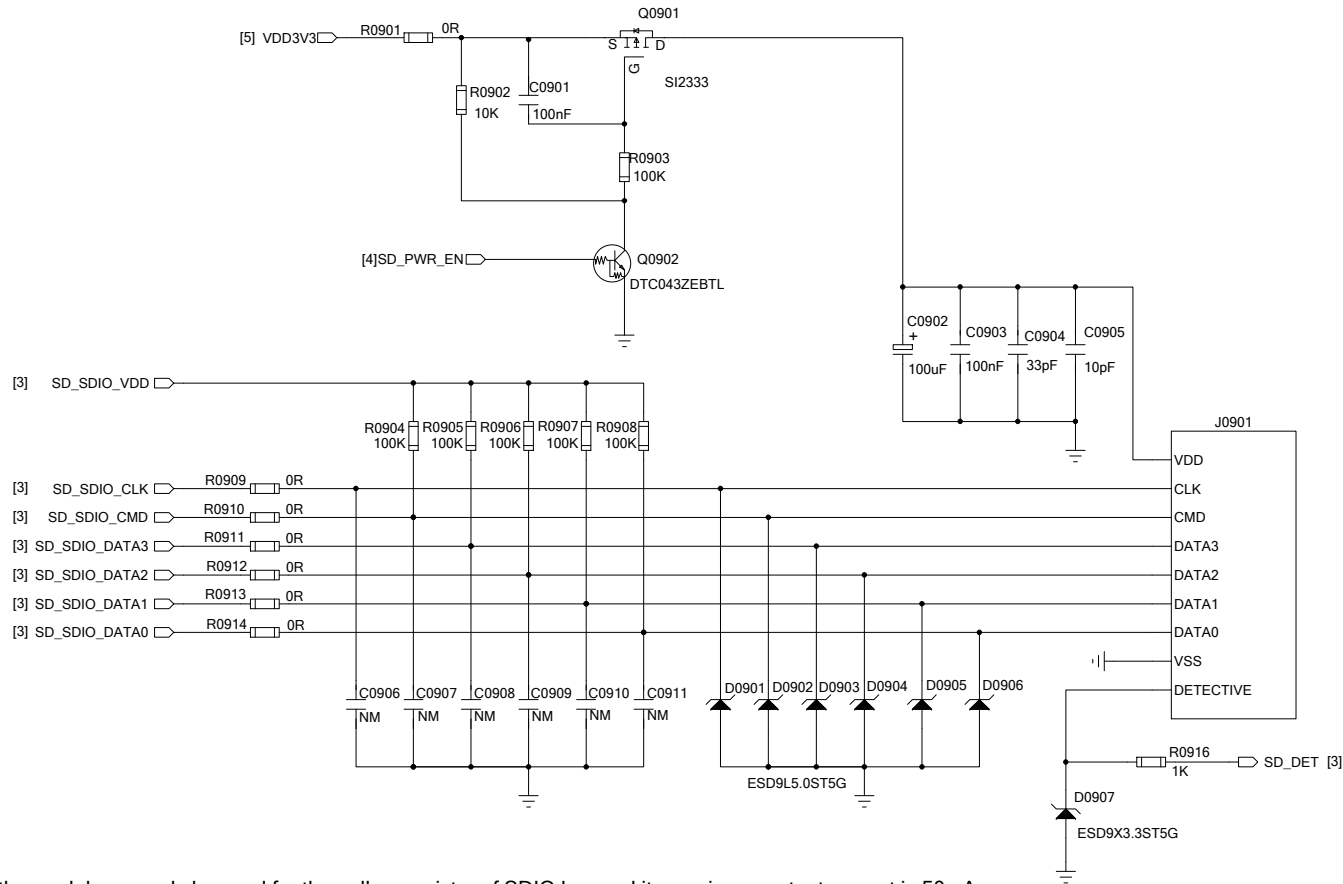
### Notes:

1. It is highly recommended to reserve a pi type main/Rx-diversity antenna circuit for convenient debugging in the future.
2. The impedance of the RF signal traces must be controlled as 50Ω when routing.

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# SD Card Interface Design



## Notes:

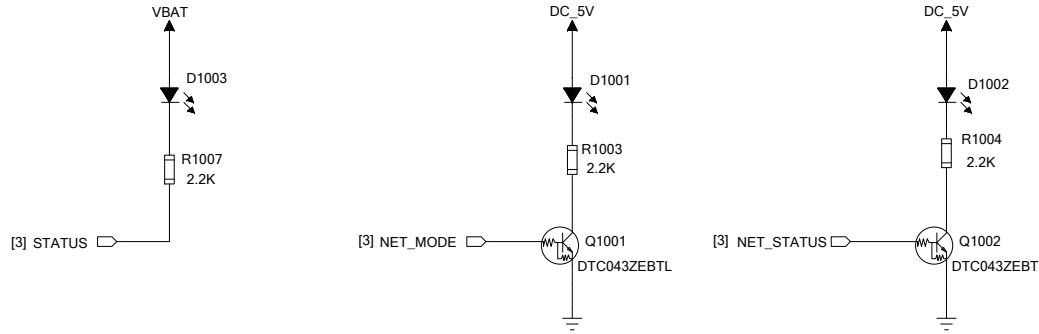
1. The pin 34 (SD\_SDIO\_VDD) on the module can only be used for the pull-up resistor of SDIO bus and its maximum output current is 50mA.
2. The supply voltage range of VDD for SD card is 2.7V~3.6V and needs to be provided with sufficient current up to 0.8A.
3. To avoid the jitter of bus, pull-up resistors R0904~R0908 are recommended to be added to SDIO bus. SD\_SDIO\_VDD should be used as the pull-up power. The values of these resistors are among 10kΩ~100kΩ and the recommended value is 100kΩ.
4. In order to adjust the signal quality, it is recommended to add 0Ω resistors R0909~R0914 in series between the module and the SD card connector. The bypass capacitors C0906~C0911 are reserved and not mounted by default.
5. It is recommended to add ESD protection components near the pins of SD card connector. The parasitic capacitance of ESD protection components should be smaller than 15pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. Route SDIO signals with 50Ω±10% impedance. It is important to route SDIO signals surrounded with ground on the layer and ground planes above and below, and the total trace length should be less than 50mm.
8. It is recommended to keep the trace length difference among SD\_SDIO\_CLK and SD\_SDIO\_DATA[0:3]/SD\_SDIO\_CMD less than 1mm.
9. Make sure the adjacent trace spacing is two times the trace width and the bus capacitance is less than 15pF.

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# Other Designs

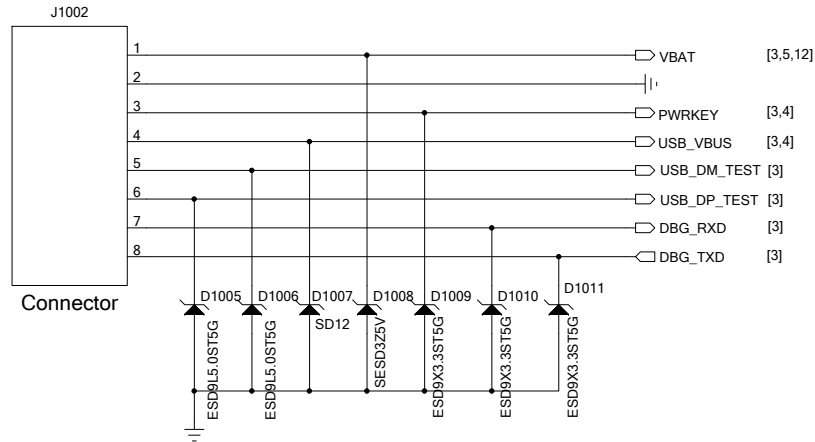
## Indicators



### Notes:

1. The STATUS is an open drain output pin.
2. For more details about NET\_MODE and NET\_STATUS, please refer to *Quectel\_EC200T\_Hardware\_Design*.
3. If the low current consumption is required when the customers' device is in sleep, the power supplies VBAT and DC\_5V of the STATUS, NET\_MODE, NET\_STATUS indicators can be replaced with external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

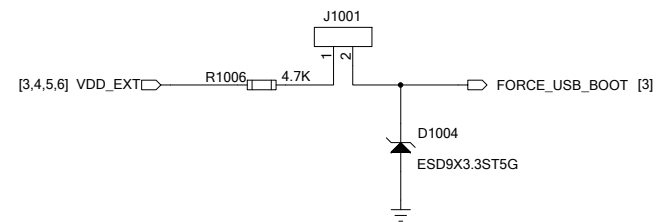
## Reserved Test Points



### Notes:

1. The test points for the USB and debug UART are reserved for getting logs.
2. The USB interface can also be used to upgrade firmware.
3. The junction capacitance of the ESD protection components on USB data lines should be less than 2pF.
4. The debug UART interface supports 1.8V power domain, and a level translator should be used if the power domain of customers' application is 3.3V.

## Emergency Download



### Notes:

1. It is recommended to reserve the FORCE\_USB\_BOOT interface design.
2. FORCE\_USB\_BOOT is kept open by default. When it is at a high level, the module will enter download mode.

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