1 GHz to 11 GHz, GaAs, HEMT, MMIC Low Noise Amplifier

Data Sheet **HMC753**

FEATURES

- Noise figure: 1.5 dB at 4 GHz (see Figure 10)
- Gain
  - 16.5 dB at 1 GHz to 6 GHz
  - 14 dB at 6 GHz to 11 GHz
- Output power for 1 dB compression (P1dB): 18 dBm at 1 GHz to 6 GHz
- Supply voltage (V_{DD}): 5 V at 55 mA
- Output third-order intercept (IP3): 30 dBm at 1 GHz to 6 GHz
- 50 Ω matched input/output (I/O)
- 24-lead lead frame chip scale package (LFCSP): 16 mm²

APPLICATIONS

- Point to point radios
- Point to multipoint radios
- Military and space
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

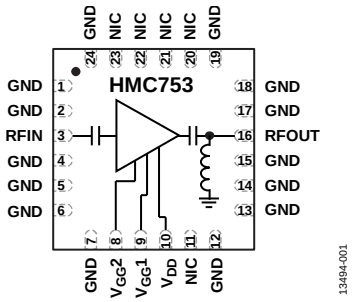

Figure 1.

GENERAL DESCRIPTION

The HMC753 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), low noise, wideband amplifier housed in a leadless, 4 mm × 4 mm LFCSP. The amplifier operates between 1 GHz and 11 GHz, providing up to 16.5 dB of small signal gain at 1 GHz to 6 GHz, a 1.5 dB noise figure at 4 GHz (see Figure 10), and an output IP3 of 30 dBm at 1 GHz to 6 GHz, while requiring only 55 mA from a 5 V supply.

The P1dB output power of up to 18 dBm at 1 GHz to 6 GHz enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for balanced, I/Q, or image rejection mixers. The HMC753 also features I/Os that are dc blocked and internally matched to 50 Ω, making the device ideal for high capacity microwave radios or very small aperture terminal (VSAT) applications.

Rev. E
Document Feedback

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This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

9/2015—Rev. 03.0111 to Rev. D

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 55 mA.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		6	GHz	
PERFORMANCE					
Gain	14	16.5		dB	
Gain Variation over Temperature		0.004		dB/°C	
Noise Figure		1.5	2	dB	
Input Return Loss		11		dB	
Output Return Loss		18		dB	
Output Power for 1 dB Compression (P1dB)		18		dBm	
Saturated Output Power (P_{SAT})		20		dBm	
Output Third Order Intercept (IP3)		30		dBm	
POWER SUPPLY					
Supply Current (I_{DD})		55		mA	V_{DD} = 5 V, set $V_{GG}2$ = 1.5 V, $V_{GG}1$ = −0.8 V typical

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	6		11	GHz	
PERFORMANCE					
Gain	10	14		dB	
Gain Variation over Temperature		0.008		dB/°C	
Noise Figure		2	2.7	dB	
Input Return Loss		8		dB	
Output Return Loss		12		dB	
Output Power for 1 dB Compression (P1dB)		15		dBm	
Saturated Output Power (P_{SAT})		17		dBm	
Output Third Order Intercept (IP3)		28		dBm	
POWER SUPPLY					
Supply Current (I_{DD})		55		mA	V_{DD} = 5 V, set $V_{GG}2$ = 1.5 V, $V_{GG}1$ = −0.8 V typical

ABSOLUTE MAXIMUM RATINGS

Table 3.

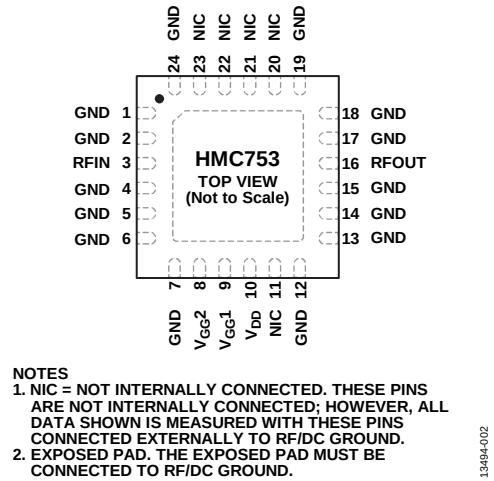
Parameter	Rating
Drain Bias Voltage	6.0 V
RF Input Power	12 dBm
Gate Bias Voltage	
$V_{GG}1$	−1.4 V to +0.3 V
$V_{GG}2$	0 V to 2.5 V
Channel Temperature	180°C
Continuous P_{DISS} (T_A) = 85°C), Derate	
8.4 mW/°C Above 85°C	0.8 W
Thermal Resistance (Channel to Die	
Bottom)	119°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity	
Human Body Model (HBM)	Class 0, Passed 100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT INTERNALLY CONNECTED; HOWEVER, ALL DATA SHOWN IS MEASURED WITH THESE PINS CONNECTED EXTERNALLY TO RF/DC GROUND.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 12 to 15, 17 to 19, 24	GND	Ground. The package bottom has an exposed metal pad that must be connected to RF/dc ground.
3	RFIN	RF Input. This pad is ac-coupled and matched to 50 Ω.
8, 9	$V_{GG}2$, $V_{GG}1$	Gate Control for the Amplifier. Follow the biasing procedures described in the Biasing Procedure section. See Figure 23 for required external components.
10	V_{DD}	Power Supply Voltage for the Amplifier. See Figure 23 for required external components.
11, 20 to 23	NC	Not Internally Connected. These pins are not internally connected; however, all data shown is measured with these pins connected externally to RF/dc ground.
16	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

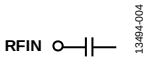


Figure 4. RFIN Interface

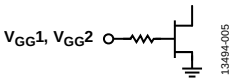


Figure 5. $V_{GG}1$, $V_{GG}2$ Interface

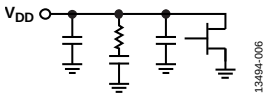


Figure 6. V_{DD} Interface

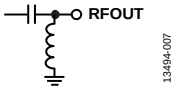


Figure 7. RFOUT Interface

TYPICAL PERFORMANCE CHARACTERISTICS

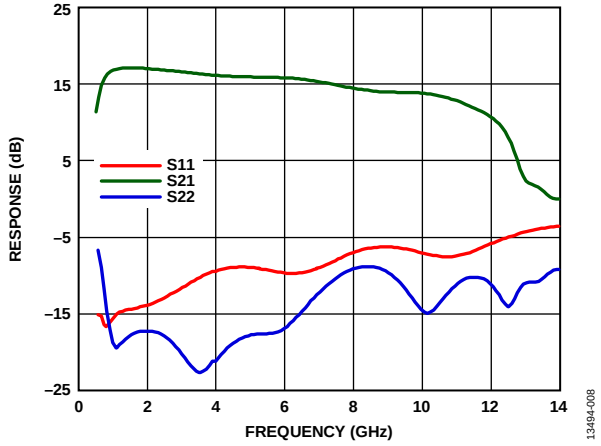


Figure 8. Broadband Gain and Return Loss (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

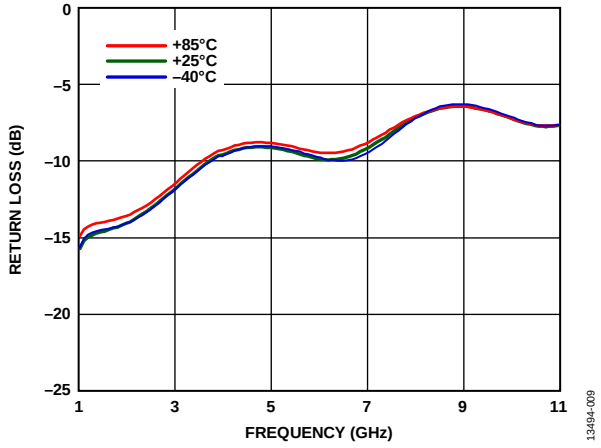


Figure 9. Input Return Loss vs. Frequency for Various Temperatures

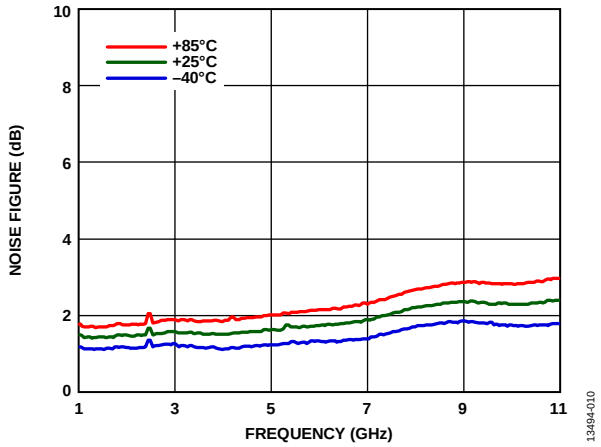


Figure 10. Noise Figure vs. Frequency for Various Temperatures (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

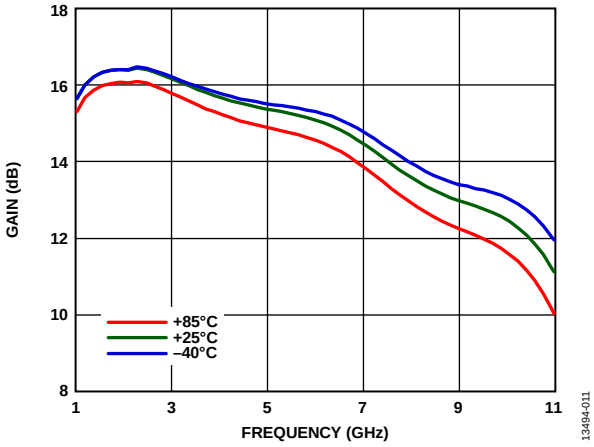


Figure 11. Gain vs. Frequency for Various Temperatures (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

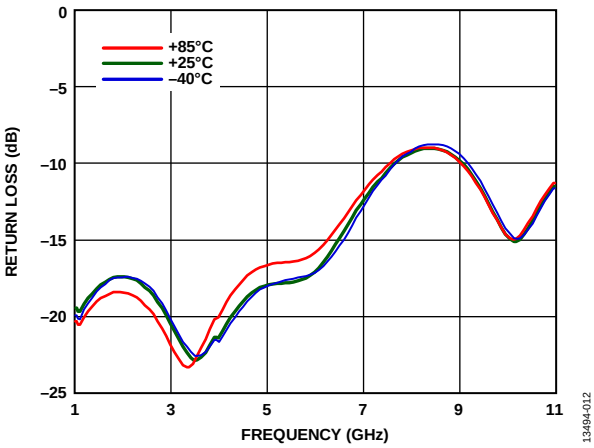


Figure 12. Output Return Loss vs. Frequency for Various Temperatures

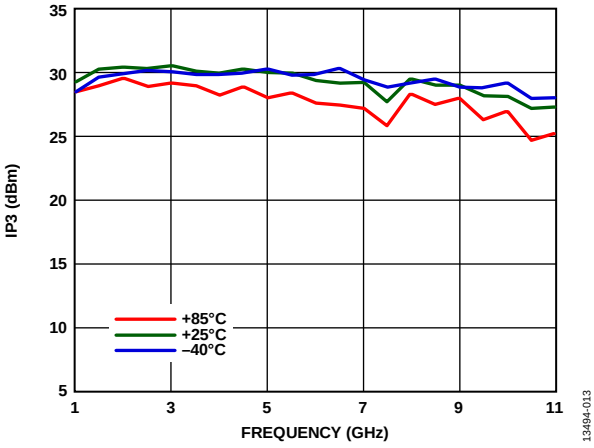


Figure 13. Output IP3 vs. Frequency for Various Temperatures

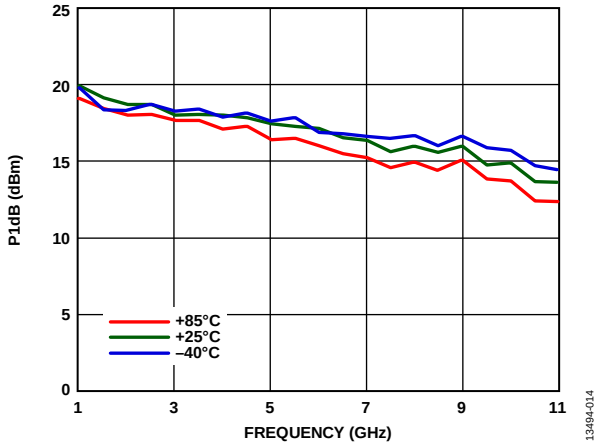


Figure 14. P1dB vs. Frequency for Various Temperatures (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

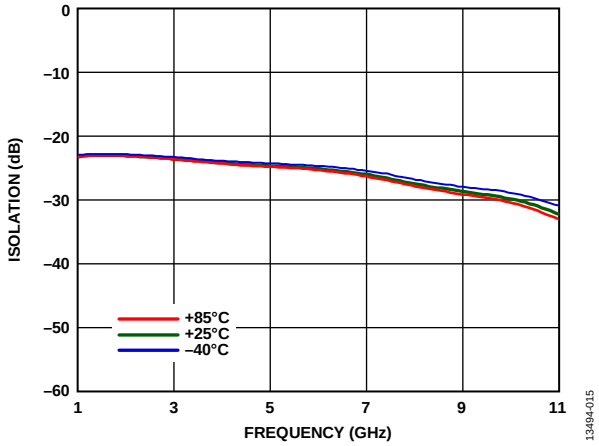


Figure 15. Reverse Isolation vs. Frequency for Various Temperatures

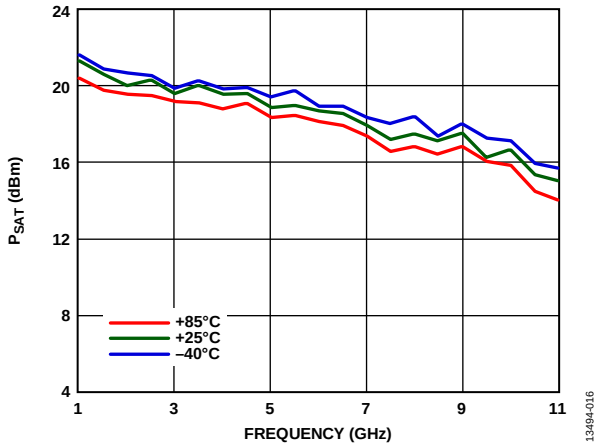


Figure 16. P_{SAT} vs. Frequency for Various Temperatures (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

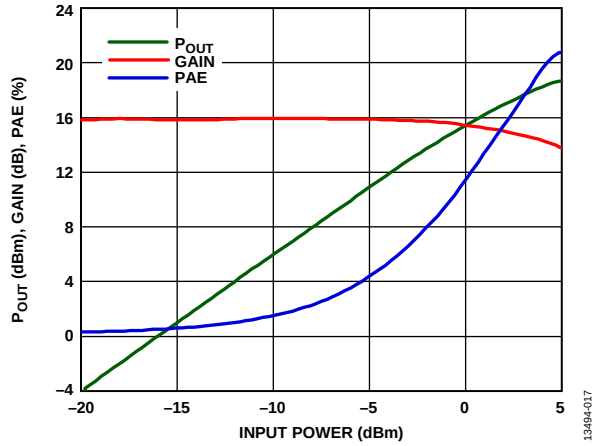


Figure 17. Power Compression at 6 GHz (Board Loss Subtracted out for Gain, Power, and Noise Figure Measurements)

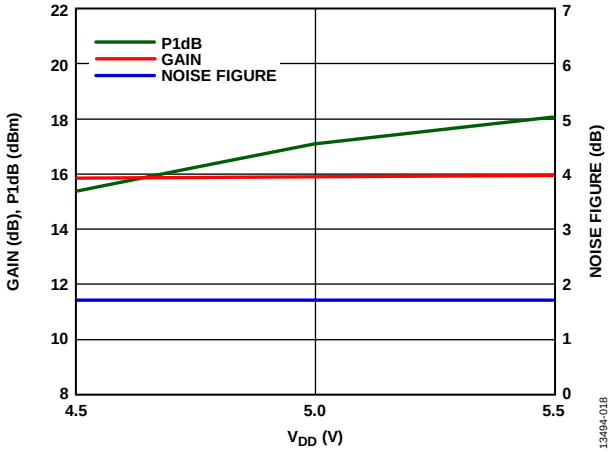


Figure 18. Gain, Noise Figure, and Power vs. Supply Voltage (V_{DD}) at 6 GHz (Board Loss Subtracted out for Gain, P1dB, and Noise Figure Measurements)

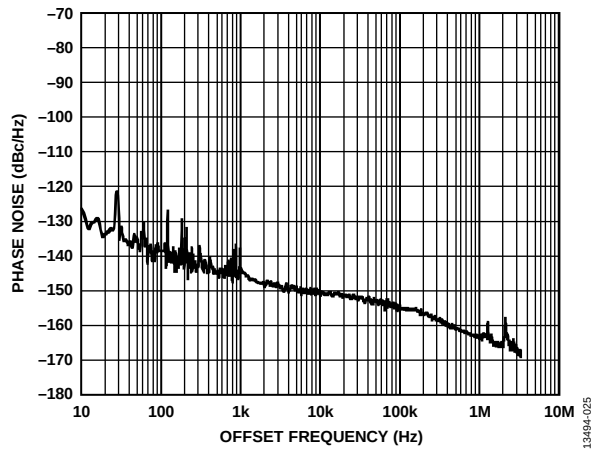


Figure 19. Additive Phase Noise vs. Offset Frequency, RF Frequency = 8 GHz, RF Input Power = 12 dBm (P_{SAT})

THEORY OF OPERATION

The circuit architecture of the HMC753 wideband, low noise amplifier is shown in Figure 20. The HMC753 uses a single gain stage to form an amplifier with typical gain of 16.5 dB at 1 GHz to 6 GHz and 14 dB at the 6 GHz to 11 GHz frequency band.

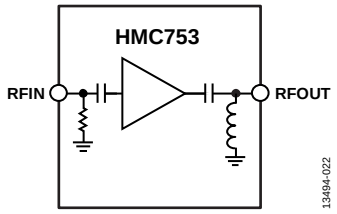


Figure 20. Wideband Low Noise Amplifier Circuit Architecture

The HMC753 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the frequency range of 1 GHz to 11 GHz. Consequently, the HMC753 can be directly inserted into a 50 Ω system with no impedance matching circuitry required. In addition, multiple HMC753 amplifiers can be cascaded back to back without the need of external matching circuitry.

The input and output impedances are sufficiently stable over variations in temperature and supply voltage that no impedance matching compensation is required.

Both RF input and RF output ports have on-chip dc block capacitors, which eliminates the need for external ac coupling capacitors.

It is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed paddle. This ensures stable operation.

To achieve the best performance out of the HMC753 and not to damage the device, the recommended biasing sequence must be followed; see the Applications Information section for further details.

APPLICATIONS INFORMATION

The HMC753 is a GaAs, MMIC, high electron mobility transistor (HEMT), low noise, wideband amplifier.

The amplifier uses two field effect transistors (FETs) in series, source to drain. The basic schematic for a fundamental cell is shown in Figure 21.

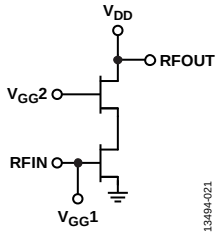


Figure 21. Fundamental Cell Schematic

All measurements for this device are taken using the evaluation printed circuit board (PCB) in its default configuration.

BIASING PROCEDURES

The recommended biasing procedure during power-up is as follows:

1. Connect GND.
2. Set $V_{GG}1$ to −1 V.
3. Set V_{DD} to 5 V.
4. Set $V_{GG}2$ to 1.5 V.
5. Increase $V_{GG}1$ to achieve a typical quiescent current (I_{DQ}) = 55 mA.
6. Apply the RF signal.

The recommended biasing procedure during power-down is as follows:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −1 V to achieve I_{DQ} = 0 mA.
3. Decrease $V_{GG}2$ to 0 V.
4. Decrease V_{DD} to 0 V.
5. Increase $V_{GG}1$ to 0 V.

The V_{DD} = 5 V and I_{DQ} = 55 mA bias conditions are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown is taken using the recommended bias conditions. Operation of the HMC753 at different bias conditions may result in performance that differs from the Typical Performance Characteristics shown in the data sheet. Biasing the HMC753 for higher drain current typically results in higher P1dB and output IP3 at the expense of increased power consumption.

EVALUATION PCB

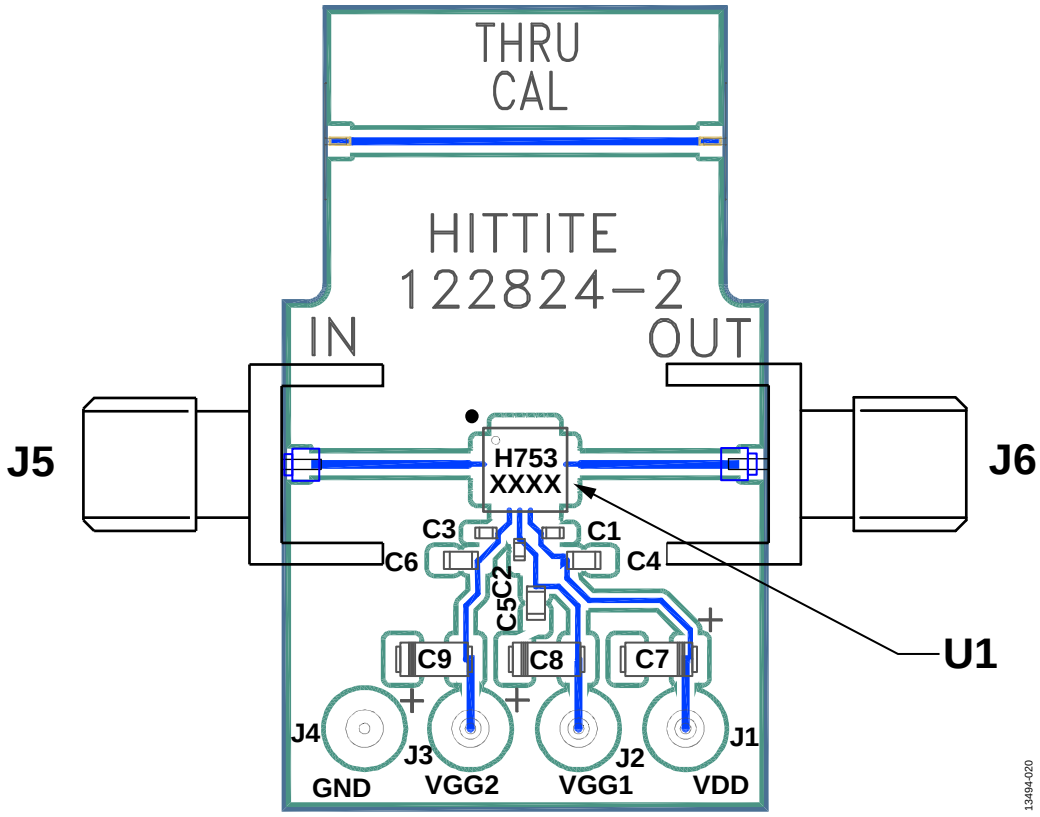


Figure 22. 122826-HMC753LP4E Evaluation PCB

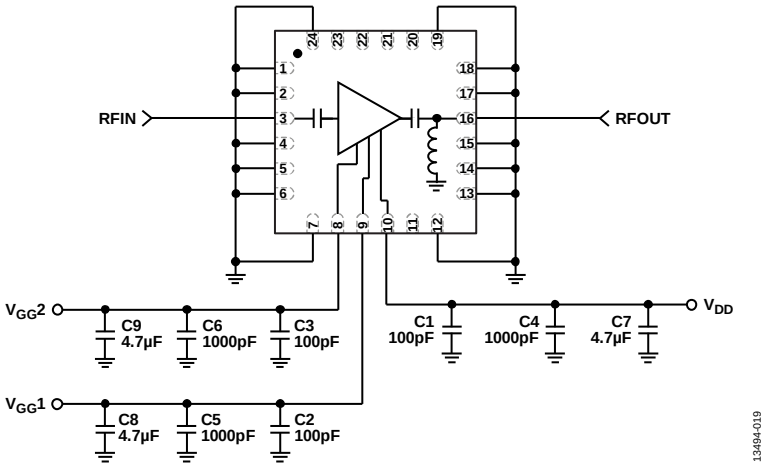


Figure 23. Typical Application Circuit

Table 5. List of Materials for Evaluation PCB 122826-HMC753LP4E[1]

Item	Description
J5, J6	SMA connectors
J1 to J4	DC pins
C1 to C3	100 pF capacitors, 0402 package
C4 to C6	10,000 pF capacitors, 0603 package
C7 to C9	4.7 µF capacitors, tantalum
U1	HMC753 amplifier
PCB[2]	122824-2 evaluation PCB

[1] Reference this number when ordering the complete evaluation PCB.
[2] Circuit board material: Rogers 4350 or Arlon 25FR.

It is recommended that the circuit board used in this application use RF circuit design techniques. It is also recommended that signal lines have a 50 Ω impedance, and the package ground leads and exposed pad be connected directly to the ground plane, as shown in Figure 23. Use a sufficient number of via holes to connect the top and bottom ground planes. Mount the evaluation board to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices, Inc., upon request.

OUTLINE DIMENSIONS

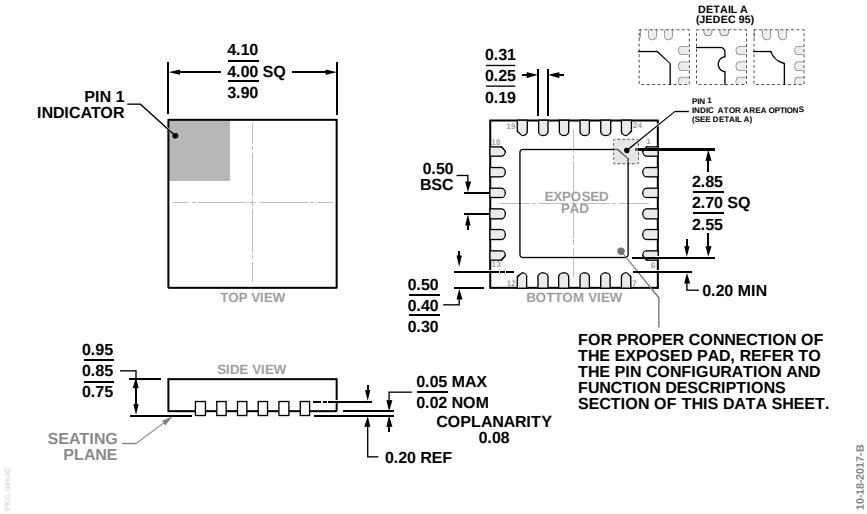


Figure 24. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(HCP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating	Package Description	Package Option
HMC753LP4E	−40°C to +85°C	MSL1	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	HCP-24-3
HMC753LP4ETR	−40°C to +85°C	MSL1	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	HCP-24-3
122826-HMC753LP4E			Evaluation Board	

[1] All models are RoHS Compliant Parts.

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