



FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
 Operating : 40/30 mA (typical.)
 Standby : 3mA (typical) normal
 2uA (typical) L-version
 1uA (typical) LL-version
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 28-pin 600 mil PDIP
 28-pin 330 mil SOP
 28-pin 8mmx13.4mm STSOP

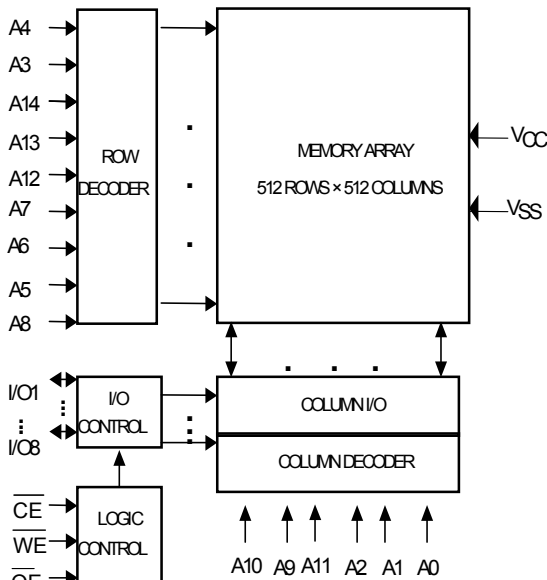
GENERAL DESCRIPTION

The UT62256C is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT62256C is designed for high-speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62256C operates from a single 5V power supply and all inputs and outputs are fully TTL compatible

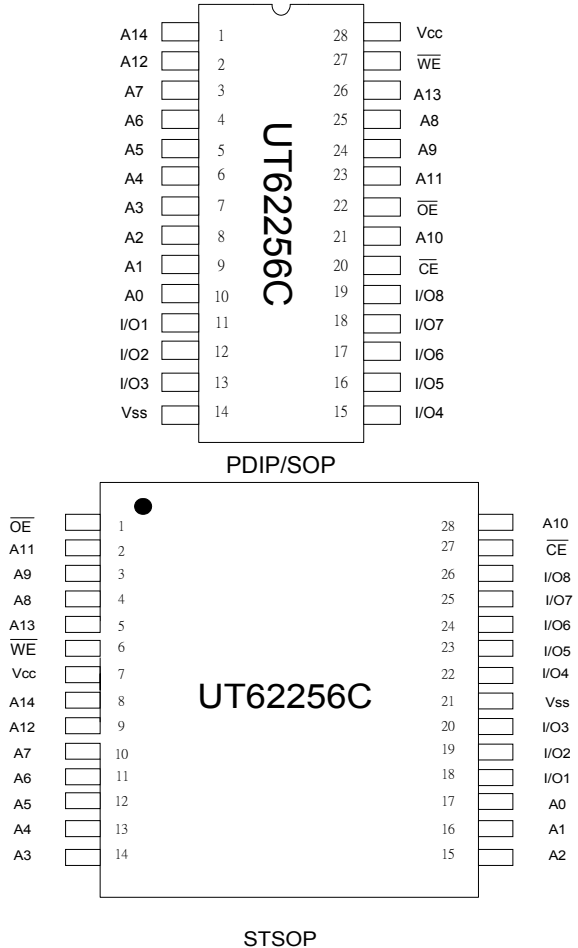
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground

PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec0	T_{solder}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	ISB, ISB1
Output Disable	L	H	H	High - Z	I_{CC}
Read	L	L	H	D_{OUT}	I_{CC}
Write	L	X	L	D_{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Input High Voltage	V_{IH}		2.2	-	$V_{CC} + 0.5$	V	
Input Low Voltage	V_{IL}		-0.5	-	0.8	V	
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	μA	
Output Leakage Current	I_{LO}	$V_{SS} \leq V_{I/O} \leq V_{CC}$ $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.4	-	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4mA$	-	-	0.4	V	
Operating Power Supply Current	I_{CC}	$\overline{CE} = V_{IL}$, $I_{I/O} = 0mA$, Cycle=Min.	-35	-	40	50	mA
			-70	-	30	40	mA
	I_{CC1}	$\overline{CE} = 0.2V$; $I_{I/O} = 0mA$ other pins at 0.2V or $V_{CC} - 0.2V$	Tcycle = 500ns	-	-	20	mA
I_{CC2}	$V_{CC} - 0.2V$	Tcycle = 1ms	-	-	10	mA	
Standby Power Supply Current	I_{SB}	$\overline{CE} = V_{IH}$	normal	-	1	10	mA
	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$			0.3	5	mA
	I_{SB}	$\overline{CE} = V_{IH}$	-L/-LL	-	-	3	mA
	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	-L	-	2	100	μA
-LL			-	1	50	μA	

**CAPACITANCE** (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 100pF, I _{OH} /I _{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (VCC = 5V±10% , TA = 0°C to 70°C)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62256C-35		UT62256C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	35	ns
Chip Enable to Output in Low Z	t _{CLZ*}	10	-	10	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High Z	t _{CHZ*}	-	25	-	35	ns
Output Disable to Output in High Z	t _{OHZ*}	-	25	-	35	ns
Output Hold from Address Change	t _{OH}	5	-	5	-	ns

(2) WRITE CYCLE

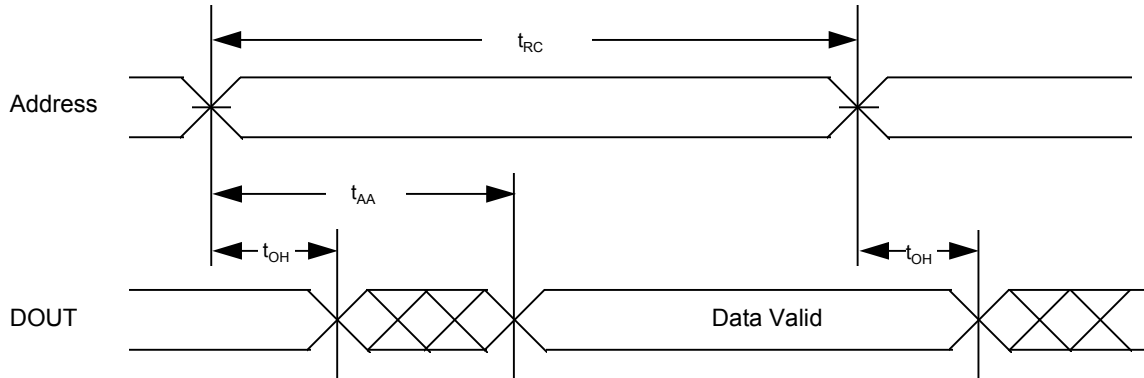
PARAMETER	SYMBOL	UT62256C-35		UT62256C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	50	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	5	-	5	-	ns
Write to Output in High Z	t _{WHZ*}	-	15	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

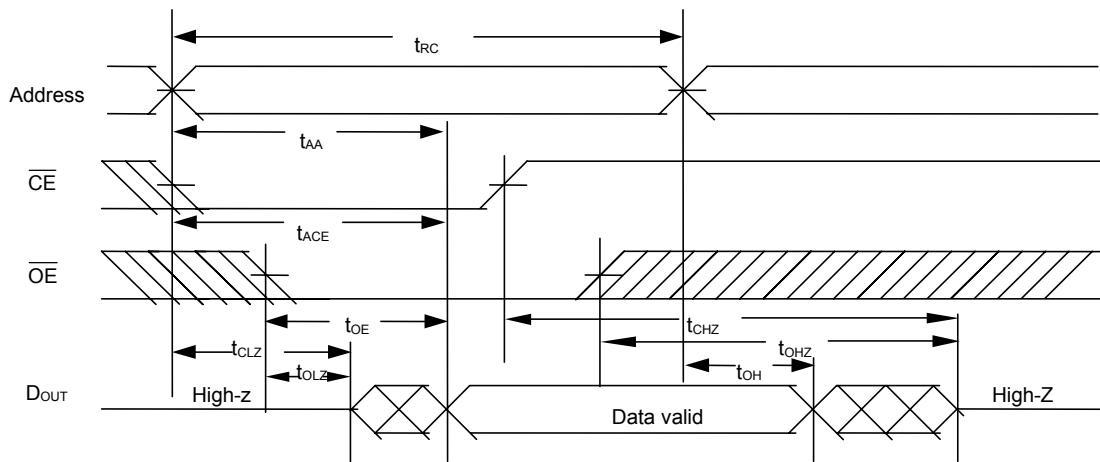


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,5,6)

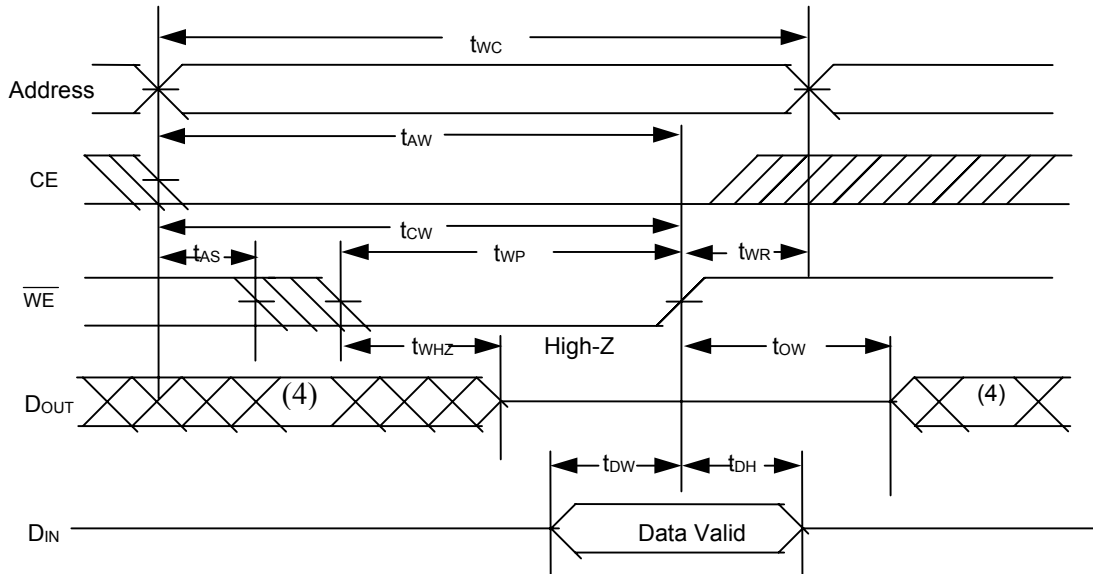


Notes :

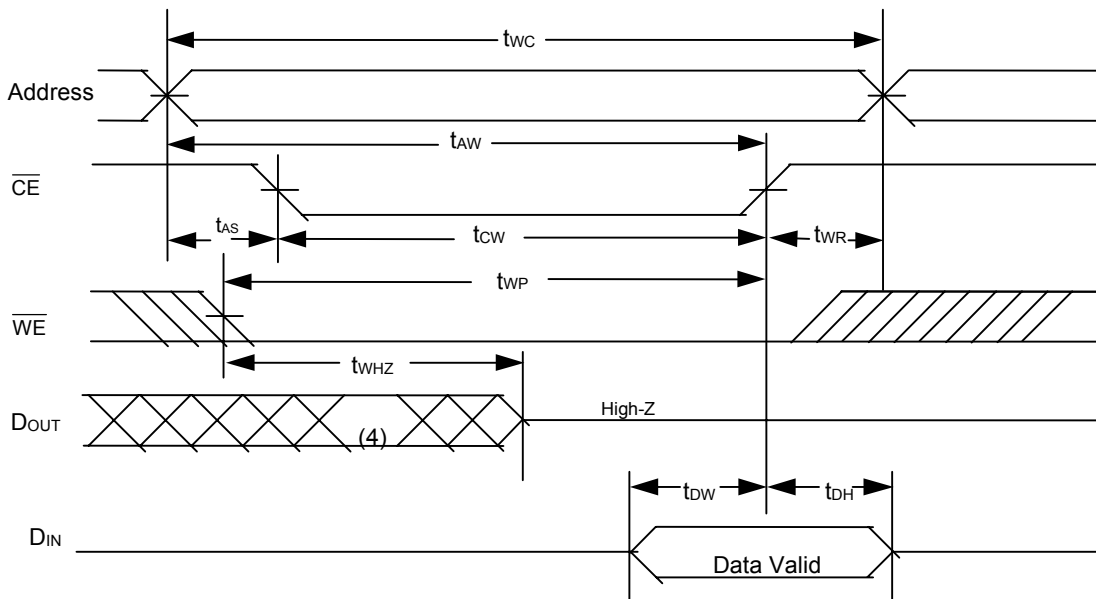
1. \overline{WE} is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with \overline{CE} transition; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5)



WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5)



Notes :

1. \overline{WE} or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} and a low \overline{WE} .
3. During a \overline{WE} controlled write cycle with \overline{OE} LOW, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} LOW transition occurs simultaneously with or after \overline{WE} LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

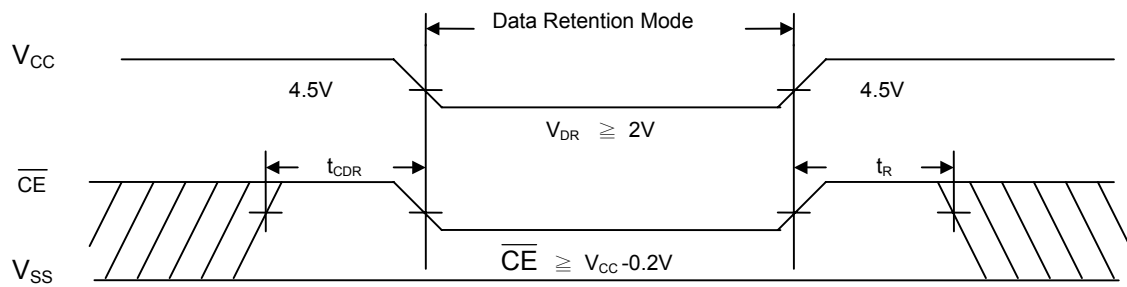


DATA RETENTION CHARACTERISTICS (TA = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	$\overline{CE} \geq V_{CC}-0.2V$	2.0	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} =3V $\overline{CE} \geq V_{CC}-0.2V$	- L	-	1	50	μA
			- LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC*}	-	-	ns	

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM





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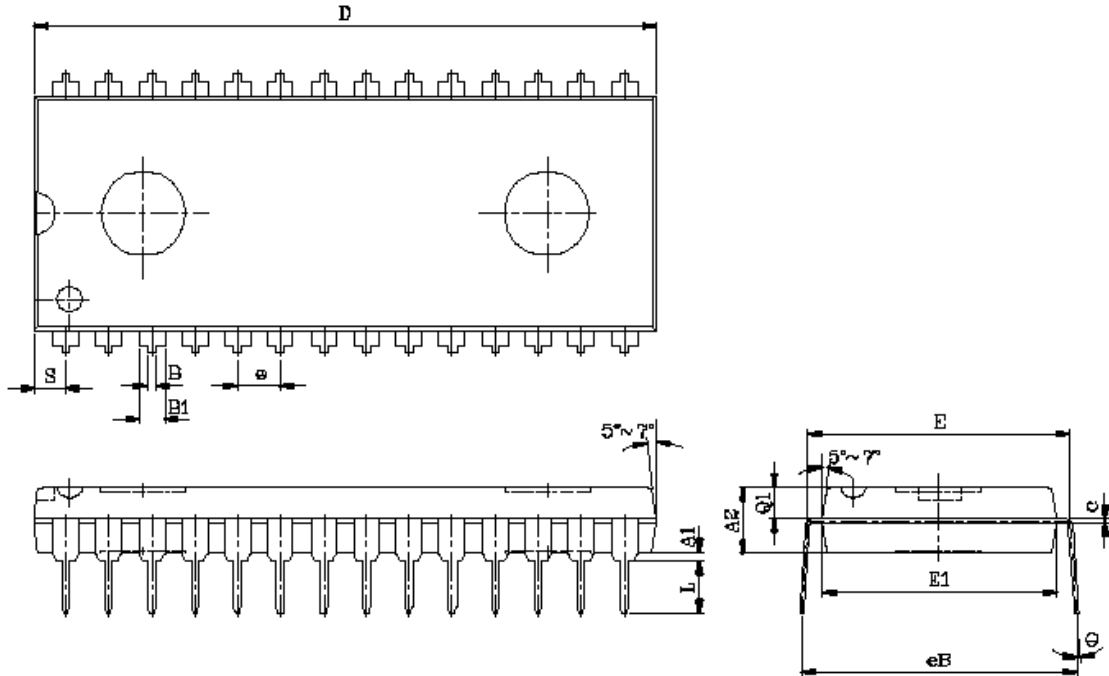
UT62256C

Rev. 1.0

32K X 8 BIT LOW POWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP PACKAGE OUTLINE DIMENSION



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150±0.005	3.810±0.127
B	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
c	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.6 (TYP)	15.24 (TYP)
E1	0.52 (MAX)	13.208 (MAX)
e	0.100 (TYP)	2.540(TYP)
eB	0.625 (MAX)	15.87 (MAX)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
θ	15°(MAX)	15°(MAX)



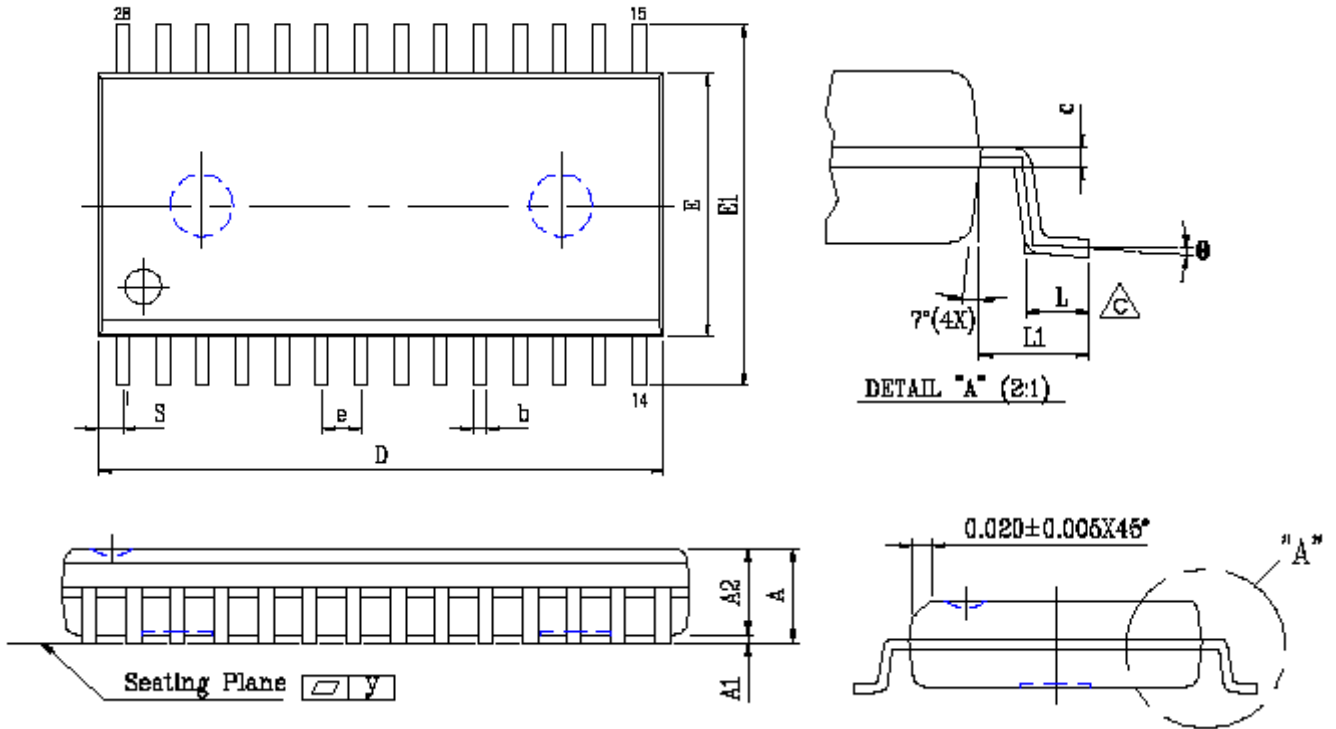
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Rev. 1.0

32K X 8 BIT LOW POWER CMOS SRAM

28 pin 330 mil SOP PACKAGE OUTLINE DIMENSION

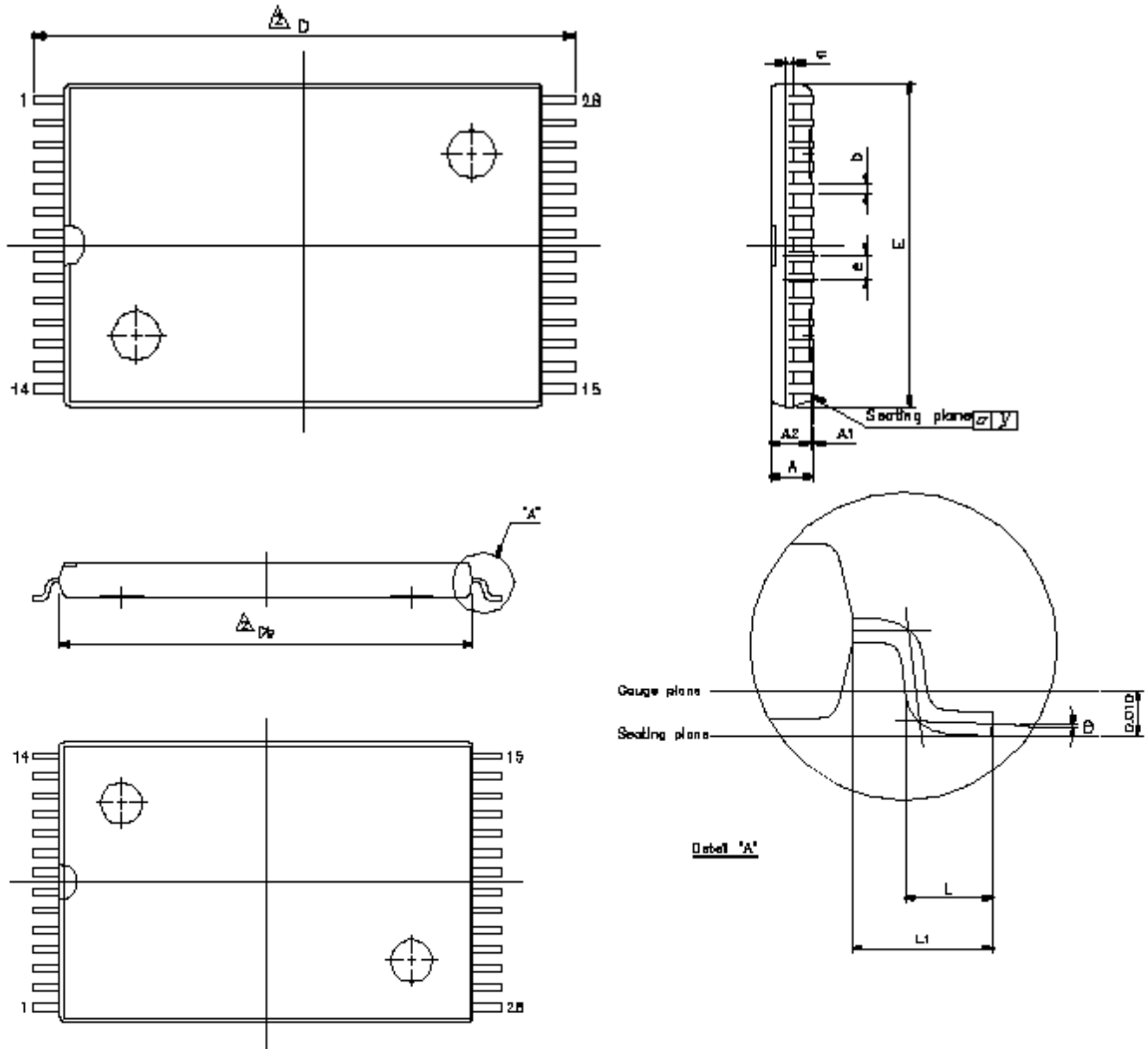


SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.120 (MAX)	3.048 (MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.0016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.728 (MAX)	18.491 (MAX)
E	0.340 (MAX)	8.636 (MAX)
E1	0.465±0.012	11.811±0.305
e	0.050 (TYP)	1.270(TYP)
L	0.05 (MAX)	1.270 (MAX)
L1	0.067±0.008	1.702 ±0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
θ	0°~10°	0°~10°





28 pin 8x13.4mm STSOP PACKAGE OUTLINE DIMENSION



Note :
E dimension is not including end flash
the total of both sides' end flash is
not above 0.3mm.



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.006 (TYP)	0.15(TYP)
c	0.010 (TYP)	0.254(TYP)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.08(MAX)	0.003(MAX)
θ	0°~5°	0°~5°



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Rev. 1.0

32K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A)	PACKAGE
UT62256CPC-70	70	5 mA	28PIN PDIP
UT62256CPC-70L	70	100 μ A	28PIN PDIP
UT62256CPC-70LL	70	40 μ A	28PIN PDIP
UT62256CSC-35	35	5 mA	28PIN SOP
UT62256CSC-35L	35	100 μ A	28PIN SOP
UT62256CSC-35LL	35	40 μ A	28PIN SOP
UT62256CSC-70	70	5 mA	28PIN SOP
UT62256CSC-70L	70	100 μ A	28PIN SOP
UT62256CSC-70LL	70	40 μ A	28PIN SOP
UT62256CLS-35L	35	100 μ A	28PIN STSOP
UT62256CLS-35LL	35	50 μ A	28PIN STSOP
UT62256CLS-70L	70	100 μ A	28PIN STSOP
UT62256CLS-70LL	70	40 μ A	28PIN STSOP



Rev. 1.0

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UT62256C
32K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	DATE
REV. 0.9	1. Original.	Apr. 26,2001
REV. 1.0	1. The test condition of I_{CC1} and I_{CC2} have been revised. 2. The symbols CE#,OE# and WE# are revised as \overline{CE} , \overline{OE} and \overline{WE} 3. The ordering information of PACKAGE ,STSOP-1 is revised as STSOP.	MAY. 14,2001



Rev. 1.0

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