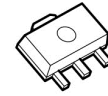


## ADJUSTABLE PRECISION SHUNT REGULATOR

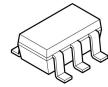
### ■ GENERAL DESCRIPTION

The NJM431S/NJM432S are adjustable precision shunt regulators. The output voltage may be set to any value between  $V_{REF}$  (about 2.5V) and 36V by two resistors. Compared to the conventional 431, the NJM431S/NJM432S are improved the voltage accuracy. And they have smaller package option to support a wide range of applications. The NJM432S is the pin assignment option.

### ■ PACKAGE OUTLINE



NJM431SU  
NJM432SU  
(SOT-89-3)



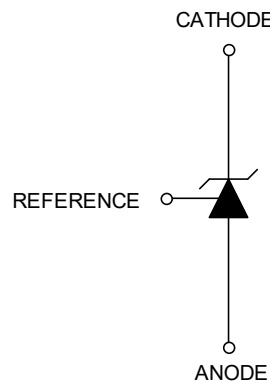
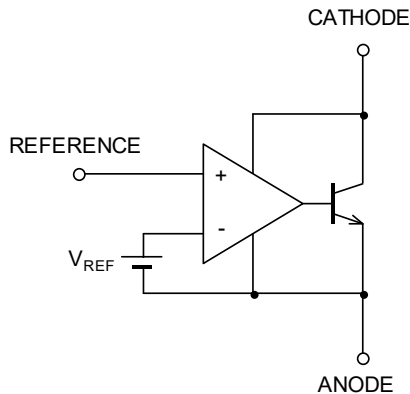
NJM431SF  
NJM432SF  
(SOT-23-5)

### ■ FEATURES

- Operating Voltage  $V_{REF}$  to 36V
- Precision Voltage Reference  $2.495 \pm 1.8\%$
- Adjustable Output Voltage
- Bipolar Technology
- Package Outline
 

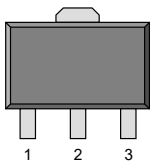
NJM431SU / NJM432SU	SOT-89-3
NJM431SF / NJM432SF	SOT-23-5

### ■ BLOCK DIAGRAM / SYMBOL



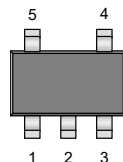
### ■ PIN CONFIGURATION

NJM431SU



- 1.REFERENCE
- 2.ANODE
- 3.CATHODE

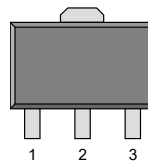
NJM431SF



- 1.N.C.
- 2.ANODE\*
- 3.CATHODE
- 4.REFERENCE
- 5.ANODE

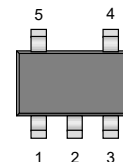
\* Pin 2 is attached to Substrate and must be connected to ANODE or left open.

NJM432SU



- 1.CATHODE
- 2.ANODE
- 3.REFERENCE

NJM432SF



- 1.N.C.
- 2.ANODE
- 3.N.C.
- 4.CATHODE
- 5.REFERENCE

# NJM431S/NJM432S

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=25^\circ\text{C}$ )

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Cathode Voltage	$V_{KA}$	37 (*1)	V
Continuous Cathode Current	$I_K$	-100 to 150	mA
Reference Input Current	$I_{REF}$	-0.05 to 10	mA
Power Dissipation	$P_D$	SOT-89-3 : 625(*2) : 1300(*3)	mW
		SOT-23-5 : 480(*4) : 650(*5)	
Operating Temperature Range	$T_{opr}$	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-50 to +150	$^\circ\text{C}$

(\*1) Unless specified, all voltage value are with respect to the anode pin.

(\*2) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 2Layers, Cu area 100mm<sup>2</sup>)

(\*3) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(\*4) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 2Layers)

(\*5) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 4Layers),

internal Cu area: 74.2 × 74.2mm

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cathode Voltage	$V_{KA}$	$V_{REF}$	-	36	V
Cathode Current	$I_K$	0.7	-	100	mA

## ■ ELECTRICAL CHARACTERISTICS

( $I_K=10\text{mA}$ ,  $T_a=25^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	$V_{REF}$	$V_{KA}=V_{REF}$ (*6)	2450	2495	2540	mV
Reference Input Voltage Change Over Temperature Range	$\Delta V_{REF}$ (dev)	$V_{KA}=V_{REF}$ (*6) $T_a=-40^\circ\text{C}$ to $+85^\circ\text{C}$	-	8	17	mV
Reference Voltage Change vs. Cathode Voltage Change	$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	(*7) $\Delta V_{KA}=10\text{V}-V_{REF}$ $\Delta V_{KA}=36\text{V}-10\text{V}$	-	-1.4 -1	-2.7 -2	mV/V
Reference Input Current	$I_{REF}$	$R1=10\text{k}\Omega$ , $R2=\infty$ (*7)	-	2	4	$\mu\text{A}$
Reference Input Current Change Over Temperature Range	$\Delta I_{REF}$ (dev)	$R1=10\text{k}\Omega$ , $R2=\infty$ (*7) $T_a=-40^\circ\text{C}$ to $+85^\circ\text{C}$	-	0.4	1.2	$\mu\text{A}$
Minimum Cathode Current	$I_{MIN}$	$V_{KA}=V_{REF}$ (*6)	-	0.4	0.7	mA
OFF State Cathode Current	$I_{OFF}$	$V_{KA}=36\text{V}$ , $V_{REF}=0\text{V}$ (*8)	-	0.1	1.0	$\mu\text{A}$
Dynamic Impedance	$ Z_{KA} $	$V_{KA}=V_{REF}$ , $I_K=1\text{mA}$ to $100\text{mA}$ , $f \leq 1\text{kHz}$ (*6)	-	0.2	0.5	$\Omega$

The maximum value of “Dynamic Impedance“, “Reference Voltage Change” and “Reference Input Current Change” are determined based on sampling evaluation from the initial production lots, and thus not tested in the production test. Therefore, these values are for the reference design purpose only.

(\*6) Test Circuit Fig.1

(\*7) Test Circuit Fig.2

(\*8) Test Circuit Fig.3

## ■ TEST CIRCUIT

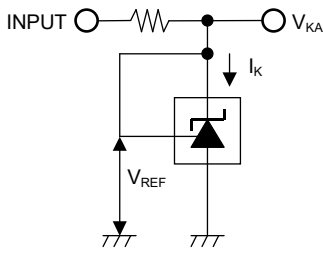


Fig.1 Test Circuit for  $V_{KA} = V_{REF}$

$$V_O = V_{KA} = V_{REF}$$

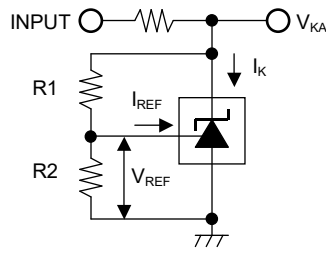


Fig. 2 Test Circuit for  $V_{KA} > V_{REF}$

$$V_O = V_{KA} = V_{REF} \left( 1 + \frac{R1}{R2} \right) + I_{REF} \times R1$$

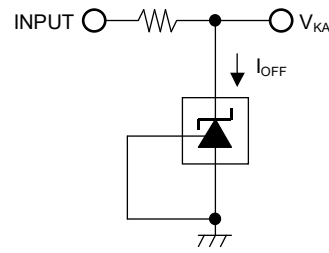
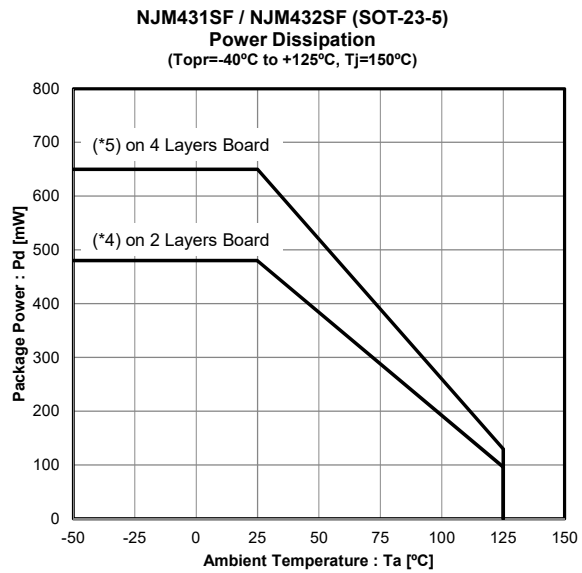
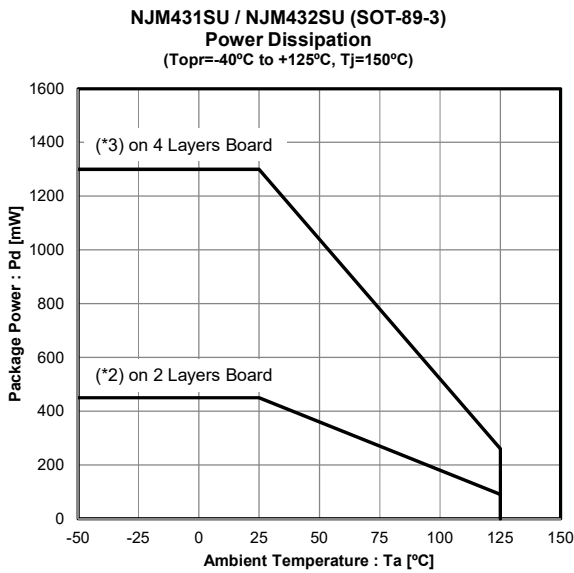


Fig.3 Test Circuit for  $I_{OFF}$

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



(\*2) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 2Layers)

(\*3) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

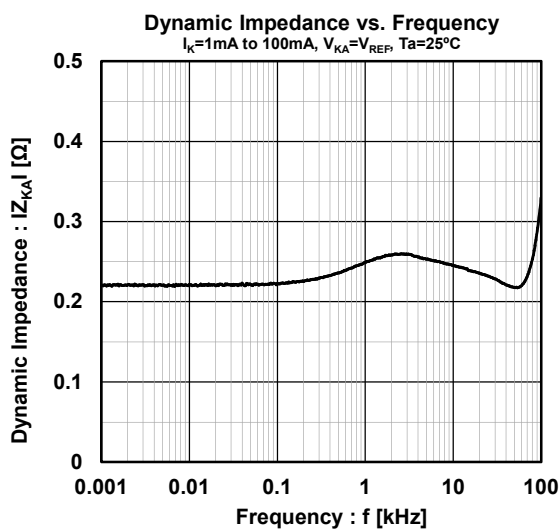
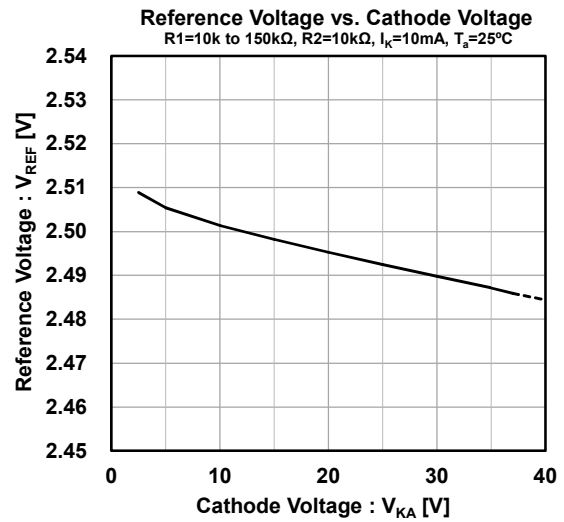
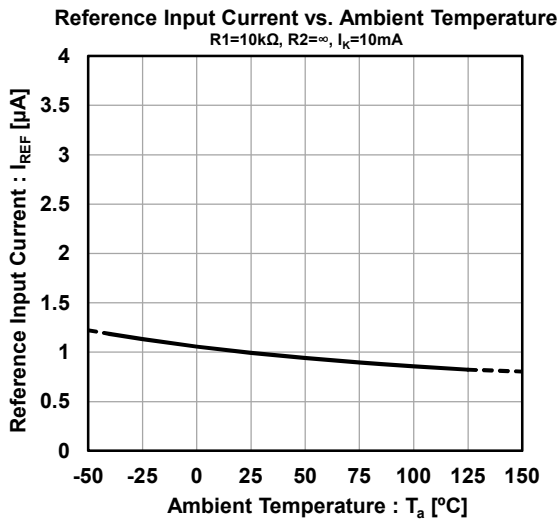
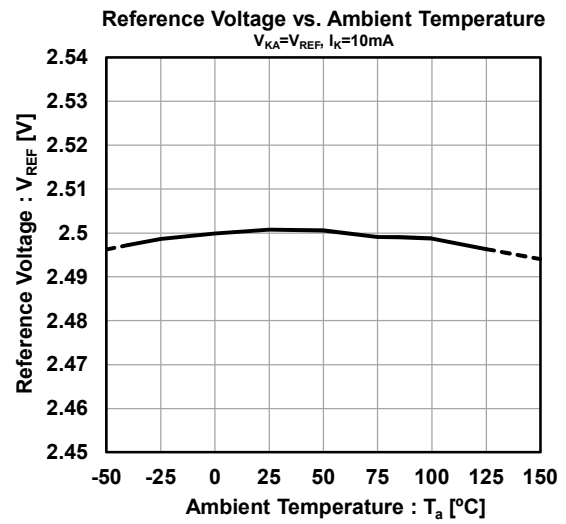
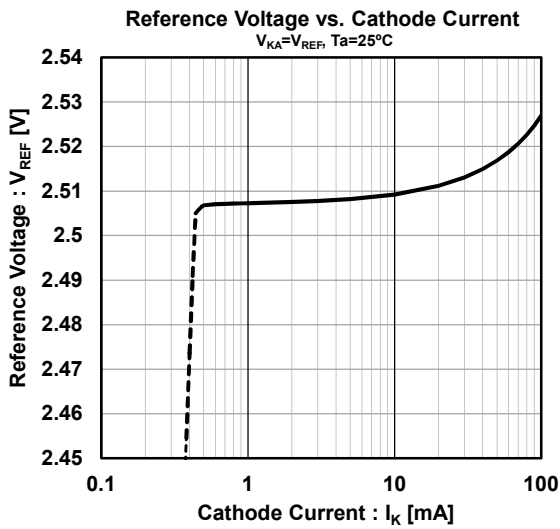
(\*4) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 2Layers)

(\*5) Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm: EIA/JEDEC standard size, 4Layers),

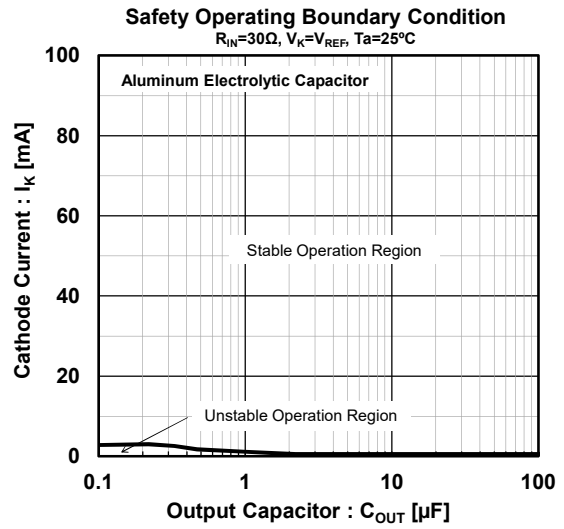
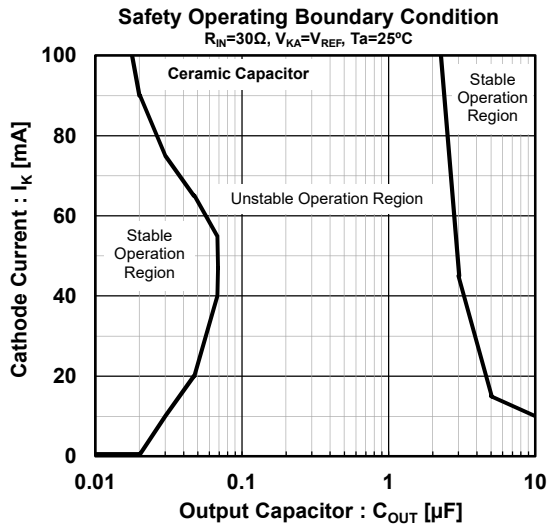
internal Cu area: 74.2 × 74.2mm

# NJM431S/NJM432S

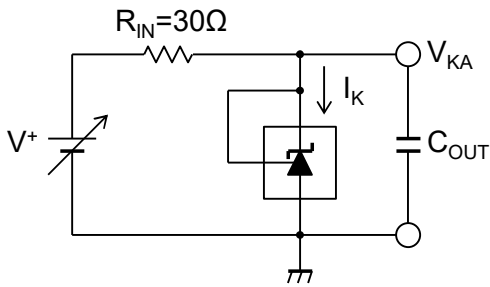
## TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS



### Safety Operating Boundary Condition Test Circuit



Note) Oscillation might occur while operating within the range of safety curve.

So that, it is necessary to make ample margins by taking considerations of fluctuation of the device.

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