Embedded MMC

EMC410T

Datasheet

Products

TS32GEMC410T

Product Description

32GB, eMMC 5.1, 3D TLC

Datasheet version

1.0

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Revision History

Revision No.	History	Released Date	Editor by
1.0	First version	2023/11/14	PM

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Transcend EMC410T Features

Part Name	Capacity
TS32GEMC410T	32GB

Features

- JEDEC e.MMC Standard Ver. 5.1 compliant
- Data bus widths: 1bit, 4bit, 8bit.
- Uses an embedded thin memory controller and 3D TLC NAND flash
- SLC mode (optional)
- Mechanical design complies with JESD21-C Specification
- Dual power system
- Core voltage (VCC) 2.7-3.6V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
- Variable clock frequencies of 0-200 MHz
- Static global wear leveling
- ECC engine: LDPC
- Fully cycle environment test
- RoHS compliant

PERFORMANCE[1)]

- Data Transfer Rate
  - Sequential Read Up to 290 MB/s
  - Sequential Write Up to 155 MB/s

RELIABILITY[1)]

- MTBF 34,789,616 hours
- Data Retention 10 years
- Warranty 3 years

Environmental specifications[1)]

- Operating -25°C to 85°C
- Non-operating -40°C to 85°C

POWER REQUIREMENTS[1)]

- VCC 2.7V-3.6V
- VCCQ (dual voltage) 1.70- 1.95V; 2.7- 3.6V

PHYSICAL DIMENSION

- Width 11.5mm
- Length 13mm
- Height(max) 1mm

Note:
1) All tests are handled by TRANSCEND, the results are affected by different system operations and environments. Data is for reference only.

Table of Content

1.Introduction

1.1 General Feature Information

Hardware Feature

- Compliant with JEDEC e.MMC Specification Ver. 5.1
- Data bus widths: 1bit, 4bit, 8bit.
- Uses an embedded thin memory controller and 3D TLC NAND flash
- Mechanical design complies with JESD21-C Specification
- Dual power system
- Core voltage (VCC) 2.7-3.6V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
- Variable clock frequencies of 0-200 MHz
- Static global wear leveling
- ECC engine: LDPC
- Fully cycle environment test
- RoHS compliant

Firmware Feature

- Field Firmware Update
- Command Queuing
- Secure Erase
- TRIM
- Background Operations
- Data Tag
- SLC mode (optional)

1.2 Product List

[Table 1] Product List

Form Factor	Part Name	Capacity
153-Ball eMMC	TS32GEMC410T	32GB

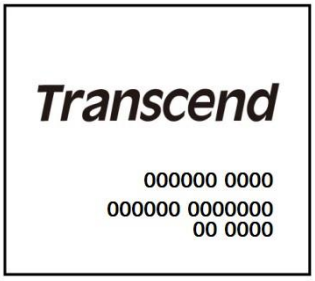
1.3 Ordering Information

T S X X X G E M C 4 1 0 T

1 2 3 4 5

1 – Transcend
2 – eMMC Density
3 – G: Gigabyte; T: Terabyte
4 – eMMC
5 – Product series with 3D TLC NAND Flash

1.4 BGA Laser Marking



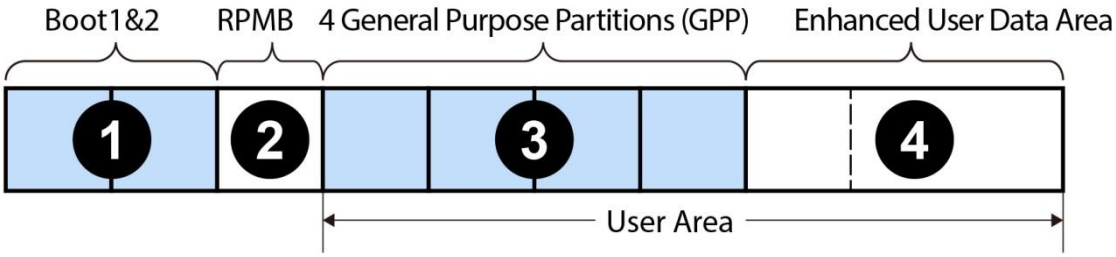
1st row : Transcend LOGO
2nd row : Serial number
3rd row : Internal use
4th row : Country of Origin + Date Code (YYWW)

2.Product Specifications

2.1 Interface and Compliance

- e.MMC Specification Ver. 5.1 Compliant
- RoHS Compliance

2.2 Capacity



[Table 2] Product Capacity

PN	User Area	Max Enhanced Partition Size	Boot 1	Boot 2	RPMB
TS32GEMC410T	31,264,342,016 bytes	10,418,651,136 bytes	4096KB	4096KB	4096KB

Note:

1) User Area: Total free space which could be used by user.
2) If the system has a requirement for preloading, the recommended capacity is Max Enhanced Partiton Size as the upper limit. If there is a requirement that exceeds this capacity, please contact Transcend for discussion

2.3 Performance

[Table 3] Sequential Max. Performance

Mode	Read	Write	Unit
	32GB	32GB	
HS400	290	155	MB/S
HS200	170	140	
DDR52	90	75	

Note: Maximum transfer speed recorded

1) 25°C, test on 8GB DRAM, Windows® 10 benchmark utility Crystal Disk Mark 8.0.4 , copied file 512MB, unit MB/s

[Table 4] Sequential sustaining Performance

Mode	Read	Write	Unit
	32GB	32GB	
HS400	285	25	MB/S
HS200	170	25	
DDR52	90	25	

Note:

1)The test is measured by full disk capacity to record sustaining performance.

2.4 Supply Voltage

[Table 5]DC Operating Parameter

Parameter	Symbol	Min.	Nom.	Max.	Unit
Supply voltage (NAND)	VCC	2.7	3.3	3.6	V
Supply voltage (I/O)	VCCQ	2.7	3.3	3.6	V
		1.7	1.8	1.95	V

2.5 Power Consumption

[Table 6] Peak Power Consumption VCC / VCCQ (3.3/1.8V at 30 degree)

Mode	Symbol	Read	Write	Unit
		32GB	32GB	
HS400	VCC	105	65	mA
	VCCQ	155	105	
HS200	VCC	65	65	
	VCCQ	115	105	
DDR52	VCC	40	40	
	VCCQ	85	30	

[Table 7] Average Power Consumption VCC / VCCQ (3.3/1.8V at 30 degree)

Mode	Symbol	Read	Write	Unit
		32GB	32GB	
HS400	VCC	100	60	mA
	VCCQ	150	100	
HS200	VCC	60	60	
	VCCQ	110	100	
DDR52	VCC	30	30	
	VCCQ	80	25	

[Table 8]Average Standby Consumption VCC/VCCQ (3.3/1.8V at 30 degree)

Mode	Symbol	32GB	Unit
Standby (Auto power saving state)	VCC	40	µA
	VCCQ	80	

2.6 Environment Specifications

[Table 9] Working Temperature

Temperature	Operating	Non operating
	-25°C to 85°C	-40°C to 85°C

Note:

1) The operating specification is regarded as Ambient Temperature. Standard grade (-25°C to +85°C) and Industrial grade (-40°C to +85°C) indicate the temperature conditions for testing devices on programmable temperature and humidity chamber room.
2) The non-operating specification is regarded as storage specification.

2.7 Moisture Sensitivity Level(MSL)

The moisture sensitivity for EMC410T is MSL = 3.

2.8 System Reliability

[Table 10] Telcordia SR332 issue 4 MTBF Specifications

Parameter	32GB
MTBF	34,789,616 hours

Note:

1) The calculation is based on 25°C.

[Table 11] Data Retention Specifications

Parameter	32GB
Data Retention	18 years[1)]
	1 year [2)]

Note:

1) Data retention was measured by assuming that eMMC reaches the maximum rated endurance at 30°C under power-off state.
2) Data retention was measured by assuming that eMMC reaches the maximum rated endurance at 55°C under power-off state.
3) The data retention is defined in JESD47 Requirements for standard classes.

[Table 12] Power Scheme

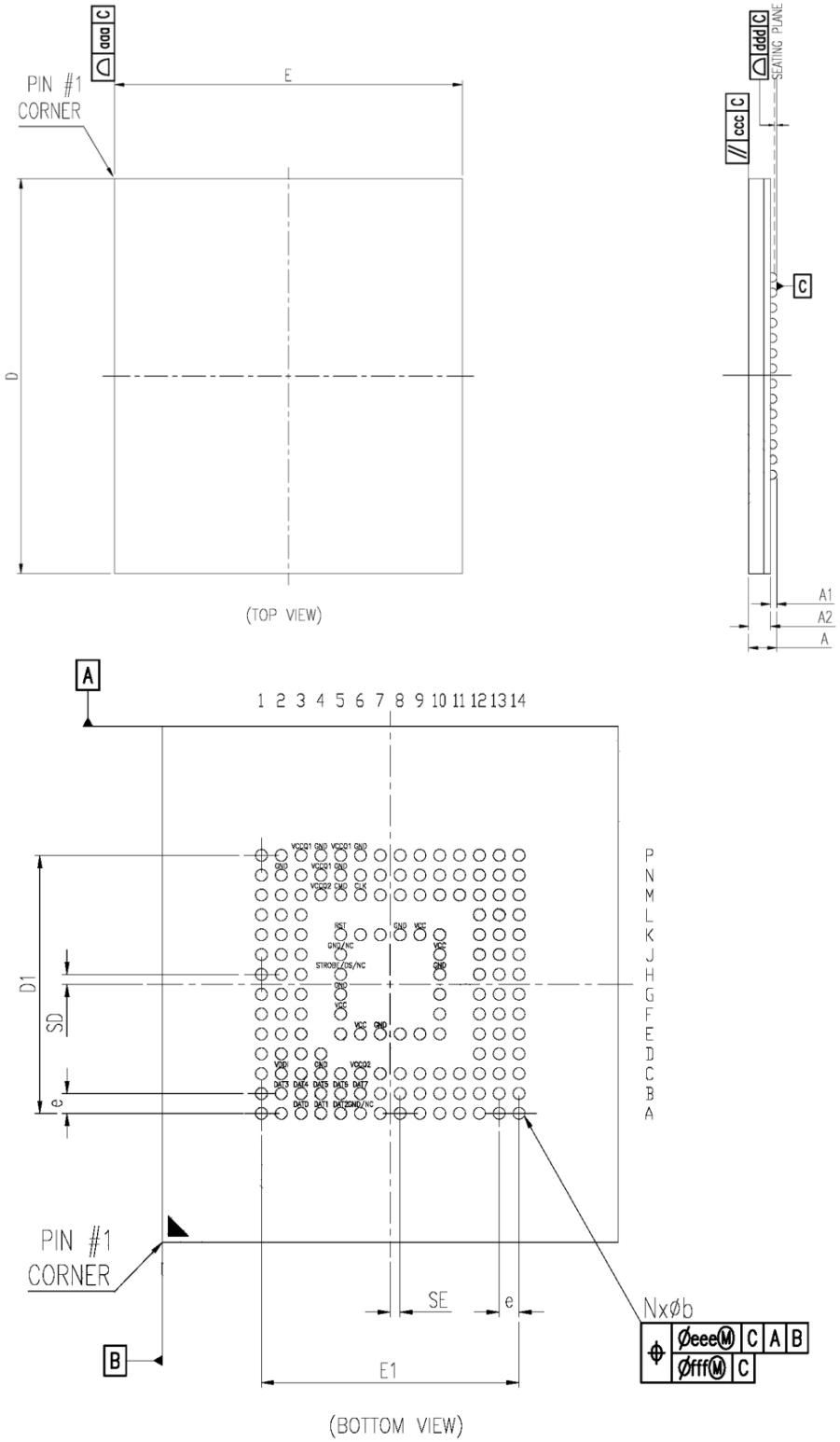
Parameter	32GB
Power Scheme	Refer Section 7(Power Scheme)

[Table 13] Warranty

Parameter	32GB
Warranty	3 years

3. Mechanical Specification

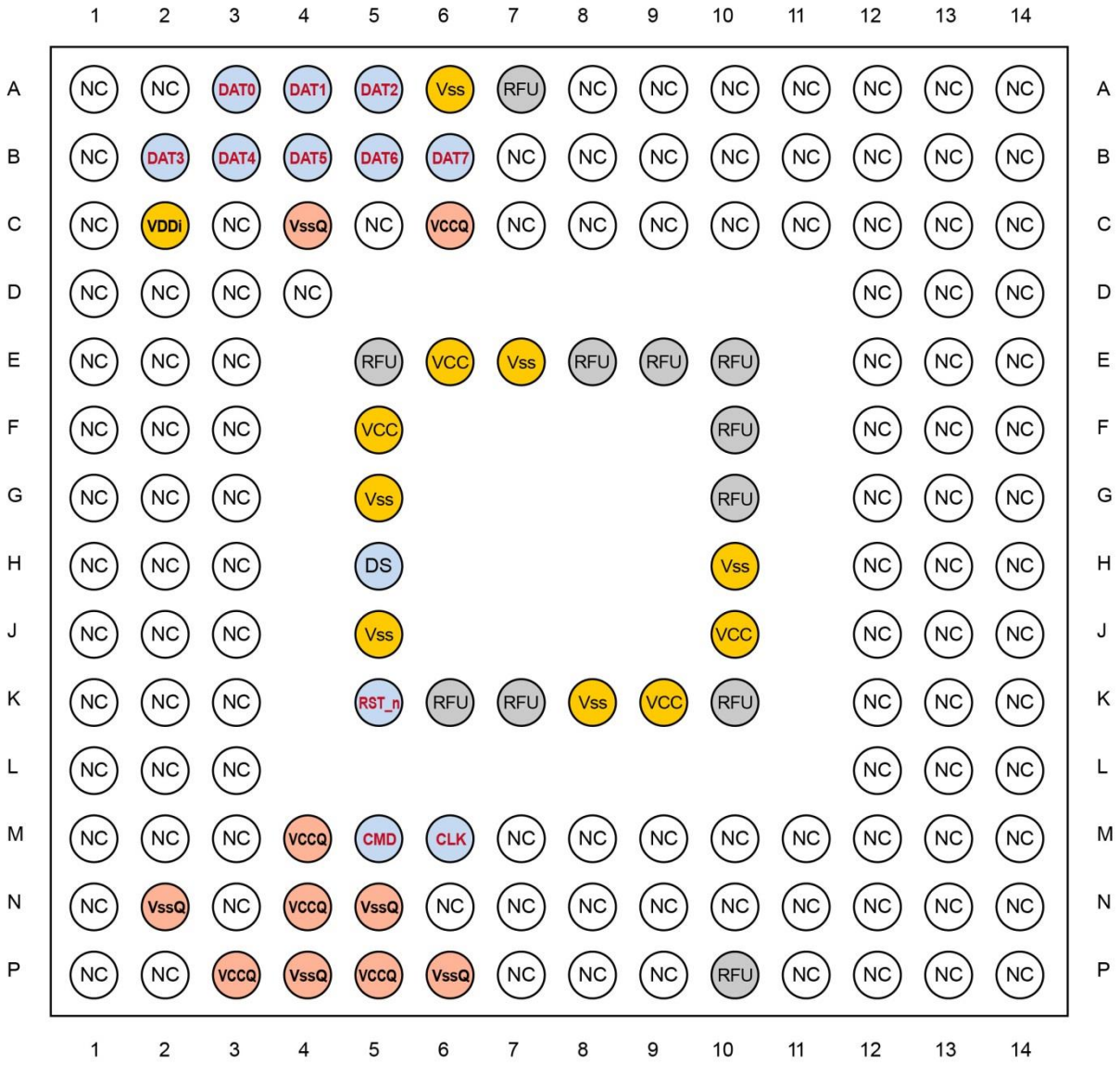
The device package consists of a 153-pin, thin fine-pitched ball grid array (BGA.) The figure below illustrates the eMMC.



[Table 14] Physical Dimensions and Weight

SYMBOL	Dimension in mm			Dimension in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	0.93	1.00	-	0.037	0.039
A1	0.15	0.21	0.26	0.006	0.008	0.010
A2	-	0.72	0.80	-	0.028	0.031
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.5 BSC			0.020 BSC.		
aaa	0.15					
ccc	0.2					
ddd	0.08					
eee	0.15					
fff	0.05					
N	SE (mm)	SD (mm)		E1 (mm)	D1 (mm)	
153L	0.25 BSC.	0.25 BSC.		6.50 BSC	6.50 BSC	
JEDEC	MO-276 (REF.)					

4.Interface Description



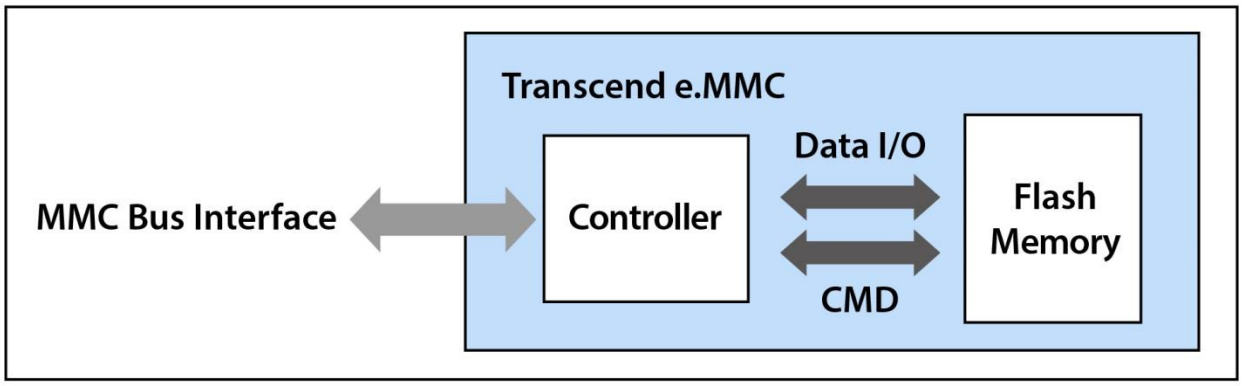
[Table 15] Interface Information

BGA Ball	Symbol	Type	Ball Function
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operation modes: • Open-drain for initialization • Push-pull for fast command transfer
A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.

BGA Ball	Symbol	Type	Ball Function
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	RST_n	Input	Reset signal pin
E6, F5, J10, K9	VCC	Supply	VCC: Flash memory interface and Flash memory power supply.
C6, M4, N4, P3, P5	VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
A6,E7, G5, H10,J5, K8	Vss	Supply	Vss: Flash memory interface and Flash memory ground connection.
C4, N2, N5, P4, P6	VssQ	Supply	VssQ: Memory controller core and MMC I/F ground connection.
C2	VDDi		VDDi: Internal power
H5	DS	Output	Data strobe
D4	NC Index	–	Index: Can be connected to ground or left floating.
A7, E5, E8, E9, E10, F10, G10, K6, K7, K10, P10	RFU	–	Reserved for future use. Left it floating for future use.
Others	NC	–	No connect: Can be connected to ground or left floating.

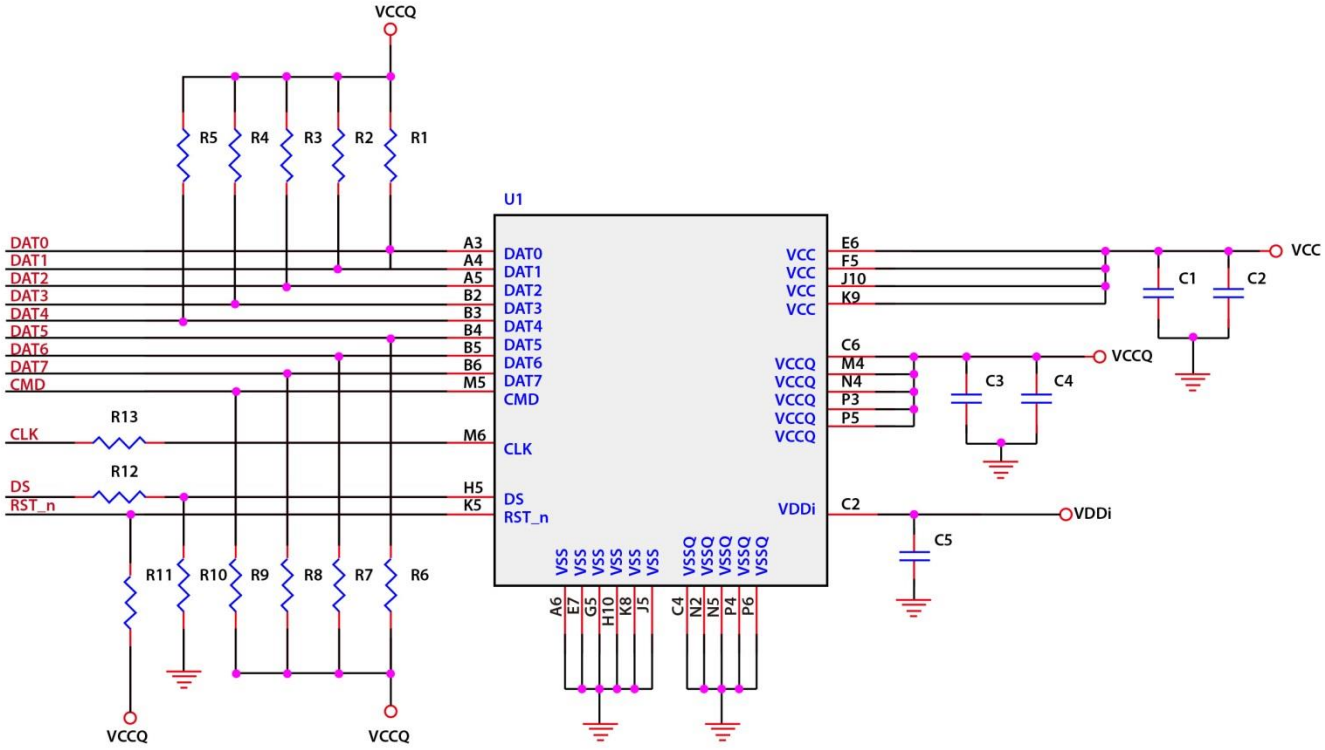
5. Block Diagram and Bus Information

5.1 Block Diagram



5.2 Reference Circuit

It is recommended that the power domains connectivity will follow figure.



[Table 16] Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Unit	Remark	Note
Pull-up resistance: DAT[7:0]	R1/R2/R3/R4 R5/R6/R7/R8	4.7	100	kΩ	To prevent bus floating	1)
Pull-up resistance: CMD	R9	10	100	kΩ		
Pull-up resistance: RST_n	R11	4.7	100	kΩ	Optional if host need H/W RESET function.	
Pull-down resistance: DS	R10	10	100	kΩ	For HS400 mode	
Serial resistance: DS	R12	0	47	Ω	Optional used to compensate eventual impedance mismatch	
Serial resistance: CLK	R13	0	47	Ω		
VCC capacitor	C1	2.2	4.7	µF	Should be placed with VCC pad as closely as possible	2)
	C2	0.1	0.22	µF		2)
VCCQ capacitor	C3	2.2	4.7	µF	Should be placed with VCCQ pad as closely as possible	2)
	C4	0.1	0.22	µF		2)
VDDi capacitor	C5	1	2.2	µF	Should be placed with VDDi pad as closely as possible	2)

Notes:

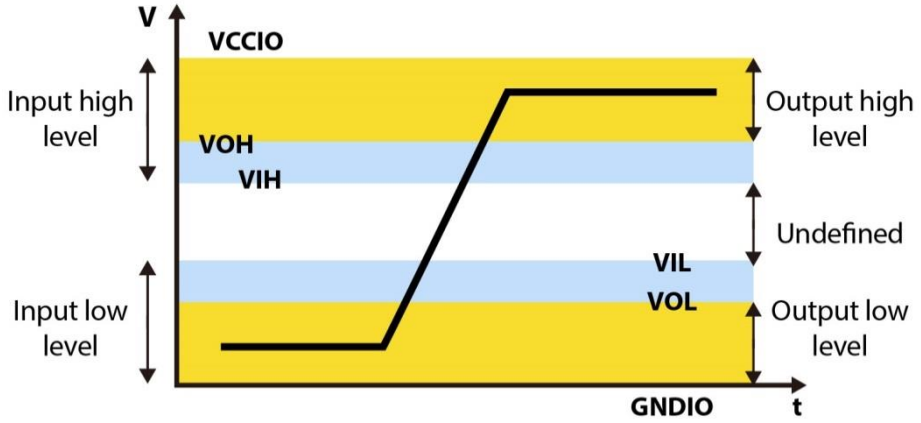
1) Recommended maximum pull-up is 50 kΩ for 1.8 V interface supply voltages. A 3.3 V part, may use the whole range up to 100 kΩ
2) Capacitor should be placed closed with Power Pad.
3) Signal trace of all DAT/CMD / DS/ CLK should be designed as 50 ohm.

5.3 Bus Load

Transcend's eMMC bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and eMMC operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and eMMC operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is eMMC's internal power node, not the power supply.
- VSS, VSSQ : Ground lines

5.4 Bus Signal Levels



[Table 17] Open-Drain Mode Bus Signal Level

Output voltage	Min.	Max.	Unit	
Output high voltage (VOH)	VCCQ – 0.2		V	
Output Low voltage (VOL)		0.3	V	IOL = 2mA

[Table 18] Push-Pull bus signal level (2.7~3.6V)

Input/ Output voltage	Min.	Max.	Unit	
Output high voltage (VOH)	0.75 * VCCQ		V	IOH = -100uA @ VDD min
Output Low voltage (VOL)		0.125 * VCCQ	V	IOL = 100uA @ VDD min
Input high voltage (VIH)	0.625 * VCCQ	VCCQ + 0.3	V	
Input Low voltage (VIL)	GND – 0.3	0.25 * VCCQ	V	

[Table 19] Push-pull bus signal level (1.70V~1.95V)

Input/ Output voltage	Max.	Min.	Unit	
Output high voltage (VOH)	VCCQ – 0.45		V	IOH = -2 mA
Output Low voltage (VOL)		0.45	V	IOL = 2 mA
Input high voltage (VIH)	0.65 * VCCQ	VCCQ + 0.3	V	
Input Low voltage (VIL)	GND – 0.3	0.35 * VCCQ	V	

[Table 20] Bus Mode

Mode	Data Rate	Bus Width	I/O Voltage	CLK
Legacy	Single	1,4,8	3.3/1.8V	0 – 26Mhz
High Speed SDR	Single	4,8	3.3/1.8V	0 – 52Mhz
High Speed DDR	Dual	4,8	3.3/1.8V	0 – 52Mhz
HS200	Single	4,8	3.3/1.8V	0 – 200Mhz
HS400	Dual	8	3.3/1.8V	0 – 200Mhz

Note:

1) Transcend eMMC support all bus mode defined in eMMC specification 5.1

6.Register information

6.1 OCR Register

[Table 21]OCR Resgister Values

OCR bit	VCCQ Voltage Window2	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b
[31]	eMMC power up status bit (busy)*	

Note*:

1)This bit is set to LOW if the device has not finished the power up routine.

6.2 CID Register

[Table 22]CID Information

Name	Field	Width	Value	CSD-slice
Manufacturer ID	MID	1	1Eh	[127:120]
Card/BGA	CBX	1	01h	[113:112]
OEM/Application ID	OID	1	FFh	[111:104]
Product name	PNM	6	533232334F20h	[103:56]
Product revision	PRV	1	Default: 10h	[55:48]
Product serial number	PSN	4	Random by production	[47:16]
Manufacturing date	MDT	1	Month Year	[15:8]
CRC7 checksum	CRC	1	-	[7:1]

6.3 CSD Register

R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 23] CSD Information

Name	Field	Width	Cell Type	Value	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	3h	[127:126]
System specification version	SPEC_VERS	4	R	4h	[125:122]
Reserved	-	2	R	-	[121:120]
Data read access-time 1	TAAC	8	R	27h	[119:112]
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	01h	[111:104]
Max. bus clock frequency	TRAN_SPEED	8	R	32h	[103:96]
Card command classes	CCC	12	R	0F5h	[95:84]
Max. read data block length	READ_BL_LEN	4	R	9h	[83:80]
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0h	[79:79]
Write block misalignment	WRITE_BLK_MISALIGN	1	R	0h	[78:78]
Read block misalignment	READ_BLK_MISALIGN	1	R	0h	[77:77]
DSR implemented	DSR_IMP	1	R	0h	[76:76]
Reserved	-	2	R	-	[75:74]
Device size	C_SIZE	12	R	FFFh	[73:62]
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	7h	[61:59]
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	7h	[58:56]
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	7h	[55:53]
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	7h	[52:50]
Device size multiplier	C_SIZE_MULT	3	R	7h	[49:47]
Erase group size	ERASE_GRP_SIZE	5	R	1Fh	[46:42]
Erase group size multiplier	ERASE_GRP_MULT	5	R	1Fh	[41:37]
Write protect group size	WP_GRP_SIZE	5	R	0Fh	[36:32]
Write protect group enable	WP_GRP_ENABLE	1	R	1h	[31:31]
Manufacturer default ECC	DEFAULT_ECC	2	R	0h	[30:29]
Write speed factor	R2W_FACTOR	3	R	2h	[28:26]
Max. write data block length	WRITE_BL_LEN	4	R	9h	[25:22]
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0h	[21:21]
Reserved	-	4	R	-	[20:17]
Content protection application	CONTENT_PROT_APP	1	R	0h	[16:16]
File format group	FILE_FORMAT_GRP	1	R/W	0h	[15:15]
Copy flag (OTP)	COPY	1	R/W	1h	[14:14]
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0h	[13:13]
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0h	[12:12]
File format	FILE_FORMAT	2	R/W	0h	[11:10]
ECC code	ECC	2	R/W/E	0h	[9:8]
CRC	CRC	7	R/W/E	TBD	[7:1]
Not used, always ’1’	-	1	–	TBD	[0:0]

6.4 Extended CSD register

R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 24] Extended CSD Information

Name	Field	Width	Cell Type	Value	CSD-slice (Byte)
Reserved	-	6	-	-	[511:506]
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	0h	[505]
Supported Command Sets	S_CMD_SET	1	R	1h	[504]
HPI features	HPI_FEATURES	1	R	1h	[503]
Background operations support	BKOPS_SUPPORT	1	R	1h	[502]
Max packed read commands	MAX_PACKED_READS	1	R	20h	[501]
Max packed write commands	MAX_PACKED_WRITES	1	R	20h	[500]
Data tag support	DATA_TAG_SUPPORT	1	R	1h	[499]
Tag unit size	TAG_UNIT_SIZE	1	R	0h	[498]
Tag Resource size	TAG_RES_SIZE	1	R	0h	[497]
Context management capabilities	CONTEXT_CAPABILITIES	1	R	78h	[496]
Large Unit Size	LARGE_UNIT_SIZE_M1	1	R	1h	[495]
Extended partitions attribute support	EXT_SUPPORT	1	R	3h	[494]
Supported modes	SUPPORTED_MODES	1	R	1h	[493]
FFU features	FFU_FEATURES	1	R	0h	[492]
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	17h	[491]
FFU Argument	FFU_ARG	4	R	FFFAFFF0h	[490:487]
Barrier support	BARRIER_SUPPORT	1	R	1h	[486]
Reserved	-	177	-	-	[485:309]

CMD Queuing Support	CMDQ_SUPPORT	1	R	1h	[308]
CMD Queuing Depth	CMDQ_DEPTH	1	R	1Fh	[307]
Reserved	-	1	-	-	[306]
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	0000h	[305:302]
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	0h	[301:270]
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	1h	[269]
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	1h	[268]
Pre EOL information	PRE_EOL_INFO	1	R	1h	[267]
Optimal read size	OPTIMAL_READ_SIZE	1	R	40h	[266]
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	40h	[265]
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	7h	[264]
Device version	DEVICE_VERSION	2	R	4205h	[263:262]
Firmware version	FIRMWARE_VERSION	8	R	100000h	[261:254]
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	0h	[253]
Cache size	CACHE_SIZE	4	R	0400h	[252:249]
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	5h	[248]
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	64h	[247]
Background operations status	BKOPS_STATUS	1	R	0h	[246]
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	0h	[245:242]
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	0Ah	[241]
Cache flushing policy	CACHE_FLUSH_POLICY	1	R	1h	[240]
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	0h	[239]
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	0h	[238]
Power class for 200MHz, at 1.95V	PWR_CL_200_195	1	R	0h	[237]
Power class for 200MHz, at 1.3V	PWR_CL_200_130	1	R	0h	[236]
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0h	[235]
Minimum Read Performance for 8bit at	MIN_PERF_DDR_R_8_52	1	R	0h	[234]

52MHz in DDR mode					
Reserved	-	1	-	-	[233]
TRIM Multiplier	TRIM_MULT	1	R	02h	[232]
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	55h	[231]
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	19h	[230]
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	0Ah	[229]
Boot information	BOOT_INFO	1	R	7h	[228]
Reserved	-	1	-	-	[227]
Boot partition size	BOOT_SIZE_MULTI	1	R	20h	[226]
Access size	ACC_SIZE	1	R	6h	[225]
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	1h	[224]
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	2h	[223]
Reliable write sector count	REL_WR_SEC_C	1	R	10h	[222]
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	10h	[221]
Sleep current (VCC)	S_C_VCC	1	R	7h	[220]
Sleep current (VCCQ)	S_C_VCCQ	1	R	7h	[219]
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	17h	[218]
Sleep/awake timeout	S_A_TIMEOUT	1	R	12h	[217]
Sleep Notification Timout	SLEEP_NOTIFICATION_TIME	1	R	0Ch	[216]
Sector Count	SEC_COUNT	4	R	3A3C000h	[215:212]
Secure Write Protect Information	SECURE_WP_INFO	1	R	1h	[211]
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	0h	[210]
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	0h	[209]
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0h	[208]
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_62	1	R	0h	[207]
Minimum Write Performance for 4 bit at 26MHz	MIN_PERF_W_4_26	1	R	0h	[206]
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	0h	[205]

Reserved	-	1	-	-	[204]
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	0h	[203]
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	0h	[202]
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	0h	[201]
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	0h	[200]
Partition switching timing	PARTITION_SWITCH_TIME	1	R	4h	[199]
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	Ah	[198]
I/O driver strength	DRIVER_STRENGTH	1	R	1Fh	[197]
Device type	DEVICE_TYPE	1	R	57h	[196]
Reserved	-	1	-	-	[195]
CSD structure version	CSD_STRUCTURE	1	R	2h	[194]
Reserved	-	1	-	-	[193]
Extended CSD revision	EXT_CSD_REV	1	R	8h	[192]
Command set	CMD_SET	1	R/W/E_P	0h	[191]
Reserved	-	1	-	-	[190]
Command set revision	CMD_SET_REV	1	R	0h	[189]
Reserved	-	1	-	-	[188]
Power class	POWER_CLASS	1	R/W/E_P	0h	[187]
Reserved	-	1	-	-	[186]
High-speed interface timing	HS_TIMING	1	R/W/E_P	0h	[185]
Strobe support	STROBE_SUPPORT	1	R	1h	[184]
Bus width mode	BUS_WIDTH	1	W/E_P	0h	[183]
Reserved	-	1	-	-	[182]
Erased memory content	ERASED_MEM_CONT	1	R	0h	[181]
Reserved	-	1	-	-	[180]
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0h	[179]
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0h	[178]
Boot bus condition	BOOT_BUS_CONDITION	1	R/W/E	0h	[177]
Reserved	-	1	-	-	[176]
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0h	[175]
Boot write protection status registers	BOOT_WP_STATUS	1	R	0h	[174]
Boot area write protection	BOOT_WP	1	R/W &	0h	[173]

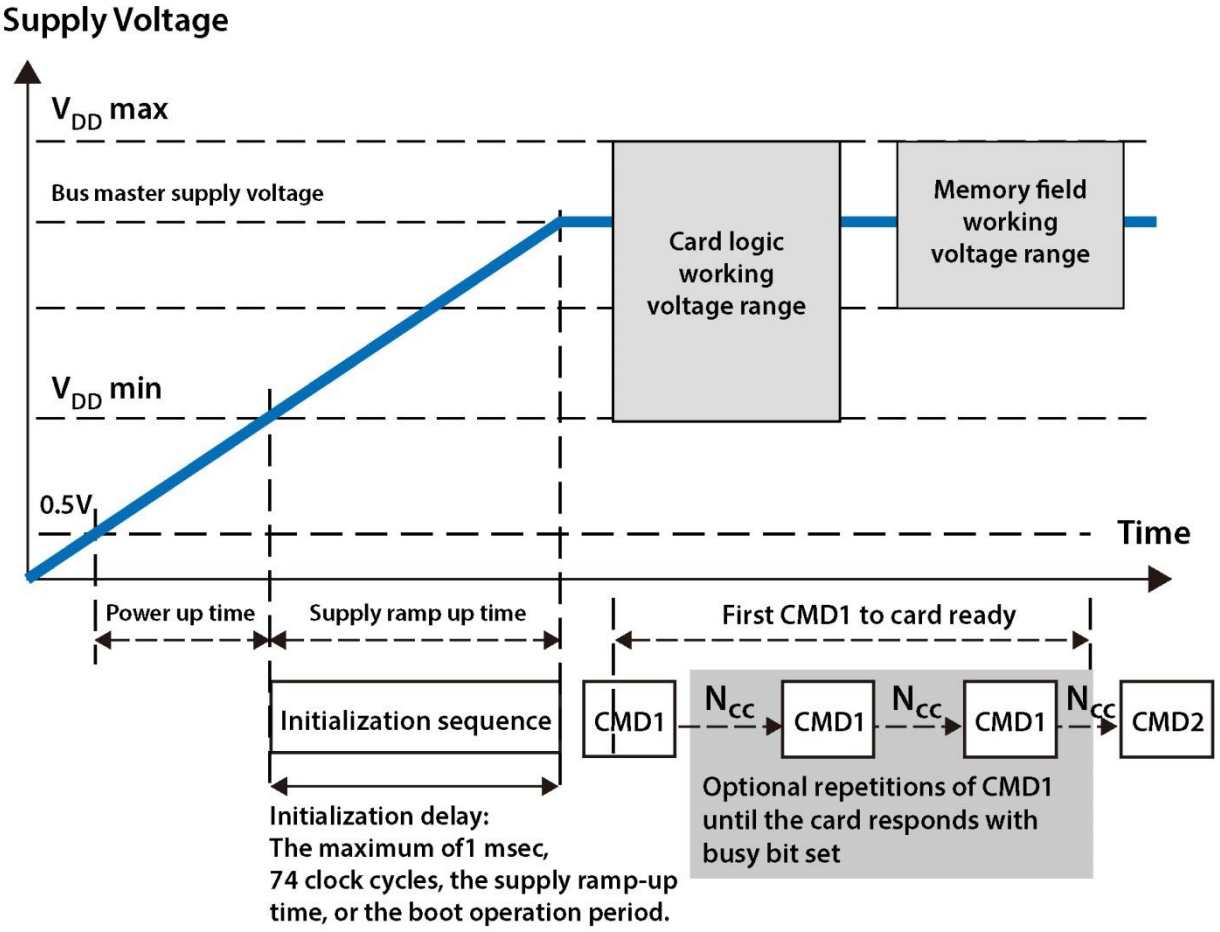
register			R/W/C_P		
Reserved	-	1	-	-	[172]
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0h	[171]
Reserved	-	1	-	-	[170]
FW configuration	FW_CONFIG	1	R/W	0h	[169]
RPMB Size	RPMB_SIZE_MULT	1	R	20h	[168]
Write reliability setting register	WR_REL_SET	1	R/W	1Fh	[167]
Write reliability parameter register	WR_REL_PARAM	1	R	15h	[166]
Start Sanitize operation	SANITIZE_START	1	W/E_P	0h	[165]
Manually start background operations	BKOPS_START	1	W/E_P	0h	[164]
Enable background operations handshake	BKOPS_EN	1	R/W	2h	[163]
H/W reset function	RST_n_FUNCTION	1	R/W	0h	[162]
HPI management	HPI_MGMT	1	R/W/E_P	0h	[161]
Partitioning Support	PARTITIONING_SUPPORT	1	R	7h	[160]
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	4DAh	[159:157]
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	0h	[156]
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	0h	[155]
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	0h	[154:143]
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	0h	[142:140]
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0h	[139:136]
Reserved	-	1	-	-	[135]
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0h	[134]
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	0h	[133]
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	0h	[132]
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	0h	[131]
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	0h	[130]
Reserved	-	2	-	-	[129:128]
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor specific	14h	[127:64]
Native sector size	NATIVE_SECTOR_SIZE	1	R	1h	[63]

Sector size emulation	USE_NATIVE_SECTOR	1	R/W	0h	[62]
Sector size	DATA_SECTOR_SIZE	1	R	0h	[61]
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	0Ah	[60]
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	0h	[59]
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	0h	[58]
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	00h	[57:56]
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	00h	[55:54]
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	00h	[53:52]
Context configuration	CONTEXT_CONF	15	R/W/E_P	0h	[51:37]
Packed command status	PACKED_COMMAND_STATUS	1	R	0h	[36]
Packed command failure index	PACKED_FAILURE_INDEX	1	R	0h	[35]
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	0h	[34]
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	0h	[33]
Flushing of the cache	FLUSH_CACHE	1	W/E_P	0h	[32]
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	0h	[31]
Mode config	MODE_CONFIG	1	R/W/E_P	0h	[30]
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	0h	[29]
Reserved	-	2	-	-	[28:27]
FFU status	FFU_STATUS	1	R	0h	[26]
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	0h	[25:22]
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	01368000h	[21:18]
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	01h	[17]
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	3Bh	[16]
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	0h	[15]
Reserved	-	15	-	-	[14:0]

7.Power Scheme

7.1 Power Up Time of eMMC

The power up of the eMMC bus is handled locally in the Device and in the bus master.



After power up (including hot insertion, i.e., inserting a Device when the bus is operating), the Device enters the pre-idle state. The power up time of the supply voltage should be less than the specified t_{PRU} for the Bus master supply voltage.

If the Device does not support boot mode, or its BOOT_PARTITION_ENABLE bit is cleared, the Device moves immediately to the idle state. While in the idle state, the Device ignores all bus transactions until CMD1 is received. If the Device supports only standard v4.2 or earlier versions, it enters the idle state immediately following power-up.

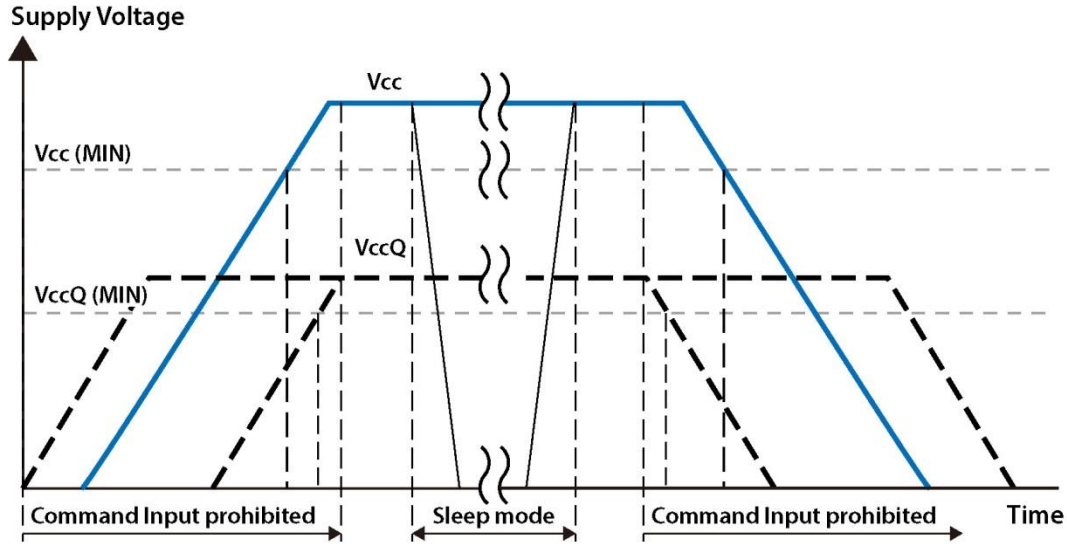
If the Device BOOT_PARTITION_ENABLE bit is set, the Device moves to the pre-boot state. The

Device then waits for boot initiation sequence. Following the boot operation period, the Device enters the idle state. During the pre-boot state, if the Device receives any CMD line transaction other than CMD1 or the boot initiation sequence (keeping the CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of 0xFFFFFFFA), the Device moves to the idle state. If the Device receives the boot initiation sequence (keeping the CMD line low for at least 74 clock cycles, or issuing CMD0 with the argument of

0xFFFFFFFA), the Device begins boot operation. If boot acknowledge is enabled, the Device shall send acknowledge pattern “010” to the host within the specified time. After boot operation is terminated, the Device enters the idle state and shall be ready for CMD1 operation. If the Device receives CMD1 in the pre-boot state, it begins responding to the command and moves to Device identification mode.
While in the idle state, the Device ignores all bus transactions until CMD1 is received.

7.2 Power Cycle

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.



If V_{CC} or V_{CCQ} are below 0.5 V for longer than 1 ms, the slave shall always return to the pre-idle state, and perform the appropriate boot behavior, as appropriate. The slave will behaves as in a standard power-up condition once the voltages have returned to their functional ranges
An exception to this behavior is if the device is in sleep state, in which the voltage on V_{CC} is not monitored.

In addition to the above rules, in case of e^2•MMC, the D-V_{DDQ} shall be ramped down before D-V_{DD} and also D-V_{DDQ} / D-V_{DD} shall both be in stable state within the operation voltage range before any commands may be issued. Both D-V_{DDQ} and D-V_{DD} may be powered-down while the device is in Sleep state. Still again both D-V_{DDQ} and D-V_{DD} shall be powered-up before host issues CMD5 to wake-up the slave device.

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