



AO4425

P-Channel Enhancement Mode Field Effect Transistor

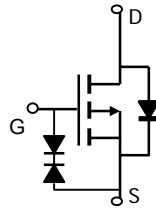
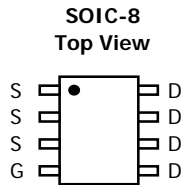


General Description

The AO4425 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications. It is ESD protected. *Standard Product AO4425 is Pb-free (meets ROHS & Sony 259 specifications). AO4425L is a Green Product ordering option. AO4425 and AO4425L are electrically identical.*

Features

- V_{DS} (V) = -38V
- I_D = -14A (V_{GS} = -20V)
- $R_{DS(ON)} < 10m\Omega$ (V_{GS} = -20V)
- $R_{DS(ON)} < 11m\Omega$ (V_{GS} = -10V)
- ESD Rating: 4000V HBM



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-38	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ\text{C}$	-14
		$T_A=70^\circ\text{C}$	-11
Pulsed Drain Current ^B	I_{DM}	-50	A
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	26	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	14	24	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-38			V
I _D DSS	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-100 -500	nA
I _G DSS	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V V _{DS} =0V, V _{GS} =±25V			±1 ±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-2	-2.5	-3.5	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-20V, I _D =-14A T _J =125°C		7.7 11	10 13.5	mΩ
		V _{GS} =-10V, I _D =-14A		8.8	11	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-14A		43		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		0.71	1	V
I _S	Maximum Body-Diode Continuous Current				4.2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, f=1MHz		3800		pF
C _{oss}	Output Capacitance			560		pF
C _{riss}	Reverse Transfer Capacitance			350		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		7.5		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-20V, I _D =-14A		63		nC
Q _{gs}	Gate Source Charge			14.1		nC
Q _{gd}	Gate Drain Charge			16.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-20V, R _L =1.35Ω, R _{GEN} =3Ω		12.4		ns
t _r	Turn-On Rise Time			9.2		ns
t _{D(off)}	Turn-Off DelayTime			97.5		ns
t _f	Turn-Off Fall Time			45.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =-14A, dI/dt=100A/μs		35	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-14A, dI/dt=100A/μs		33		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

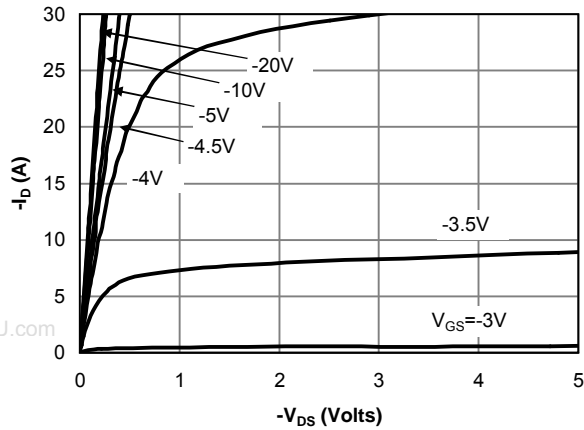


Fig 1: On-Region Characteristics

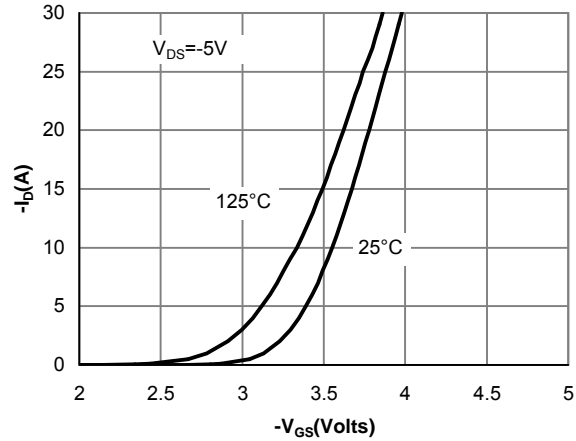


Figure 2: Transfer Characteristics

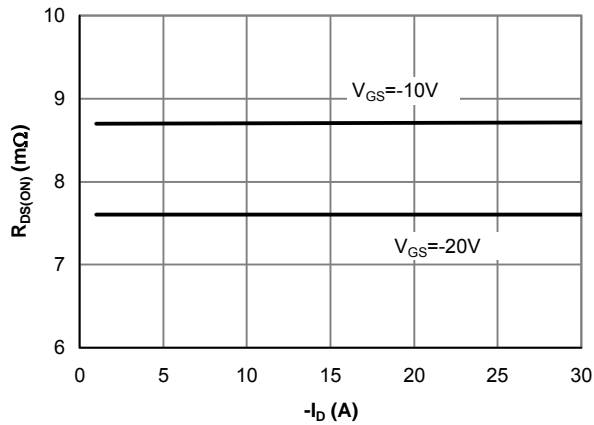


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

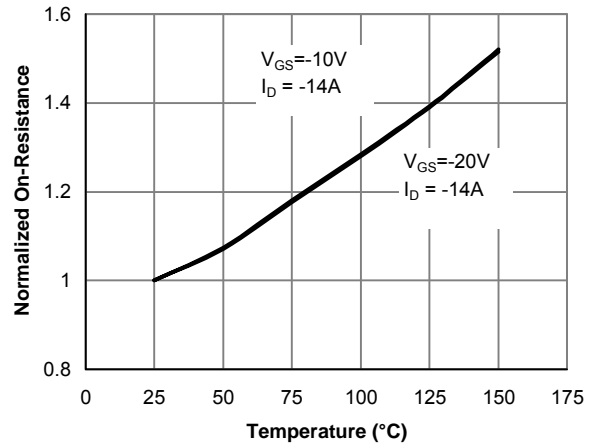


Figure 4: On-Resistance vs. Junction Temperature

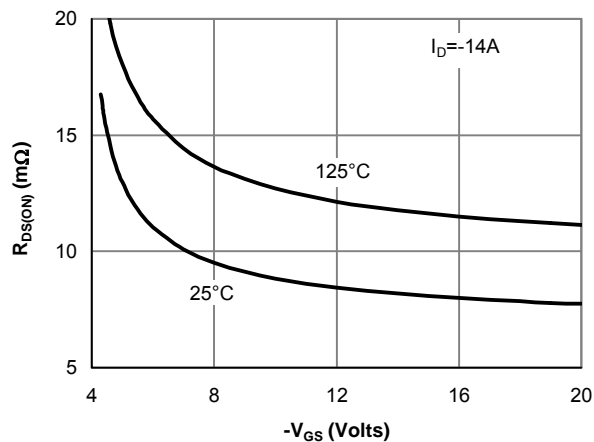


Figure 5: On-Resistance vs. Gate-Source Voltage

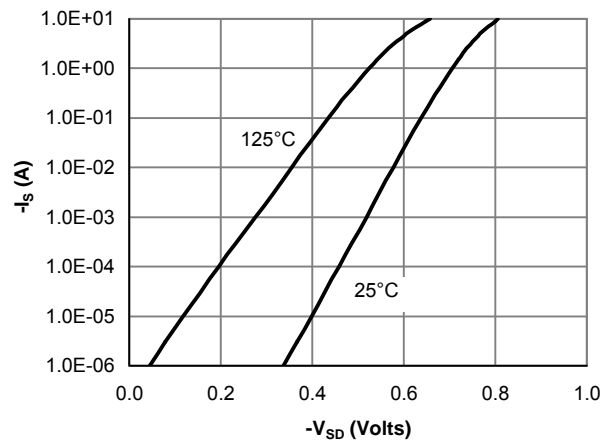


Figure 6: Body-Diode Characteristics

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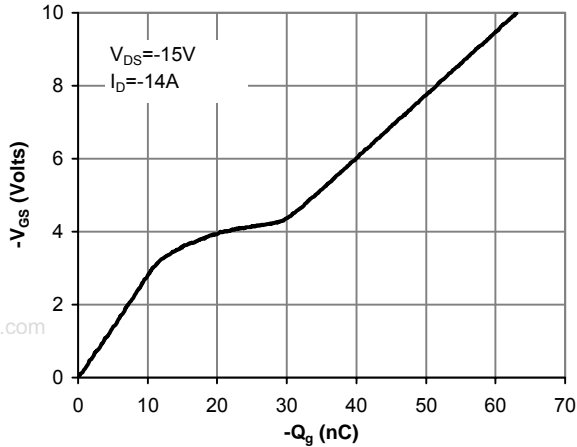


Figure 7: Gate-Charge Characteristics

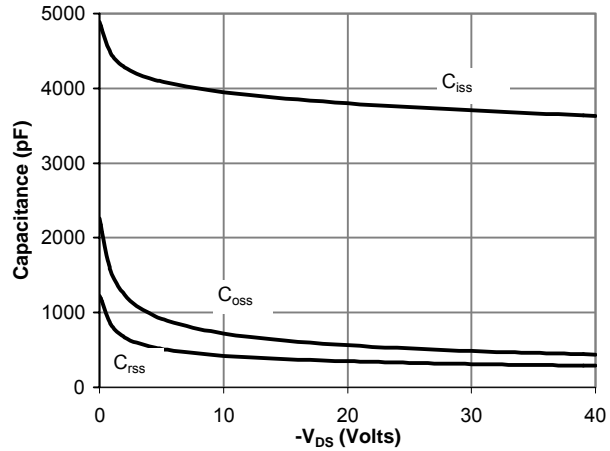


Figure 8: Capacitance Characteristics

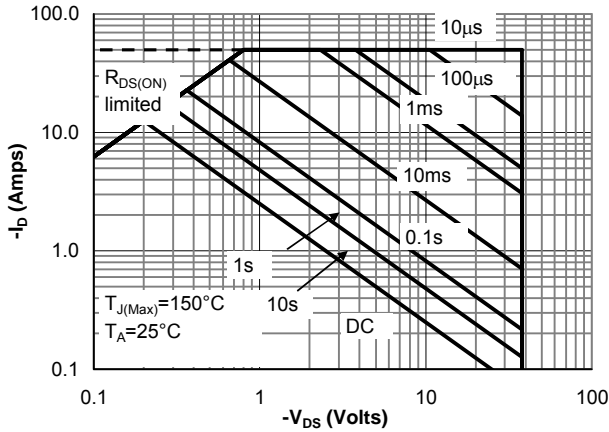


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

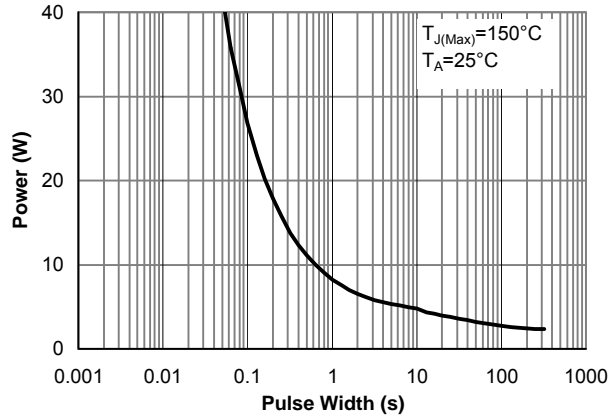


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

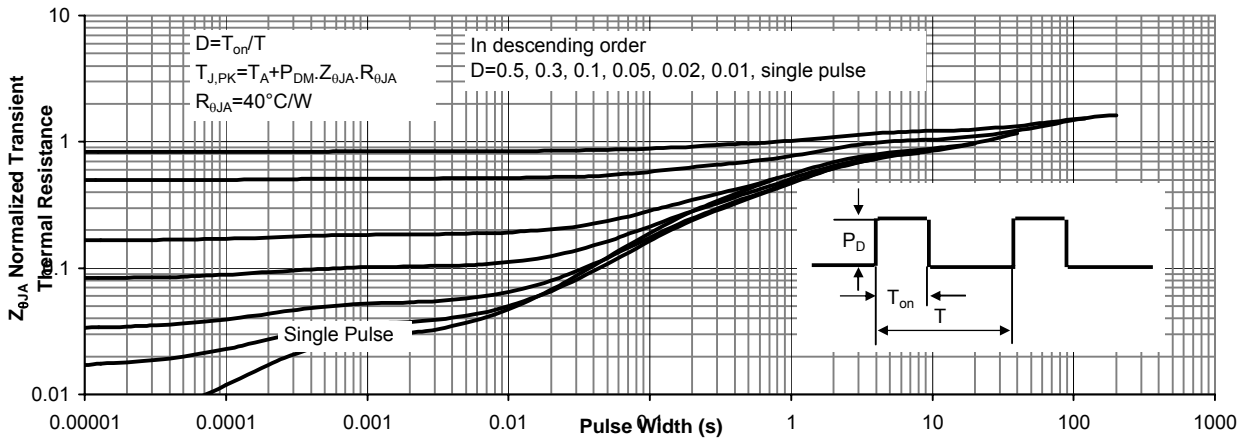


Figure 11: Normalized Maximum Transient Thermal Impedance