



1 pC Charge Injection, 100 pA Leakage CMOS ± 5 V/5 V/3 V 4-Channel Multiplexer

ADG604

FEATURES

- 1 pC Charge Injection (Over the Full Signal Range)
- ± 2.7 V to ± 5.5 V Dual Supply
- 2.7 V to 5.5 V Single Supply
- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- 100 pA Max @ 25°C Leakage Currents
- 85 Ω Typ On Resistance
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption ($<0.1 \mu\text{W}$)
- TTL/CMOS Compatible Inputs
- 14-Lead TSSOP Package

APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Battery-Powered Instruments
- Communication Systems
- Sample and Hold Systems
- Remote-Powered Equipment
- Audio and Video Signal Routing
- Relay Replacement
- Avionics

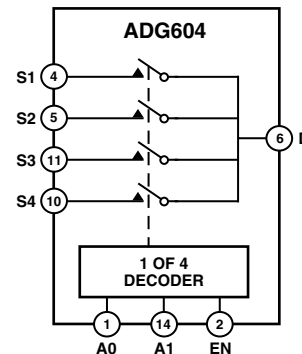
GENERAL DESCRIPTION

The ADG604 is a CMOS analog multiplexer, comprising four single channels. It operates from a dual supply of ± 2.7 V to ± 5.5 V, or from a single supply of 2.7 V to 5.5 V.

The ADG604 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. A Logic "0" on the EN pin disables the device.

The ADG604 offers ultralow charge injection of ± 1.5 pC over the entire signal range and leakage currents of 10 pA typical at 25°C . It offers on resistance of 85 Ω typ, which is matched to within 2 Ω between channels. The ADG604 also has low power dissipation yet gives high switching speeds. The ADG604 is available in a 14-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection (Q_{INJ} : ± 1.5 pC Typ over the Full Signal Range)
2. Leakage Current <0.5 nA max @ 85°C
3. Dual ± 2.7 V to ± 5.5 V or Single 2.7 V to 5.5 V Supply
4. Fully Specified to 125°C
5. Small 14-Lead TSSOP Package

REV. A

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ADG604—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------------------------|----------------|----------------------|--|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | V | |
| On Resistance (R_{ON}) | 85 115 | 140 | 160 | Ω Typ Ω Max | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1 |
| On Resistance Match Between Channels (ΔR_{ON}) | 2 4 | 5.5 | 6.5 | Ω Typ Ω Max | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 25 40 | 55 | 60 | Ω Typ Ω Max | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 ± 0.1 | ± 0.25 | ± 4 | nA Typ nA Max | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, Test Circuit 2 |
| Drain OFF Leakage I_D (OFF) | ± 0.01 ± 0.1 | ± 0.5 | ± 8 | nA Typ nA Max | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, Test Circuit 2 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 ± 0.1 | ± 0.5 | ± 10 | nA Typ nA Max | $V_S = V_D = \pm 4.5\text{ V}$, Test Circuit 3 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.4 | V Min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V Max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | ± 0.1 | μA Typ μA Max | $V_{IN} = V_{INL}$ or V_{INH} |
| C_{IN} , Digital Input Capacitance | 2 | | | pF Typ | |
| DYNAMIC CHARACTERISTICS | | | | | |
| Transition Time | 70 100 | 120 | 150 | ns Typ ns Max | $V_{S1} = +3\text{ V}$, $V_{S4} = -3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4 |
| t_{ON} Enable | 80 105 | 130 | 150 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 6 |
| t_{OFF} Enable | 30 45 | 55 | 65 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 6 |
| Break-Before-Make Time Delay, t_{BBM} | 20 | | 10 | ns Typ ns Min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5 |
| Charge Injection | -1 | | | pC Typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, Test Circuit 7 |
| Off Isolation | -75 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8 |
| Channel-to-Channel Crosstalk | -70 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 10 |
| Bandwidth -3 dB | 280 | | | MHz Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9 |
| C_S (OFF) | 5 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 17 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 18 | | | pF Typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | 1.0 | μA Typ μA Max | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V |
| I_{SS} | 0.001 | | 1.0 | μA Typ μA Max | Digital Inputs = 0 V or 5.5 V |

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------------------------|-------------------|--------------------|--|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 210 290 | 350 | 380 | Ω Typ Ω Max | $V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1 |
| On Resistance Match Between Channels (ΔR_{ON}) | 3 | 12 | 13 | Ω Typ Ω Max | $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 ± 0.1 | ± 0.25 | ± 4 | nA Typ nA Max | $V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$, Test Circuit 2 |
| Drain OFF Leakage I_D (OFF) | ± 0.01 ± 0.1 | ± 0.5 | ± 8 | nA Typ nA Max | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$, Test Circuit 2 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 ± 0.1 | ± 0.5 | 10 | nA Typ nA Max | $V_S = V_D = 4.5\text{ V}/1\text{ V}$, Test Circuit 3 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.4 | V Min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V Max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | ± 0.1 | μA Typ μA Max | $V_{IN} = V_{INL}$ or V_{INH} |
| C_{IN} , Digital Input Capacitance | 2 | | | pF Typ | |
| DYNAMIC CHARACTERISTICS | | | | | |
| Transition Time | 90 150 | 185 | 210 | ns Typ ns Max | $V_{S1} = 3\text{ V}$, $V_{S4} = 0\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4 |
| t_{ON} Enable | 105 150 | 190 | 220 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 6 |
| t_{OFF} Enable | 45 70 | 80 | 90 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 6 |
| Break-Before-Make Time Delay, t_{BBM} | 30 | | 10 | ns Typ ns Min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5 |
| Charge Injection | 0.3 | | | pC Typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, Test Circuit 7 |
| Off Isolation | -65 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8 |
| Channel-to-Channel Crosstalk | -70 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 10 |
| Bandwidth -3 dB | 250 | | | MHz Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9 |
| C_S (OFF) | 5 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 17 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 18 | | | pF Typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | 1.0 | μA Typ μA Max | $V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V |

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$.

Specifications subject to change without notice.

ADG604—SPECIFICATIONS

SINGLE SUPPLY¹

($V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^{\circ}\text{C}$ unless otherwise noted.)

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|-------------------------|----------------|-----------------|--|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 380 | 420 | 460 | Ω Typ | $V_{DD} = 2.7\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1 |
| On Resistance Match Between Channels (ΔR_{ON}) | | | 5 | Ω Typ | $V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.01 ± 0.1 | ± 0.25 | ± 4 | nA Typ nA Max | $V_{DD} = 3.3\text{ V}$ $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2 |
| Drain OFF Leakage I_D (OFF) | ± 0.01 ± 0.1 | ± 0.5 | ± 8 | nA Typ nA Max | $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 ± 0.1 | ± 0.5 | ± 10 | nA Typ nA Max | $V_S = V_D = 1\text{ V}/3\text{ V}$, Test Circuit 3 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V Min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V Max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | ± 0.1 | μA Typ μA Max | $V_{IN} = V_{INL}$ or V_{INH} |
| C_{IN} , Digital Input Capacitance | 2 | | | pF Typ | |
| DYNAMIC CHARACTERISTICS | | | | | |
| Transition Time | 170 320 | | 450 | ns Typ ns Max | $V_{S1} = 2\text{ V}$, $V_{S4} = 0\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4 |
| t_{ON} Enable | 180 250 | 390 | 390 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 6 |
| t_{OFF} Enable | 100 160 | 265 | 225 | ns Typ ns Max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$, Test Circuit 6 |
| Break-Before-Make Time Delay, t_{BBM} | 100 | | 10 | ns Typ ns Min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 2\text{ V}$, Test Circuit 5 |
| Charge Injection | 0.3 | | | pC Typ | $V_S = 0\text{ V}$ to 3.3 V , $R_S = 0\ \Omega$, $C_L = 1\ \mu\text{F}$, Test Circuit 7 |
| Off Isolation | -65 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8 |
| Channel-to-Channel Crosstalk | 70 | | | dB Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 10 |
| Bandwidth -3 dB | 250 | | | MHz Typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9 |
| C_S (OFF) | 5 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 17 | | | pF Typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 18 | | | pF Typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | 1.0 | μA Typ μA Max | $V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V |

NOTES

¹Y Version Temperature Range: -40°C to $+125^{\circ}\text{C}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

| | |
|--|---|
| V _{DD} to V _{SS} | 13 V |
| V _{DD} to GND | -0.3 V to +6.5 V |
| V _{SS} to GND | +0.3 V to -6.5 V |
| Analog Inputs ² | V _{SS} - 0.3 V to V _{DD} + 0.3 V |
| Digital Inputs ² | -0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First |
| Peak Current, S or D | 20 mA (Pulsed at 1 ms, 10% Duty Cycle Max) |
| Continuous Current, S or D | 10 mA |
| Operating Temperature Range (Y Version) | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |

| | |
|--|---------|
| Junction Temperature | 150°C |
| TSSOP Package θ _{JA} Thermal Impedance | 150°C/W |
| θ _{JC} Thermal Impedance | 27°C/W |
| Lead Temperature, Soldering (10 seconds) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at EN, A0, A1, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATION

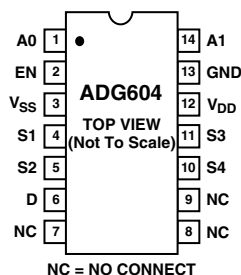


Table I. Truth Table

| A1 | A0 | EN | ON Switch |
|----|----|----|-----------|
| X | X | 0 | None |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 4 |

CAUTION

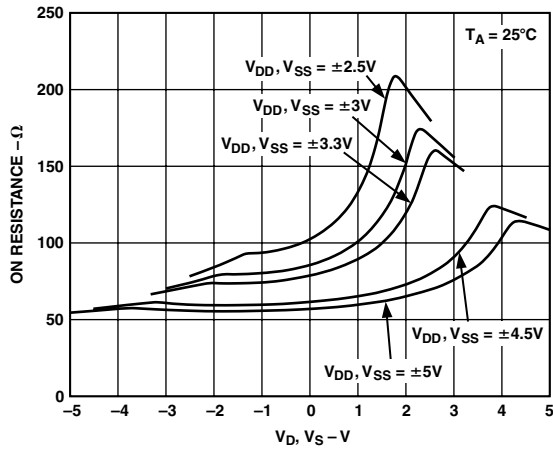
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG604 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



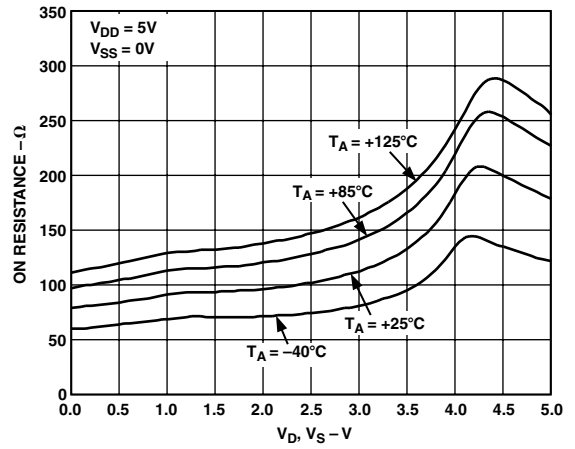
TERMINOLOGY

| | |
|-------------------------|--|
| V_{DD} | Most Positive Power Supply Potential |
| V_{SS} | Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device. |
| GND | Ground (0 V) Reference |
| I_{DD} | Positive Supply Current |
| I_{SS} | Negative Supply Current |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| R_{ON} | Ohmic Resistance between D and S |
| ΔR_{ON} | On Resistance Match between any two channels, i.e., $R_{ON\ Max} - R_{ON\ Min}$ |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of On resistance as measured over the specified analog signal range. |
| I_S (OFF) | Source Leakage Current with the Switch "OFF" |
| I_D (OFF) | Drain Leakage Current with the Switch "OFF" |
| I_D, I_S (ON) | Channel Leakage Current with the Switch "ON" |
| V_D, V_S | Analog Voltage on Terminals D, S |
| V_{INL} | Maximum Input Voltage for Logic "0" |
| V_{INH} | Minimum Input Voltage for Logic "1" |
| I_{INL} (I_{INH}) | Input Current of the Digital Input |
| C_S (OFF) | Channel Input Capacitance for "OFF" Condition |
| C_D (OFF) | Channel Output Capacitance for "OFF" Condition |
| C_D, C_S (ON) | "On" Switch Capacitance |
| C_{IN} | Digital Input Capacitance |
| t_{ON} (EN) | Delay time between the 50% and 90% points of the digital input and switch "ON" condition. |
| t_{OFF} (EN) | Delay time between the 50% and 90% points of the digital input and switch "OFF" condition. |
| $t_{TRANSITION}$ | Delay time between the 50% and 90% points of the digital input and switch "ON" condition when switching from one address state to another. |
| t_{BBM} | "OFF" time or "ON" time measured between the 80% points of both switches, when switching from one address state to another. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A measure of unwanted signal coupling through an "On" switch. |
| Bandwidth | Frequency Response of the "On" Switch |
| Insertion Loss | Loss Due to the On Resistance of the Switch |

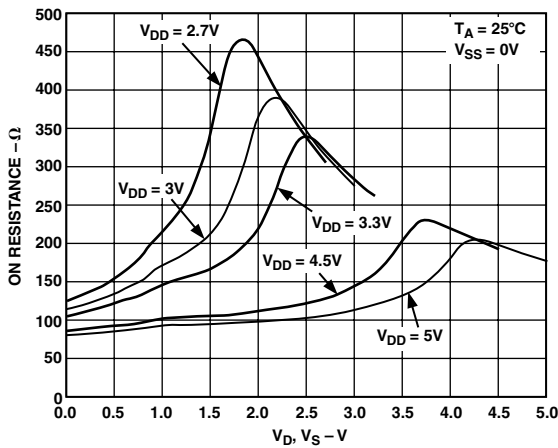
Typical Performance Characteristics—ADG604



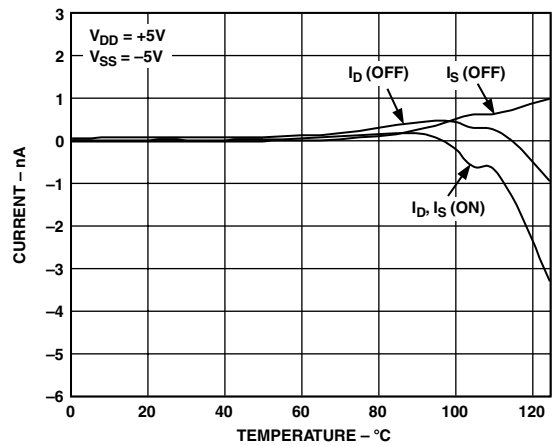
TPC 1. On Resistance vs. V_D (V_S), Dual Supply



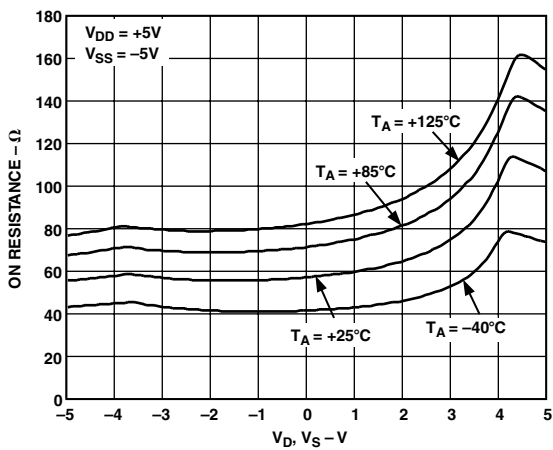
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply



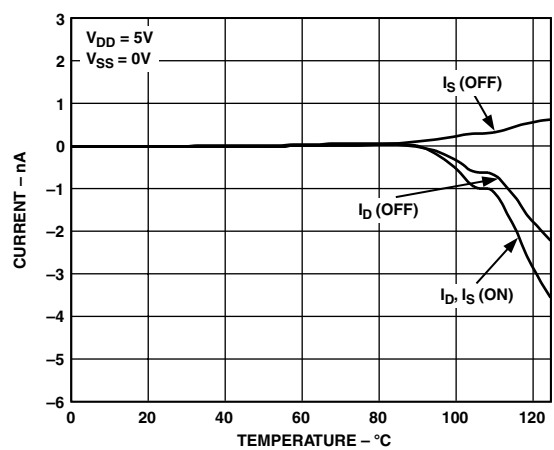
TPC 2. On Resistance vs. V_D (V_S), Single Supply



TPC 5. Leakage Currents vs. Temperature, Dual Supply

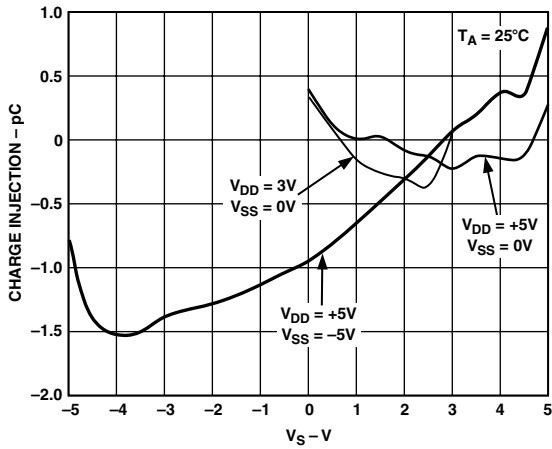


TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures, Dual Supply

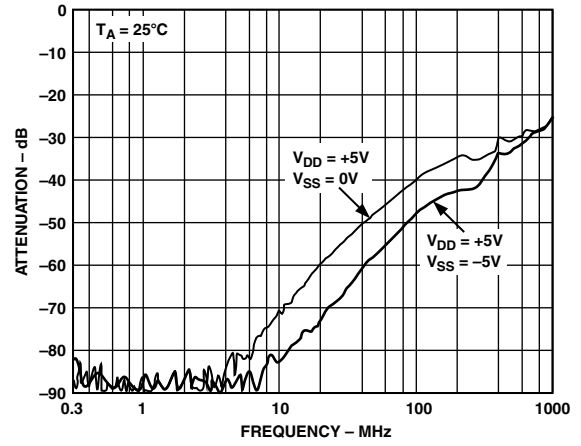


TPC 6. Leakage Currents vs. Temperature, Single Supply

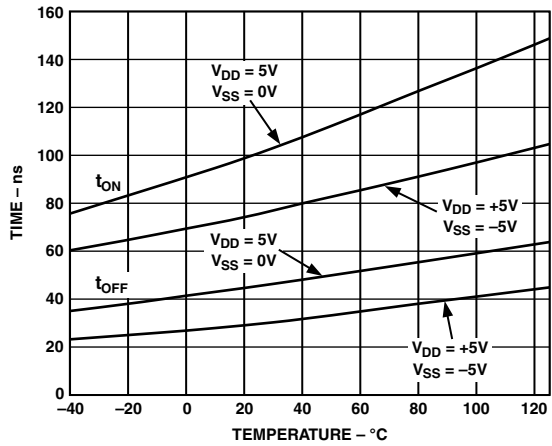
ADG604



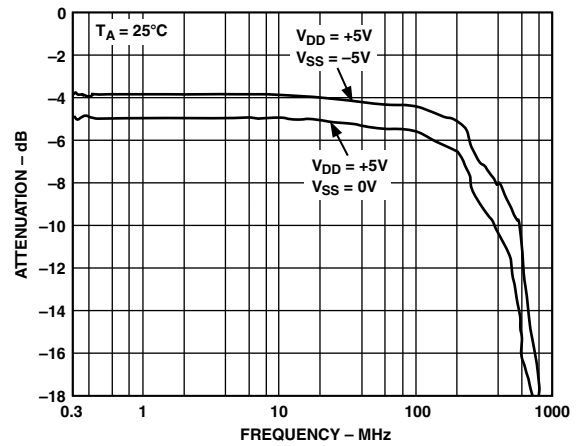
TPC 7. Charge Injection vs. Source Voltage



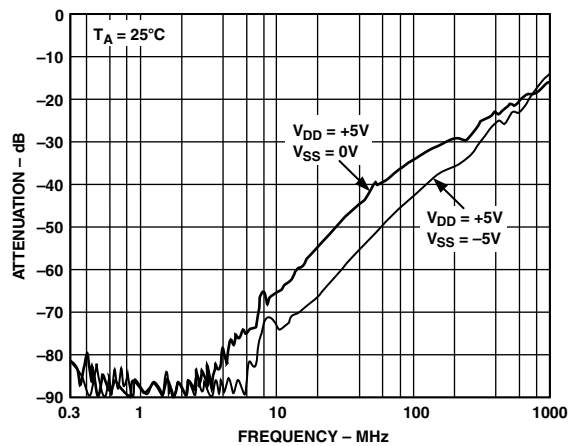
TPC 10. Crosstalk vs. Frequency



TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

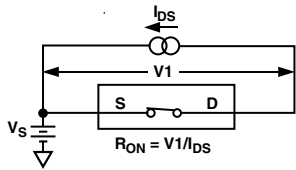


TPC 11. On Response vs. Frequency

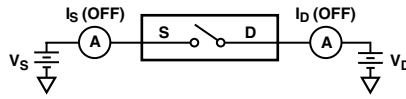


TPC 9. Off Isolation vs. Frequency

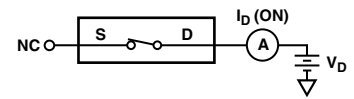
Test Circuits



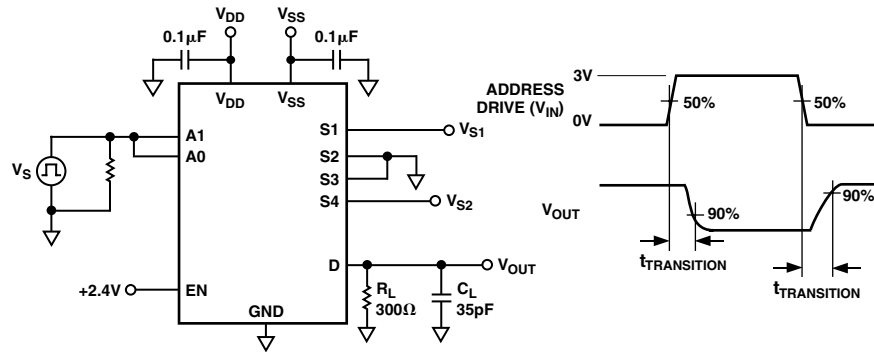
Test Circuit 1. On Resistance



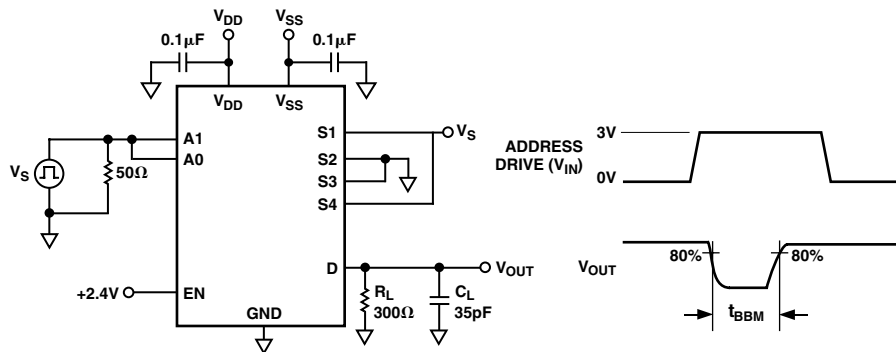
Test Circuit 2. Off Leakage



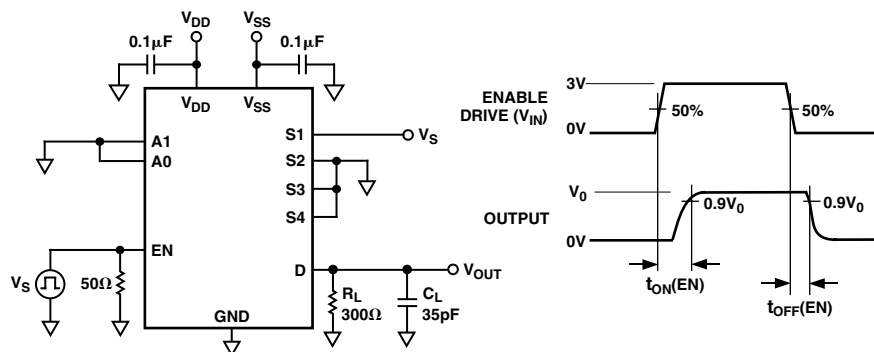
Test Circuit 3. On Leakage



Test Circuit 4. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

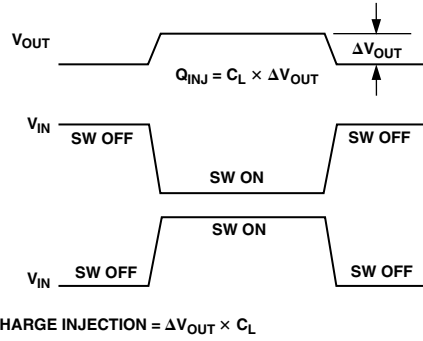
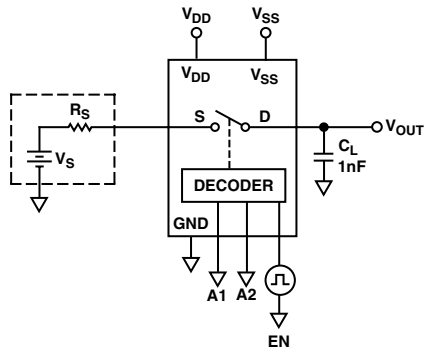


Test Circuit 5. Break-Before-Make Delay, t_{BBM}

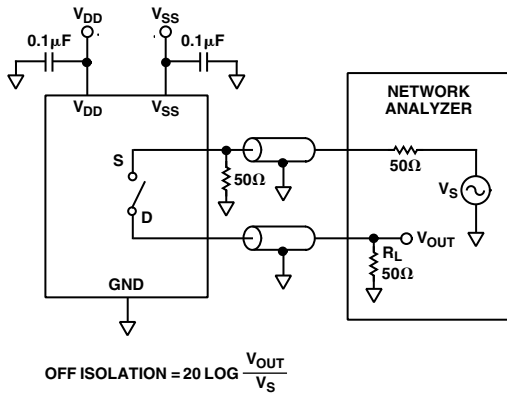


Test Circuit 6. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$

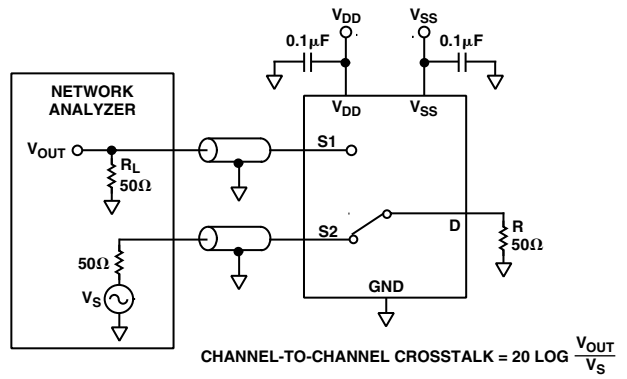
ADG604



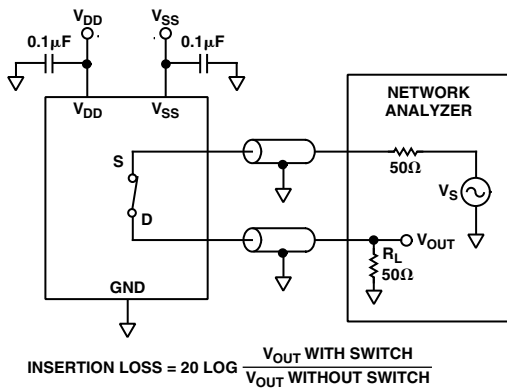
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation

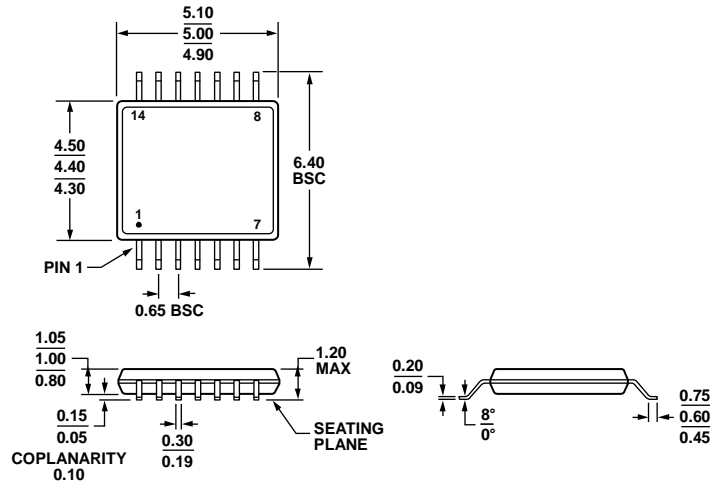


Test Circuit 10. Channel-to-Channel Crosstalk



Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 1. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061906-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG604YRUZ | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 |
| ADG604YRUZ-REEL7 | -40°C to +125°C | 14-Lead Thin Shrink Small Outline Package [TSSOP] | RU-14 |

¹ Z = RoHS Compliant Part.

REVISION HISTORY

7/2018—Rev. 0 to Rev. A

- Changed Automotive Temperature Range: -40°C to +125°C to Temperature Range: -40°C to +125°C 1
- Deleted Note 2, Dual Supply Table; Renumbered Sequentially 2
- Deleted Note 2, Single Supply Table; Renumbered Sequentially 3
- Deleted Note 2, Single Supply Table; Renumbered Sequentially 4
- Changed Operating Temperature Range, Automotive (Y Version) to Operating Temperature Range, (Y Version); Absolute Maximum Ratings Table 5
- Updated Outline Dimensions..... 11
- Moved Ordering Guide 11
- Changes to Ordering Guide..... 11

2/2002—Revision 0: Initial Version

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[ADG604YRUZ](#) [ADG604YRUZ-REEL7](#)