

MOSFET

OptiMOS™ 5 Power-MOSFET, 30 V

Features

- Optimized for high performance buck converters
- Monolithic integrated Schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5$ V
- 100% avalanche tested
- N-channel
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

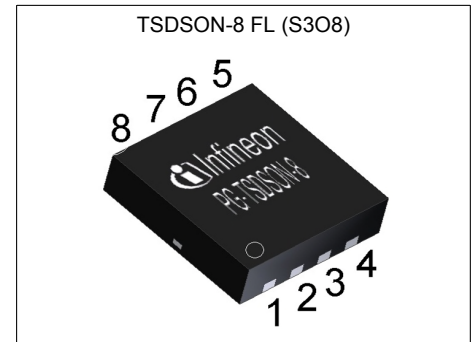
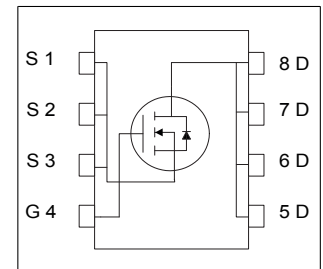


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	2.0	m Ω
I_D	123	A
Q_{OSS}	18	nC
$Q_G(0V..4.5V)$	11.4	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSZ0501NSI	PG-TSDSON-8 FL	0501NSI	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	123	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ K/W}^2)$
		-	-	78		
		-	-	110		
		-	-	70		
		-	-	25		
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	492	A	$T_C=25\text{ °C}$
Avalanche current, single pulse ⁴⁾	I_{AS}	-	-	20	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	40	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	50 2.1	-	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=60\text{ K/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.5	K/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	60	K/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$, $I_D=10\text{ mA}$
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	$I_D=10\text{ mA}$, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	0.5	mA	$V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
		-	2	-		$V_{DS}=24\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1	2.5	m Ω	$V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
		-	1.7	2.0		$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	1.4	2.3	Ω	-
Transconductance	g_{fs}	55	110	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	1500	2000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	540	730	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	36	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	4	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	22	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	3	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

¹⁾ Defined by design. Not subject to production test

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3.9	-	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.5	-	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	2.9	-	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	4.3	-	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ²⁾	Q_g	-	11.4	15	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ²⁾	Q_g	-	24	33	nC	$V_{DD}=15\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	10.5	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	Q_{oss}	-	18	-	nC	$V_{DD}=15\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	50	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	492	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.55	0.7	V	$V_{GS}=0\text{ V}$, $I_F=7\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery charge	Q_{rr}	-	5	-	nC	$V_R=15\text{ V}$, $I_F=7\text{ A}$, $di_F/dt=400\text{ A}/\mu\text{s}$

¹⁾ See "Gate charge waveforms" for parameter definition

²⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

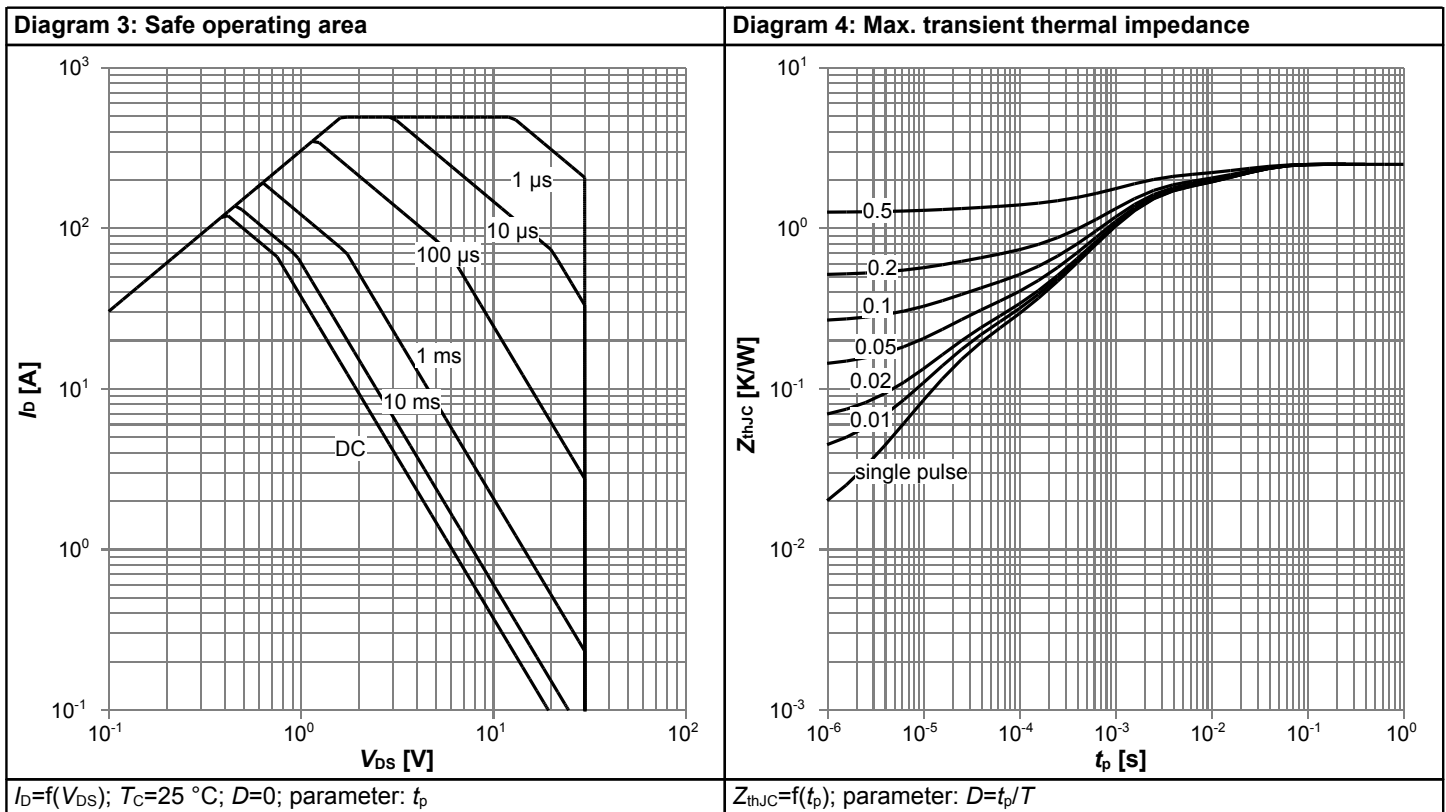
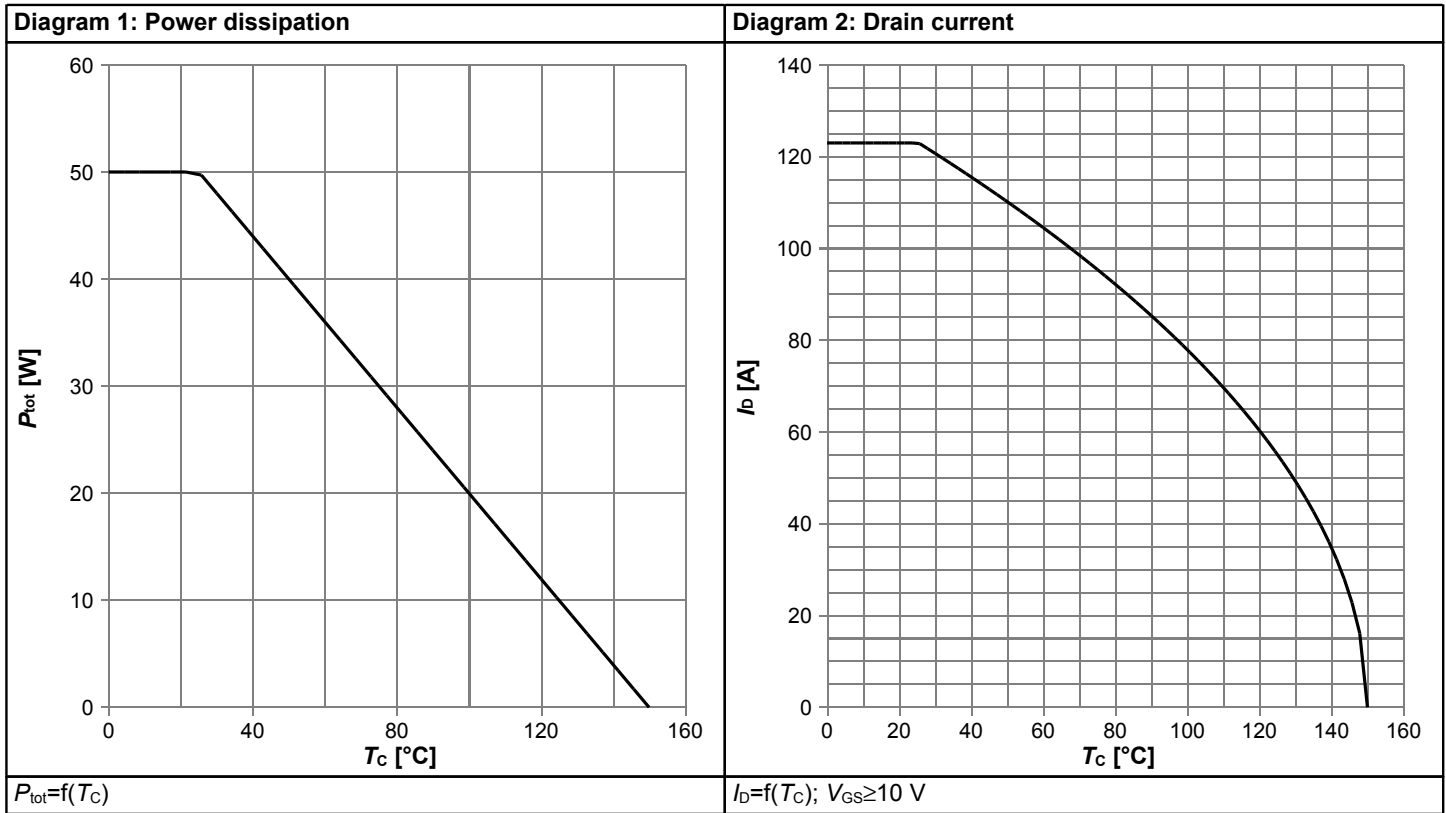
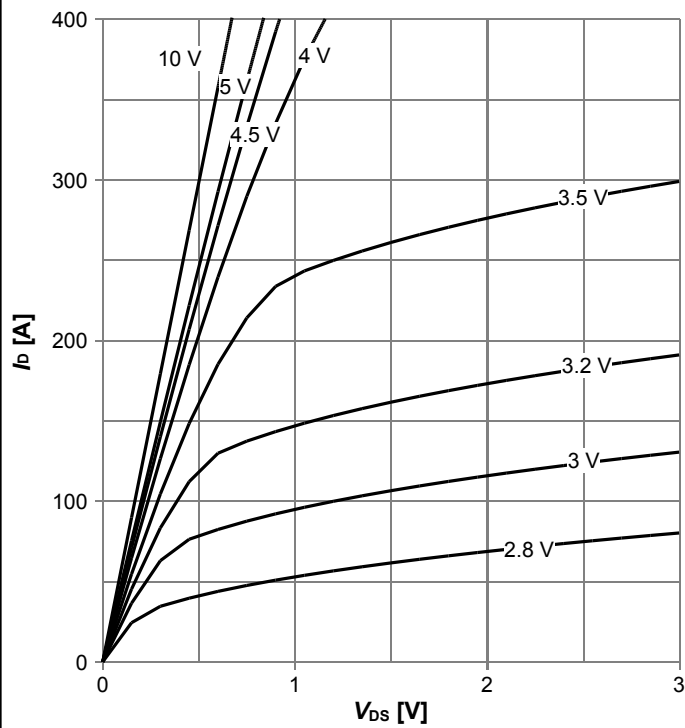
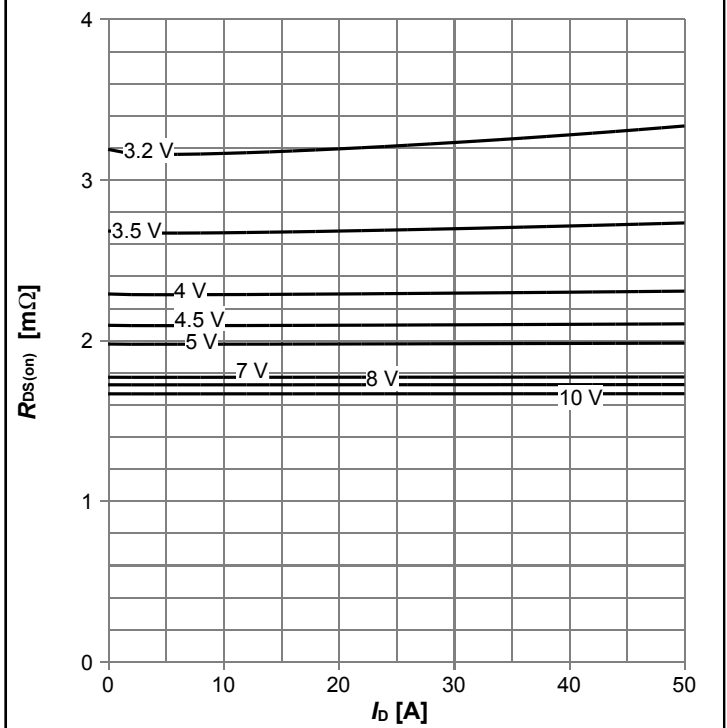


Diagram 5: Typ. output characteristics



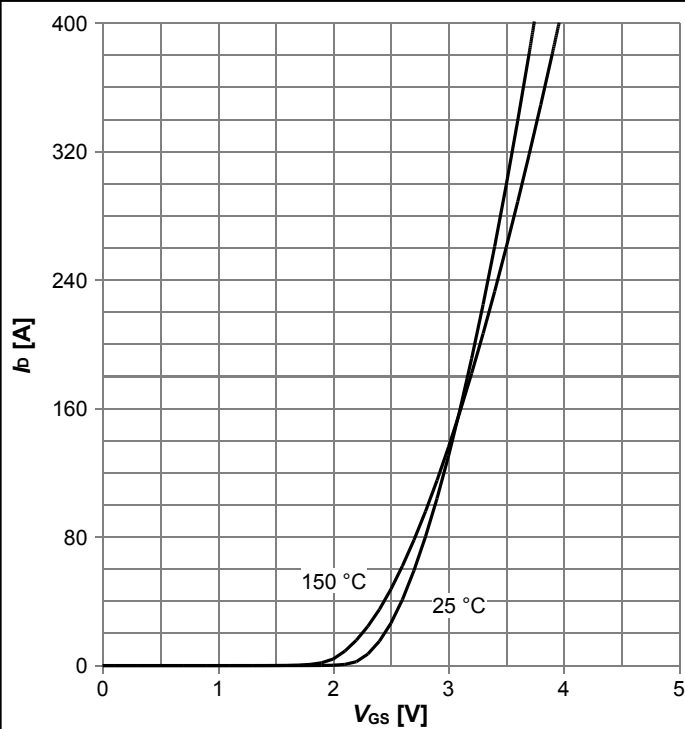
$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



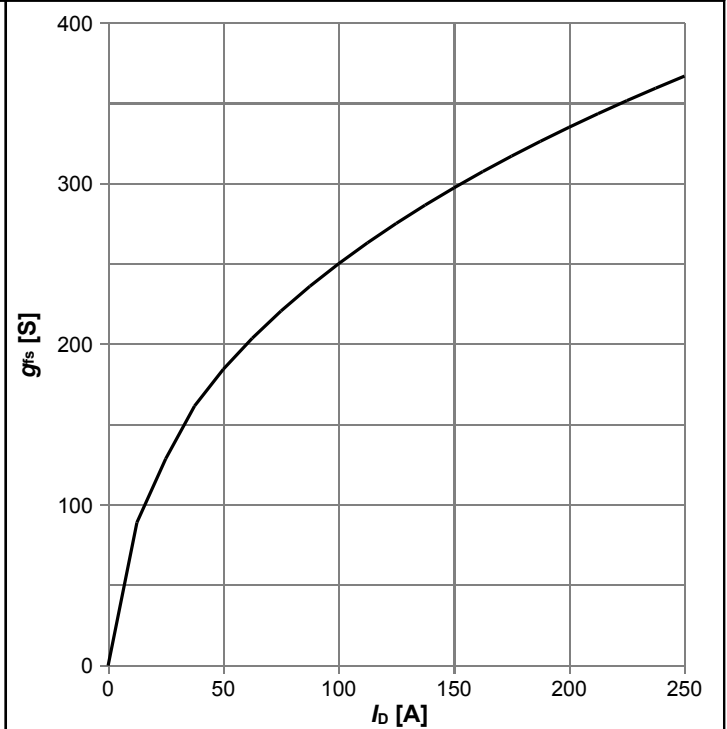
$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



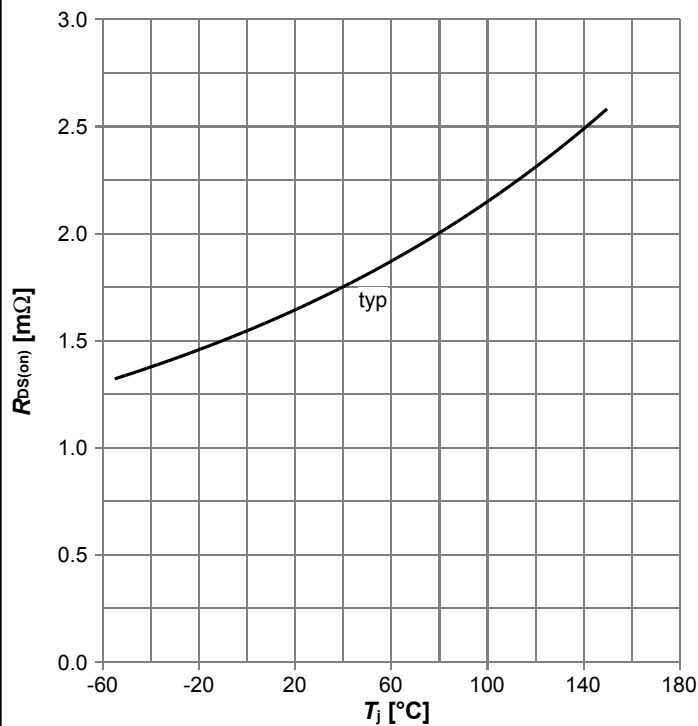
$I_D = f(V_{GS}); |V_{DS}| > 2 \cdot I_D \cdot R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



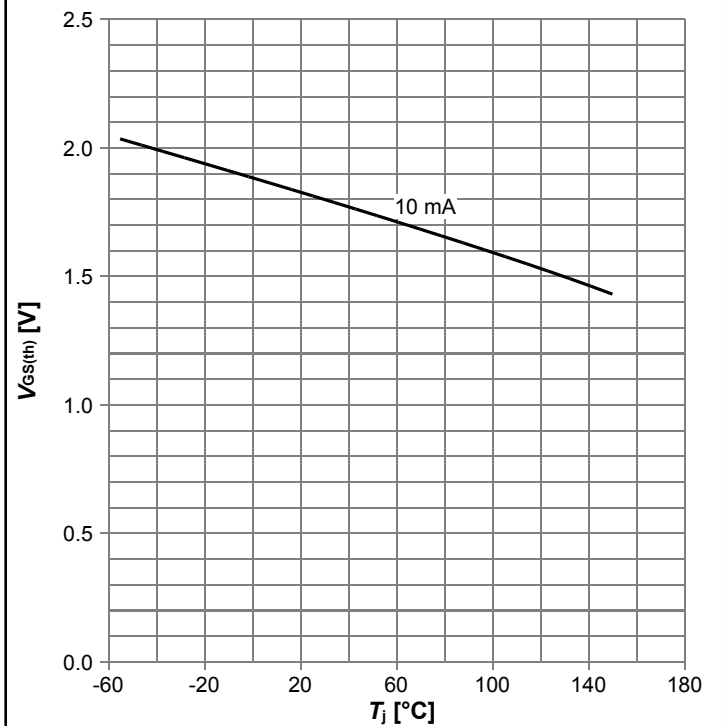
$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



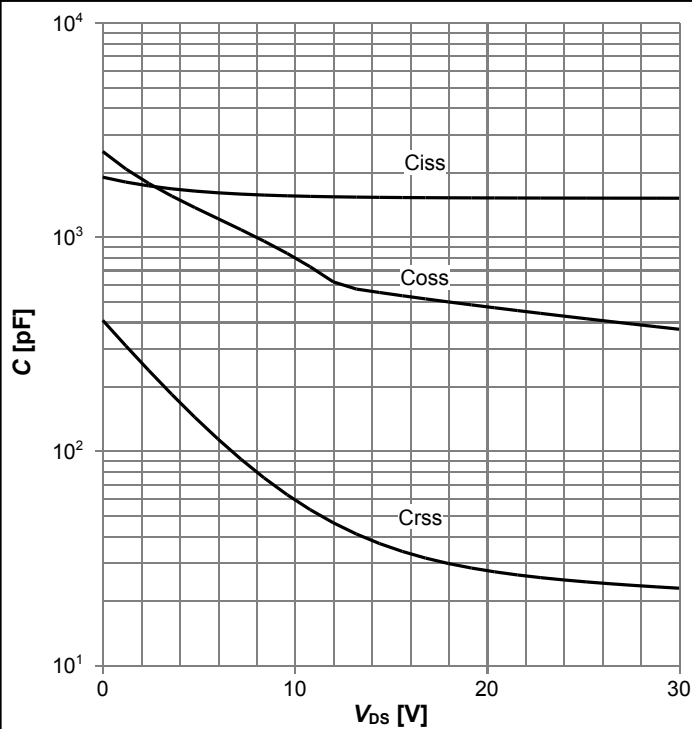
$R_{DS(on)}=f(T_j)$; $I_D=30$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



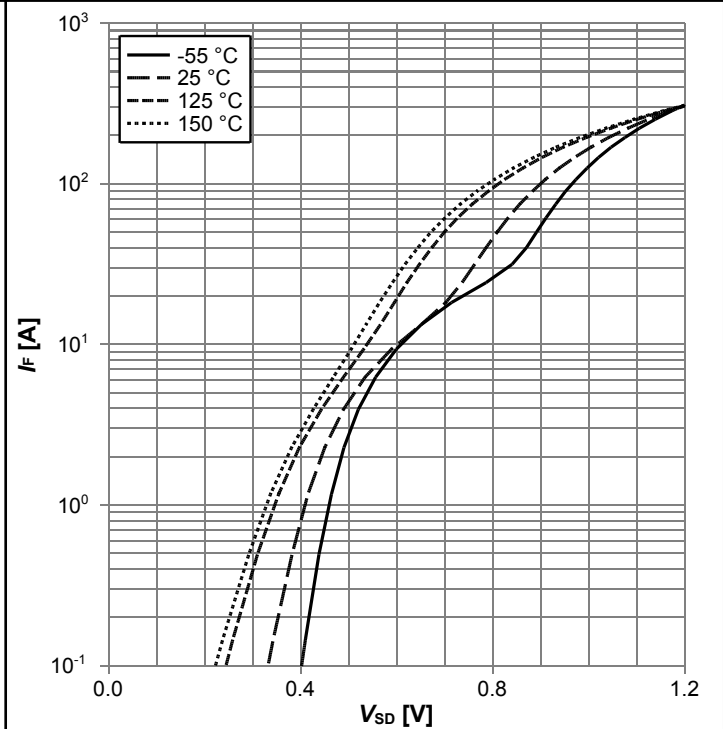
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



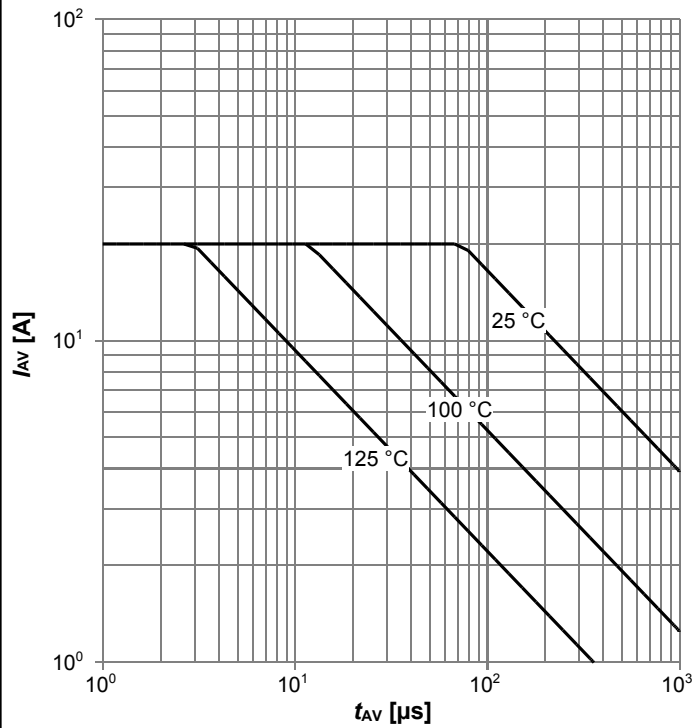
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



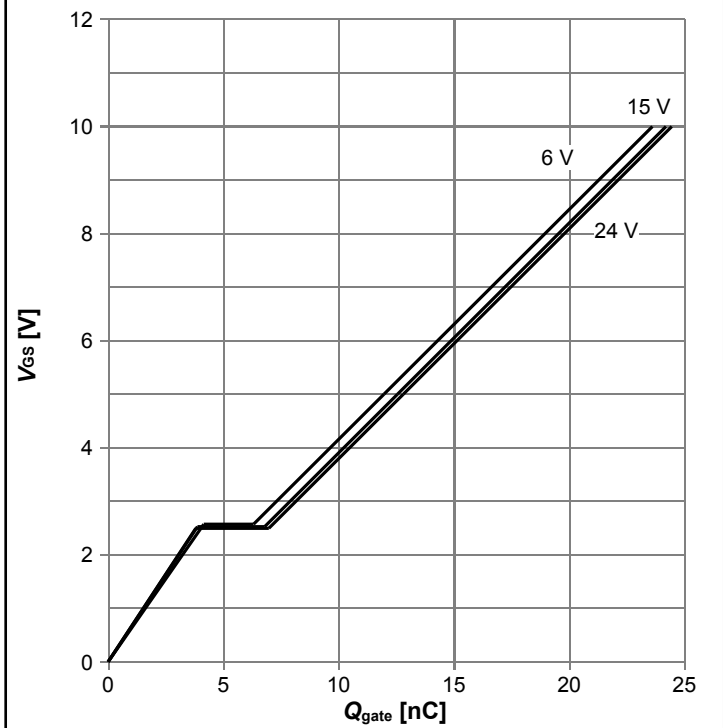
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



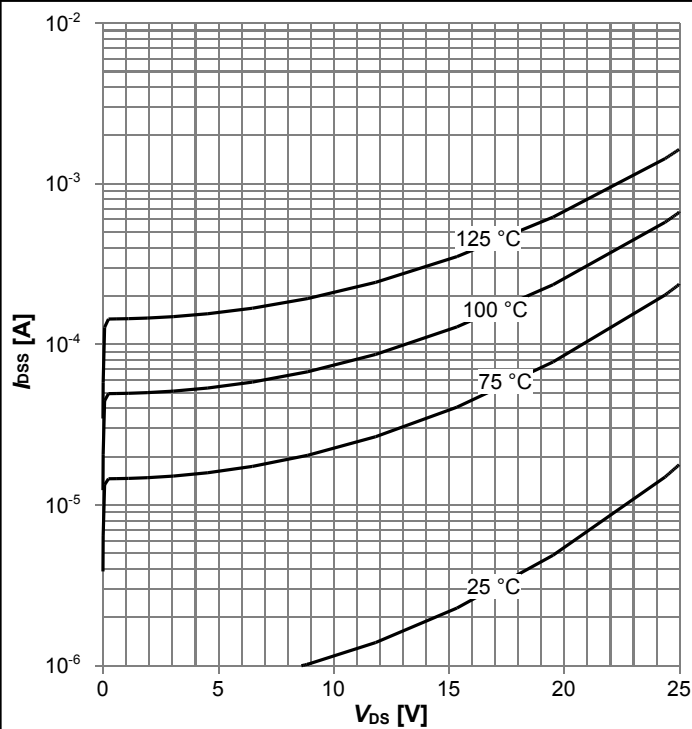
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate})$; $I_D=30$ A pulsed; parameter: V_{DD}

Diagram 15: Typ. drain-source leakage current

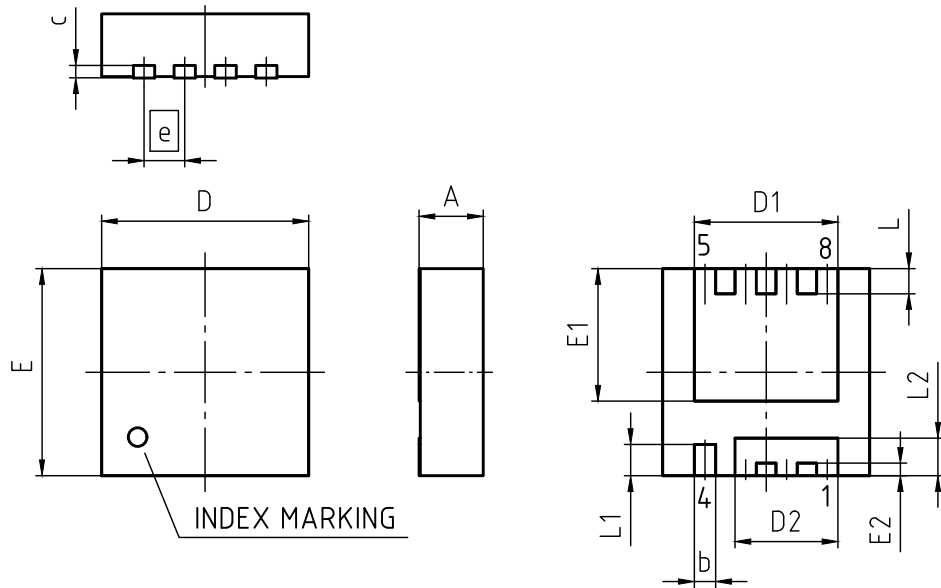


$I_{BSS}=f(V_{DS})$; $V_{GS}=0$ V; parameter: T_j

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TSDSON-8-U03		
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

BSZ0501NSI

Revision: 2020-11-16, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-04-27	Release of final version
2.1	2020-08-13	Update current rating and footnotes
2.2	2020-11-16	Update package drawing

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