High speed CAN Transceivers Application Note

TLE6250G

TLE6250GV33

TLE6251DS

TLE6251G

Author : Stéphane Fraissé

Automotive Power

Never stop thinking

Edition 2006-04-01

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

Attention please!

The information given in this Data Sheet shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

High speed CAN

Revision History: 2006-04-01

Previous Version: none

Page	Subjects (major changes since last revision)

1 Introduction.

The increasing number of electronics equipment in todays cars implies a lot of information exchange. To avoid a massive usage of wires between modules, a digital protocol has been created. This protocol has been named CAN for Controller Area Network. CAN allows communication, to a speed up to 1Mbit/s. To avoid noisy communication in terms of electromagnetic emission, the medium is a twisted pair and the electrical signal is differential. **Figure 1** shows the typical signal of high speed CAN, and the basic reason for low electro-magnetic emission. When CAN_H rises, some parasitic are emitted. In the same time, CAN_L goes down, in the same proportion. The sum of these parasitics are 0, so to say the electromagnetic emission is limited.

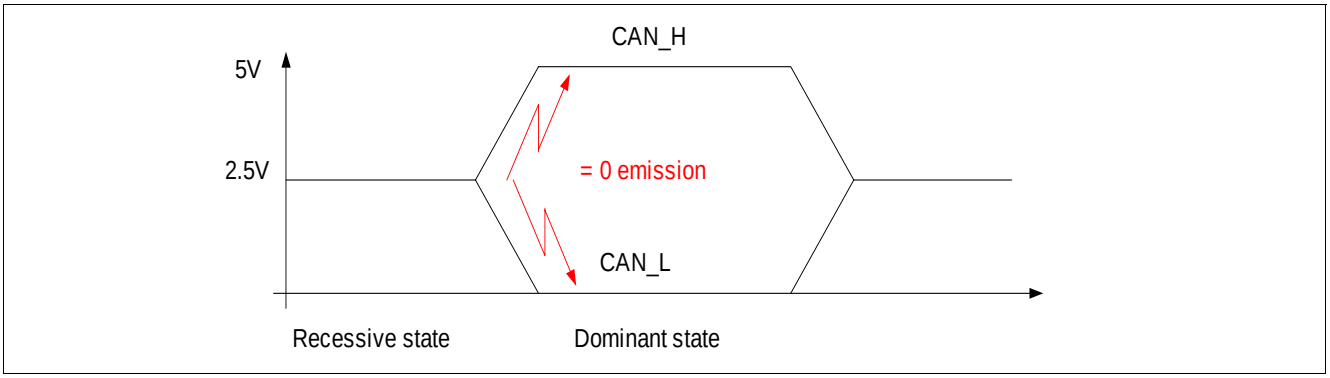


Figure 1 Typical high speed CAN signal

This application note is intended to present the high speed CAN application and the usage of Infineon CAN transceivers in these applications. This document refers to international standard ISO 11898-2 **[5]**, SAE J2284, ISO 11898-5 **[6]**, and well as to the TLE6250G **[1]**,TLE6251DS **[2]**, and TLE6251G **[3]** datasheets.

First part of the document will describes high speed CAN network in the automotive environnement. Then it will focus on transceivers itself for easy interfacing with micro-controller, and will conclude by application hints to successfully reach the challenges of such networks require.

1.1 Recessive Level.

During the recessive state, the signal is specified by the ISO 11898-2 **[5]**and ISO11898-5 **[6]**. The **Table 1** gives the parameters (extract of the ISO11898-2 **[5]** table 4).

Table 1 DC parameters for recessive output of CAN node

Parameter	Notation	Unit	min	Nom	Max	Condition
Output bus voltage	V_{CAN_H}	V	2,0	2,5	3	no load
	V_{CAN_L}	V	2,0	2,5	3	
Differential output bus voltage	V_{diff}	mV	-500	0	50	no load
Differential input voltage	V_{diff}	V	-1		0,5	

1.2 Dominant level.

During the dominant state, the signal is specified by the ISO 11898-2 **[5]** and ISO11898-5 **[6]**. The **Figure 2** shows the definition of the parameters, described in **Table 2** (extract of the ISO11898-2 **[5]** table 5).

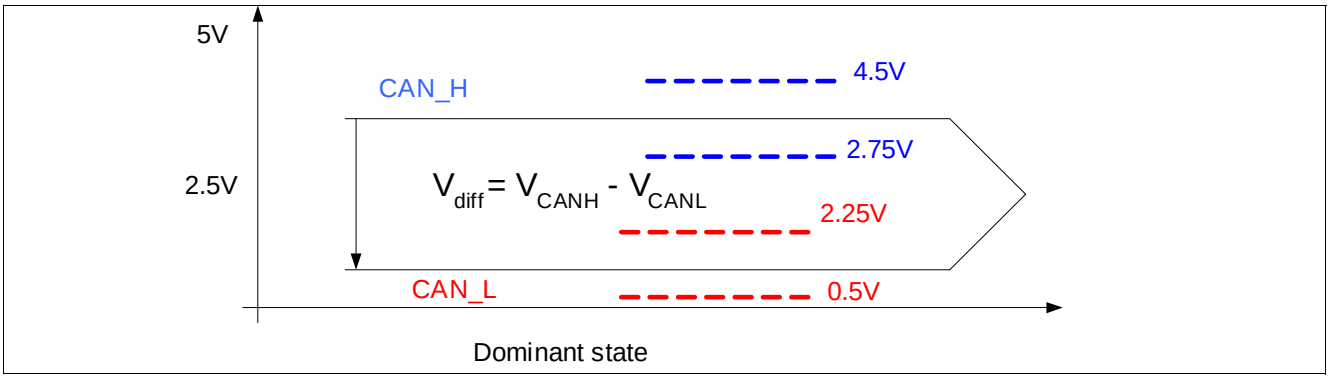


Figure 2 Dominant level

Table 2 DC parameters for dominant output of CAN node

Parameter	Notation	Unit	min	Nom	Max	Condition
Output bus voltage	V_{CAN_H}	V	2,75	3,5	4,5	load R_L / 2
	V_{CAN_L}	V	0,5	1,5	2,25	
Differential output bus voltage	V_{diff}	V	1,5	2	3	load R_L / 2
Differential input voltage	V_{diff}	V	-0,9		5	load R_L / 2

1.3 Driver symmetry.

In the ISO11898-5 **[6]**, the driver symmetry is specified. This is to improve the EMC behaviour. The **Figure 3** shows the definition of the parameter, unsymmetry appears often when CAN_H and CAN_L are not perfectly synchronized. The **Table 3** gives the specified values.

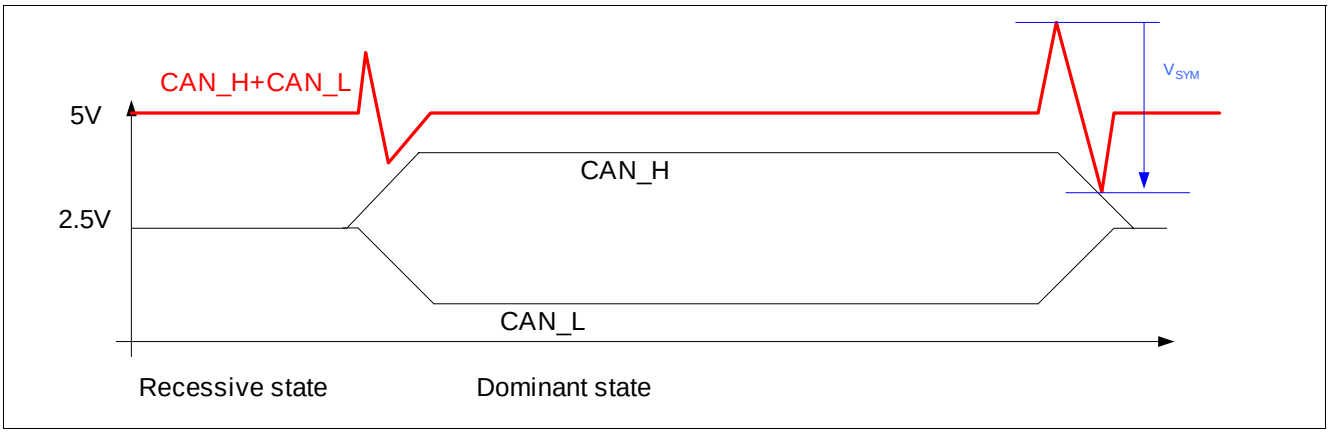


Figure 3 Common mode voltage definition.

Table 3 Driver symmetry

Prameter	Notation	Unit	Min	Nom	Max	Condition
Driver symmetry	V_{SYM}	V	0,9	1	1,1	Load = 120Ω, 4.7nF F = 250kHz,

2 In Vehicle Network.

2.1 Type of supplies in the vehicle.

According to car makers requirements, the modules can be supplied or not supplied when car is parked. Main reason for unsupplied modules is current saving for the car's battery, when supplied modules can quickly wake up on CAN request, or monitoring discretes inputs like switches.

2.1.1 Unsupplied modules in the parked car. (Clamp 15)

Unsupplied modules are mainly under hood applications as engine control unit. When the car is parked, a main switch cut the battery supply off (see **Figure 4**). This supply line is often called Clamp 15 or KL15 (Klemme 15 in German). Since the battery isn't present, the voltage regulator is off and the transceiver is unsupplied. We will see later on (**Chapter 5.2**) the basic requirements of such applications for the transceivers.

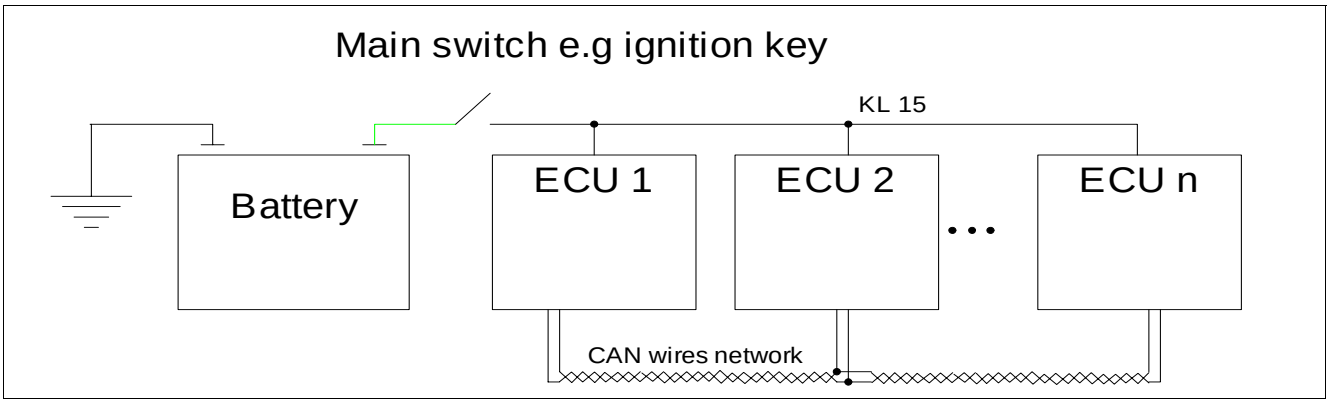


Figure 4 Typical Clamp 15 application

2.1.2 Supplied modules in the parked car. (Clamp 30)

Supplied modules, even when car is parked are mainly requested in the body of the vehicle, as door modules, RF keyless receiver, etc... The battery voltage comes directly to the module. This supply line is often called Clamp 30 or KL30 (Klemme 30 in German). Since the battery is present, the LDO is or can be ON, and the transceiver is or can be supplied. We will see in the **Chapter 5.2** the basic requirements of such applications for the transceivers.

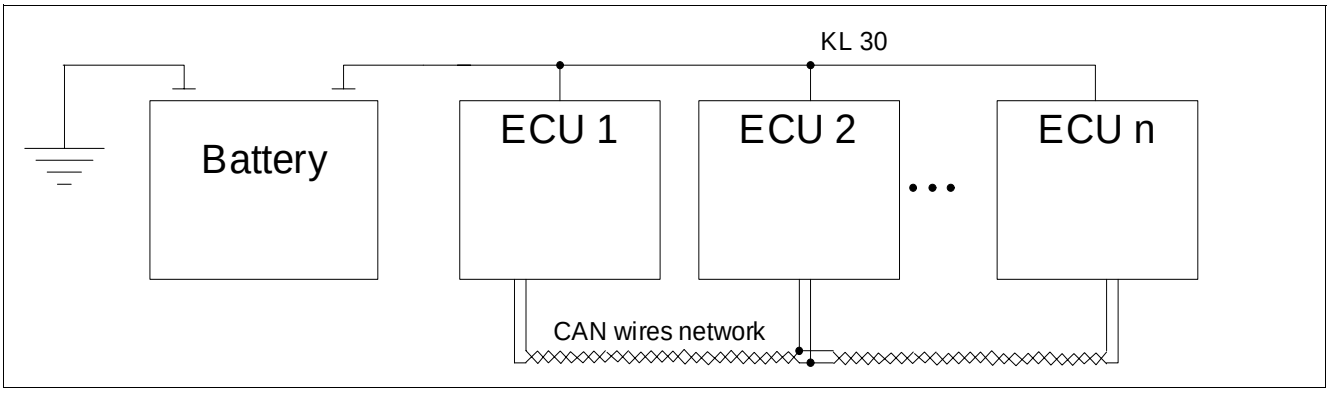


Figure 5 Typical Clamp 30 application

2.1.3 Mixed network.

It´s also possible to mix the two solutions. Some modules are CAN or discretes switches wakeable, some are only supplied by a main switch. **Figure 6** shows the application principle. The **Chapter 5.2** describes the challenges to achieve with this kind of mixed network.

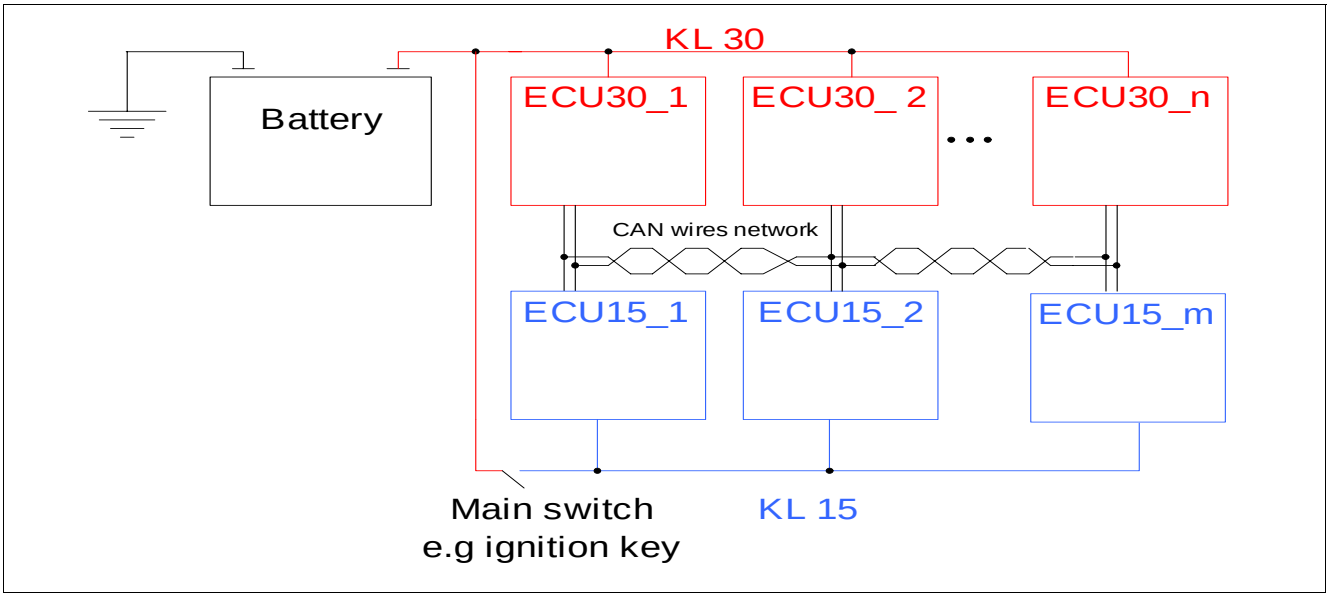


Figure 6 Mixed CL15 and CL30 network

2.2 Ground line.

The ground line has a big influence on the electronic equipment, especially for communication purposes, since the physical layer depends on voltage level. The 0V reference is the chassis of the vehicle. The ground pin of the module might not be at this chassis reference. If the ground is shifted between modules, each transceivers are at different ground level and so communication mismatch might occurs.

The ground line also influences the EMC and ESD performance of the module and of the vehicle. See **Chapter 6** and **Chapter 7**.

2.2.1 High current applications.

The ground reference of the vehicle is the chassis. Some applications like power-steering, starter-alternator, etc... have a huge current to ground (80Amps or even higher). Moreover, the current is often not DC. Special consideration should be taken with respect to ground cable and its resistor, as well as its inductance has to be taken into account. **Figure 7** shows a typical high current module. Wiring companies often give the resistance of the cable, in Ω/km. A standard 1mm² cross section cable has a resistance of about 20 Ω/km. A 80 Amps application with a 1m cable means then a ground shift of about 1.6V, without considering the connectors, and PCB traces resistance. This voltage drop cannot be neglected. The **Figure 7** also shows a possible voltage drop, inside the module due to the PCB trace. This will mainly affect the ESD and EMC robustness. Please refer to the **Chapter 6** and **Chapter 7**.

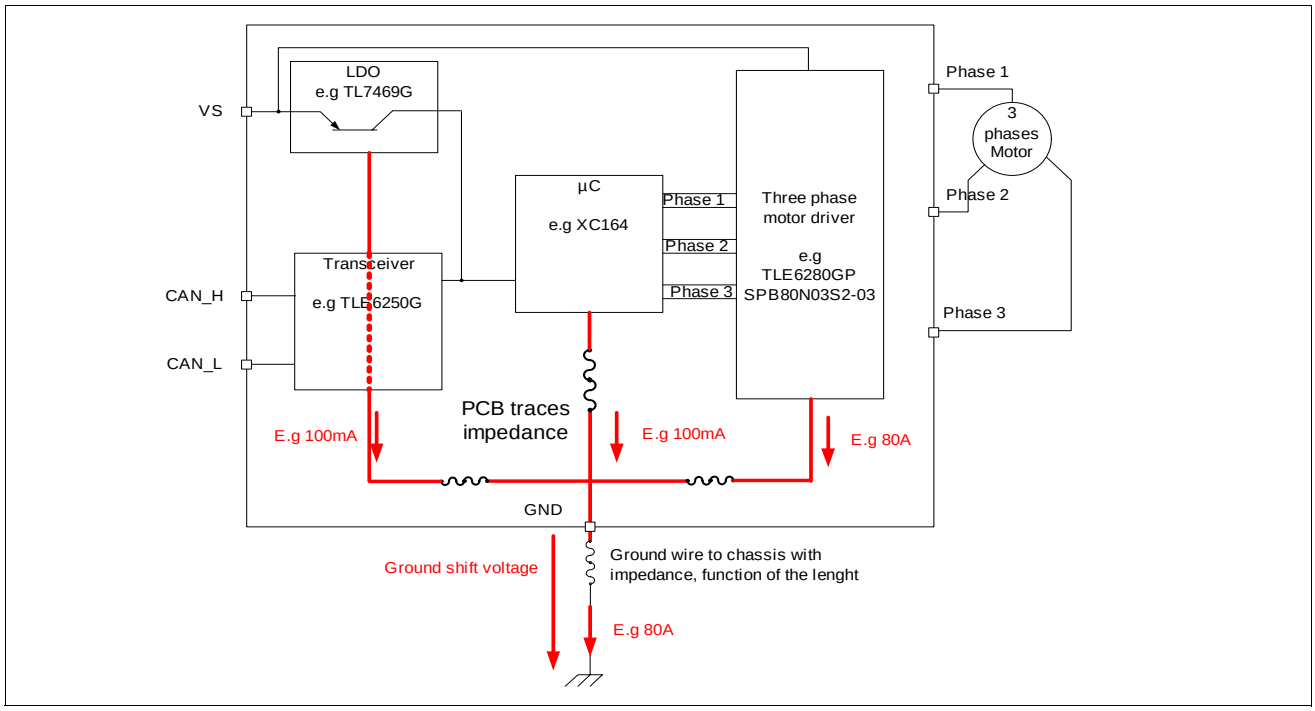


Figure 7 Typical high current application

2.2.2 Low current application.

Most of applications are low current applications, where the voltage drop in the ground wire is close to zero and so the ground current can be neglected.

2.3 The Transceiver in the automotive environment.

This chapter describes the behavior of the transceivers in the automotive environment, meaning for example, loss of ground, low battery voltage, cranking pulse, load dump, etc... Each car maker (OEM) specify its own environmental specification so that application note cannot cover all cases, but gives application hints on how to deal with these issues.

2.3.1 Low battery voltage.

This situation happens mainly during the cranking of the engine. Except for the TLE6251G, the transceivers are not directly connected to the battery voltage. The transceiver is then mainly dependant on the voltage regulator behavior. Please refers to **Chapter 3.3.8**, for the voltage regulator's choice.

2.3.1.1 TLE6250G.

The TLE6250G has no special under voltage function integrated. To get the device working and warranted, the V_{cc} pin should be higher than the minimum operating voltage specified in the data sheet **[1]** so 4.5V. Below this value, it is observed that the device is still working, sending and receiving data, but the parameters are not warranted and not compliant to the ISO standard. The recessive voltage is proportional to the V_{cc}, typical half V_{cc}. For example, with a V_{cc} of 4V, the recessive voltage will be 2V typical. It is then recommended to monitor the battery voltage by an external circuitry or early warning function of the voltage regulator, to avoid miscommunication during this time.

When the V_{cc} voltage is too low, typical 3V, the device is in OFF state, comparable to unsupplied.

2.3.1.2 TLE6251DS.

The TLE6251DS doesn't integrate any under voltage function and behaves as the TLE6250G. Please refers to **Chapter 2.3.1.1**.

2.3.1.3 TLE6251G.

The TLE6251G integrates undervoltage detection for all supply pins, Vs, V_{cc} and $V_{\mu C}$. If one of these pins see a voltage below the specified minimum values (see **[3]**) , the device goes after a filtering blanking time to standby mode, in case Vs is in undervoltage , or to Sleep Mode in case of undervoltage detection on V_{cc} or $V_{\mu C}$. Please refers to **Figure 8** for explanation of Vs. Please also refers to **Chapter 4.3.5.2**, for undervoltage detection on $V_{\mu c}$/ V_{cc}.

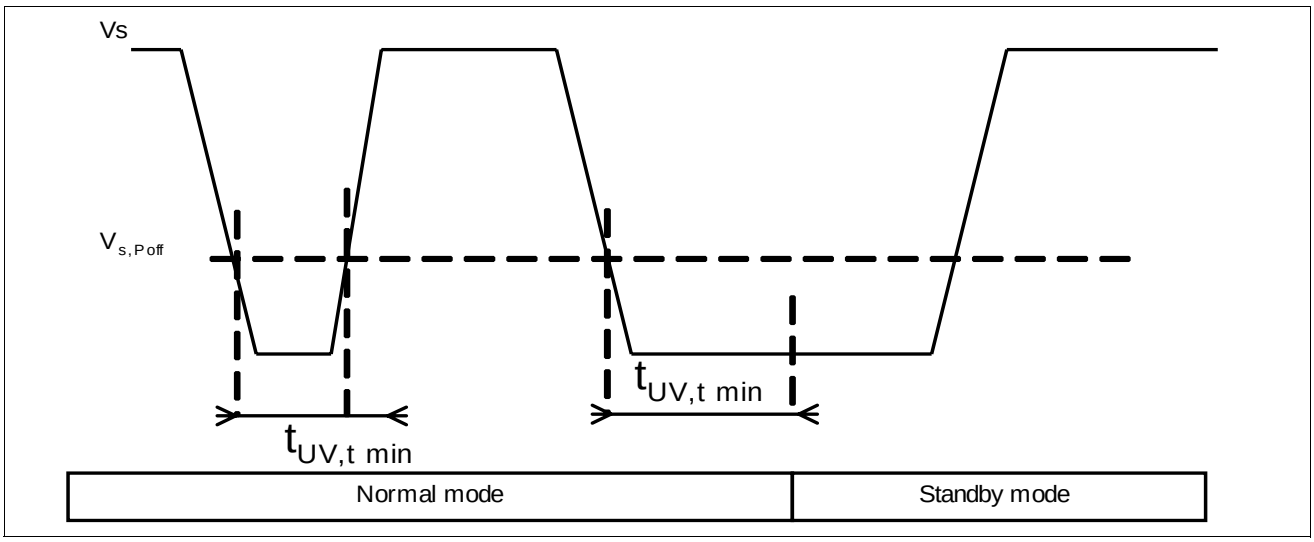


Figure 8 Undervoltage detection mechanism for Vs.

Since the undervoltage mechanism is below the minimum operating voltage (for production spread and temperature dependancy reasons), between these under voltage states and minumum operation, the device is active and operates, without warranted conformity to the ISO standard. Last but not least, the Vs undervoltage detection threshold is buffered with an hysteresis.

2.3.2 High battery voltage.

We discuss here all high battery voltage conditions, like jump start, load dump, or highest nominal battery voltage. The voltage should not exceed the absolute maximum rating. Otherwise, the device could be damaged or destroyed. The high battery voltage as well as load dump are voltage regulator issues. Since the dissipated power in the LDO is directly proportional to the input voltage, (see **Equation (1)**), the issue is to get rid of the power in the LDO.

Power loss in a LDO: $P_{loss} = (Vbat - V_{cc}) * I_{out} + V_{bat} * I_q$ (1)

I_{out} is the output current of the LDO.

I_q is the current consumption of the LDO (values can be found in the LDO datasheet).

If the power dissipation challenge is passed, the application will work properly.

2.3.2.1 TLE6250G / TLE6251DS.

For 12V applications, the concern of the high operating battery voltage is limited to two very special cases, double failure (CAN_H or CAN_L shorted to battery and high voltage operation). The absolute maximum rating warranties no destruction of the device because the highest voltage seen is the 34V load dump.

The only concerns is the power dissipation, when CAN_L is shorted to battery. The device limits the current, but with battery voltage, the temperature will increase dramatically and the device might go into thermal shutdown. (failure case 3 and 6, see **Figure 30**).

2.3.2.2 TLE6251G.

In addition to the TLE6250G and TLE6251DS (see **Chapter 2.3.2.1**) remarks, the TLE6251G includes an high side switch. In case of high battery voltage, the power loss in the switch cannot be neglected and so it is recommended to not connect a low ohmic load on the INH output. The INH pin should be considered as a high voltage signal only. See also **Chapter 4.3.8**.

2.3.3 Reverse polarity.

Same remark as for the **Chapter 2.3.2**. The issue is mainly carried by the voltage regulator. Anyway, some possible current path exists and has to be described in the following sections.

2.3.3.1 TLE6250G / TLE6251DS.

A possible failure would be a current flowing into the CAN_L output stage DMOS, due to its parasitic body diode. To avoid this, the TLE6250G and TLE6251DS includes in serial a diode on the bus output lines. Please see block diagrams of the devices in the data sheets **[1] [2] [3]**.

2.3.3.2 TLE6251G.

The TLE6251G includes a P channel DMOS high side switch (pin INH). The maximum reverse battery voltage the device can withstand is very small (-300mV)**[3]**. It is then necessary to protect the Vs pin of the TLE6251G with a diode, preferably Schottky diode to get rid of the low voltage issue (**Chapter 2.3.1**). The power loss in this diode is negligible, since the Vs pin doesn't need a high current, whatever the mode the device is. It is then suggested to use the diode in common with the voltage regulators.

2.3.4 Short circuit on the bus.

Unfortunatly, the short circuit is a problem which can occur in the vehicle when the signal goes out the electronic module. All cases of short circuit are described in the **Figure 30**. The transceiver family from Infineon withstand all these cases, but communication cannot be warranted anymore. The **Chapter 3** describes in details the resulting current to be handled by the voltage regulator.

2.3.4.1 Termination resistors case in short circuit to Vbat.

In case CAN_H is in short circuit to Vbat, (failure case 6, see **Figure 30**), the power loss in the termination resistors has to be taken into account. The **Figure 9** shows the path of the current, in the case the termination is splitted (2x60Ω or 120Ω). Purpose of the Split is described in **Chapter 5.2**. The transceiver will limit the current to the I_{CANL_SC} value, if the battery voltage is higher than 12V.

Power loss in the resistor : $1/2 \times R_{termination} \times I_{CANL\_SC}^2$. (2)

The coefficient 1/2 comes to the ratio recessive dominant. See also **Chapter 3.1.4**

According to **Equation (2)**, the power loss in the 60Ω resistors will be at an average of 300mW and in the 120Ω resistor an average of 600mW. This power has to be taken into account when designing the network termination resistors.

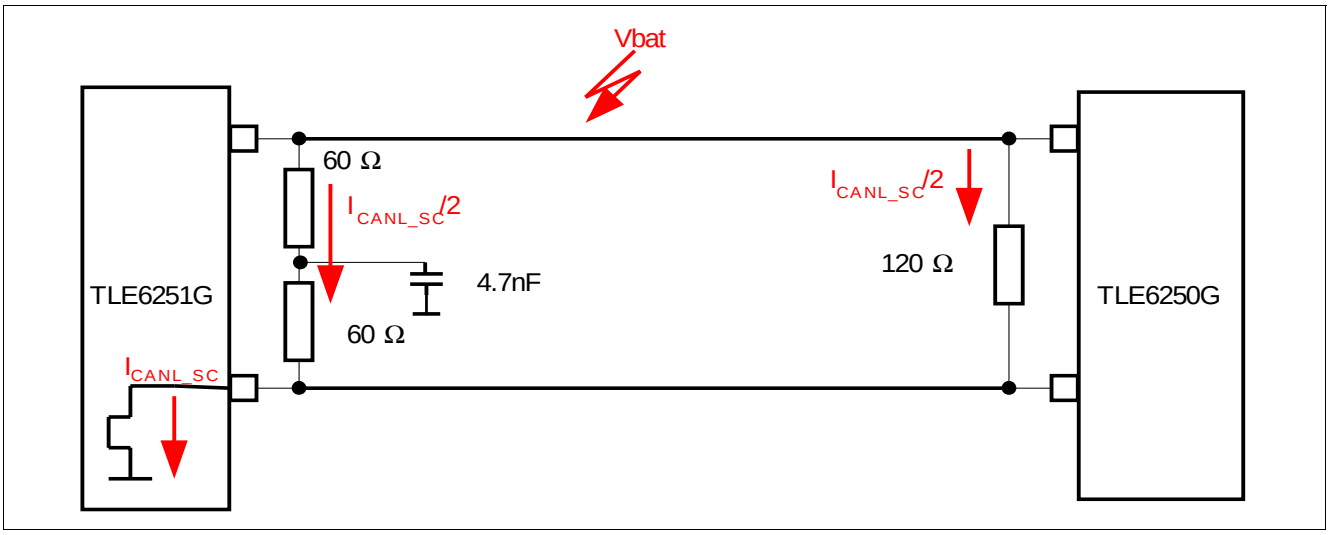


Figure 9 Current in the termination resistors in case of short circuit to Vbat.

Please also notice that in case of CAN_H shorted to Vbat, due to the voltage drop in the resistors, it is possible to see an “appearing” permanent dominant signal.

2.3.5 Temperature.

The Infineon transceiver family is qualified from -40°C to 150°C, as required by the automotive standard. The **Chapter 3** will show the power consumption of the devices, in the different cases.

2.3.6 Ground shift.

In the **Chapter 2.2** we have seen the influence on the ground line for the module. We will now describe the application of interfacing an high current application and a low current application. **Figure 10** shows an application with one ground shift module, in connection with one not connected. We limit the drawing to two modules for simplification purpose, the description remains valid with several modules.

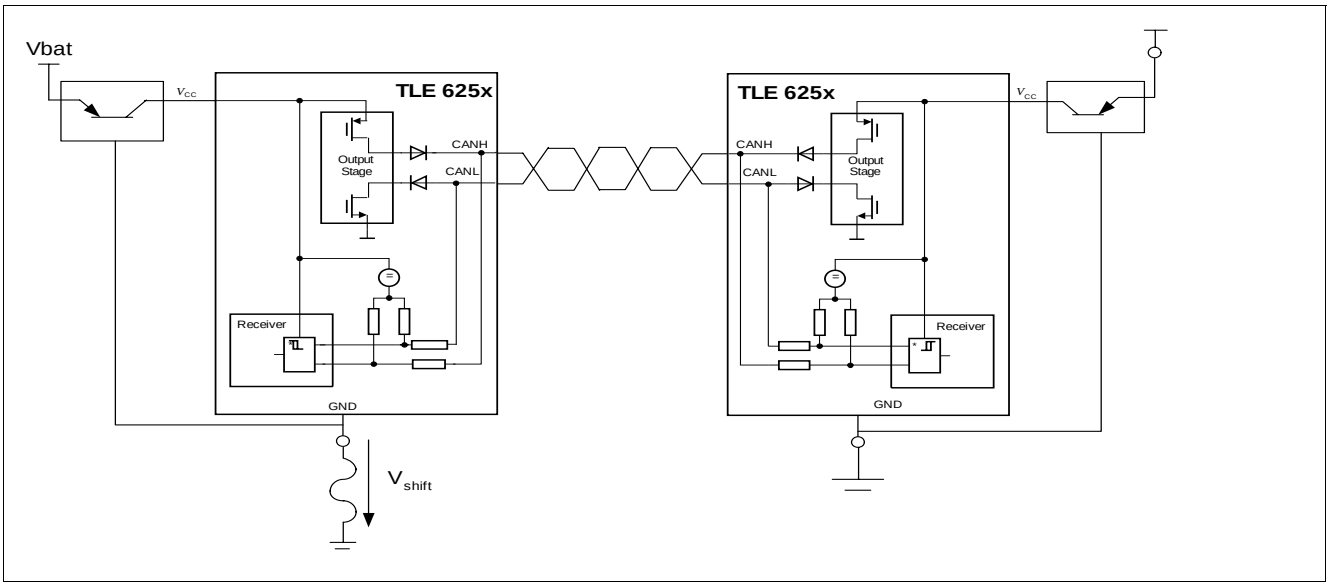


Figure 10 System with one ground shift event

When the module subjected to a ground shift is transmitting, the CAN_H and CAN_L output stages of receiving nodes are OFF. In other words, the receivers for both CAN_H and CAN_L are modeled as resistors to ground.

The values can be found in the datasheet of the respective products considered, under the name R_i. Since the sender has its ground shifted to a V_{shift} value, the recessive level V_{rec} seen from the chassis ground is no longer 2.5V typical but V_{rec} + V_{shift}. The same shift has to be taken into account for the dominant signal. This voltage is the voltage seen by the receiver. The Infineon transceivers are differential transceivers, with a wide common mode range. The CAN_H and CAN_L DC value are not of primary importance, if below the absolute maximum rating. Only the difference voltage (CAN_H - CAN_L) is taken into account by the receiver. **Figure 11** shows a typical CAN signal with a DC ground shift of +2V, and **Figure 12** shows a rough ground shift due to high inrush in the application load. In both cases, the communication remains excellent.

The recessive system level when the ground shifted module is sending, is equaled to the mean value of all transceivers recessive voltages. **Equation (3)** gives the value of the system recessive voltage in that case.

Vrec = [(Vrec_1+ Vshift_1) + (Vrec_2 + Vshift_2) + ... (Vrec_n + Vshift_n)] / n (3)

n is the number of connected modules.

Vrec_1, 2..n are the specific recessive level of the transceiver on nodes 1, 2, ...n

Vshift_1, 2, ... n are the specific ground shift on nodes 1, 2, ...n.

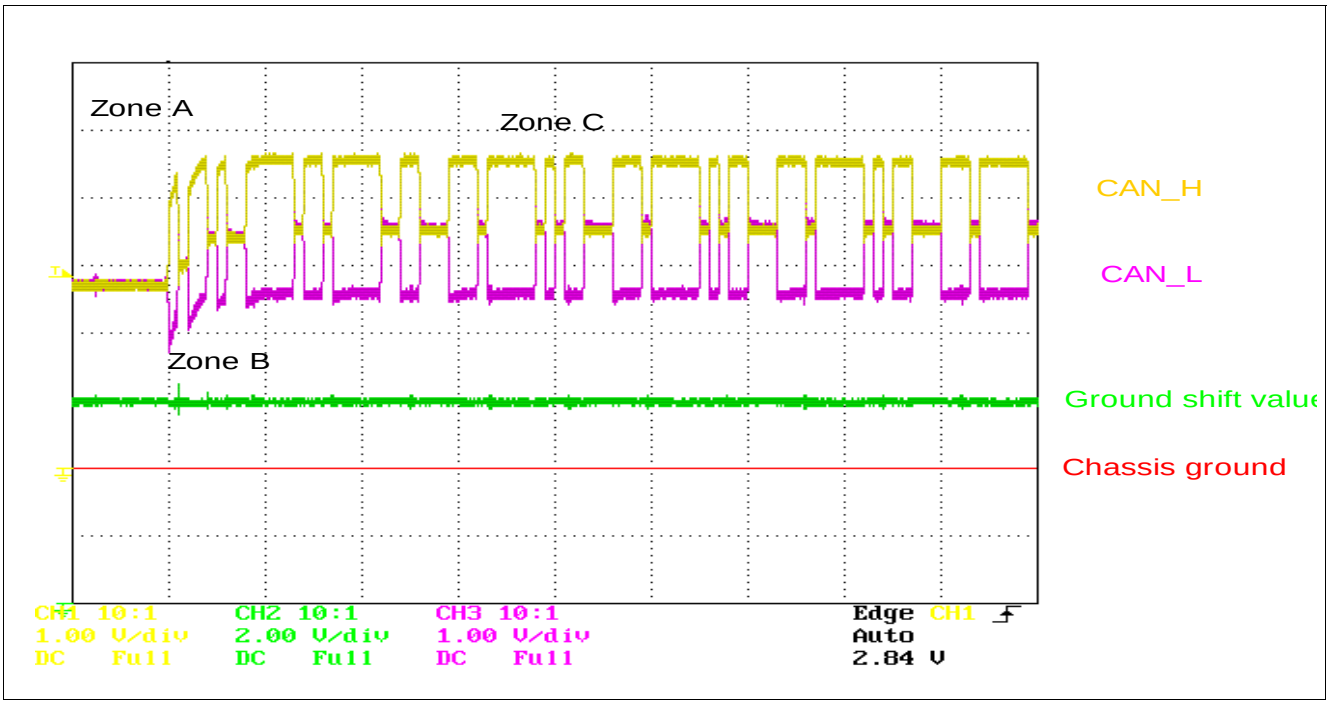


Figure 11 Typical DC ground shift signal.

Zone A : Shows the recessive voltage of the system, so close to the nominal recessive value of 2.5V

Zone B : When the transmitter starts to communicate (zone B), the signal grows quickly, and load the capacitors of the system. (parasitics of the wiring, terminations capacitors, ...).

Zone C : The communication is stabilized, and the recessive voltage is reaching the value, as computed on **Equation (3)**.

It is important to notice that the supply current of the transceiver will increase.

If n represents the number of nodes on the network,

R_{i_n} is the impedance to ground of the CAN_H / CAN_L input for each nodes,

V_{shift} is the ground shift voltage,

The extra supply current is : I_{cc_shift} = V_{shift} / (R_{i_n} / n), assuming all input resistances identical

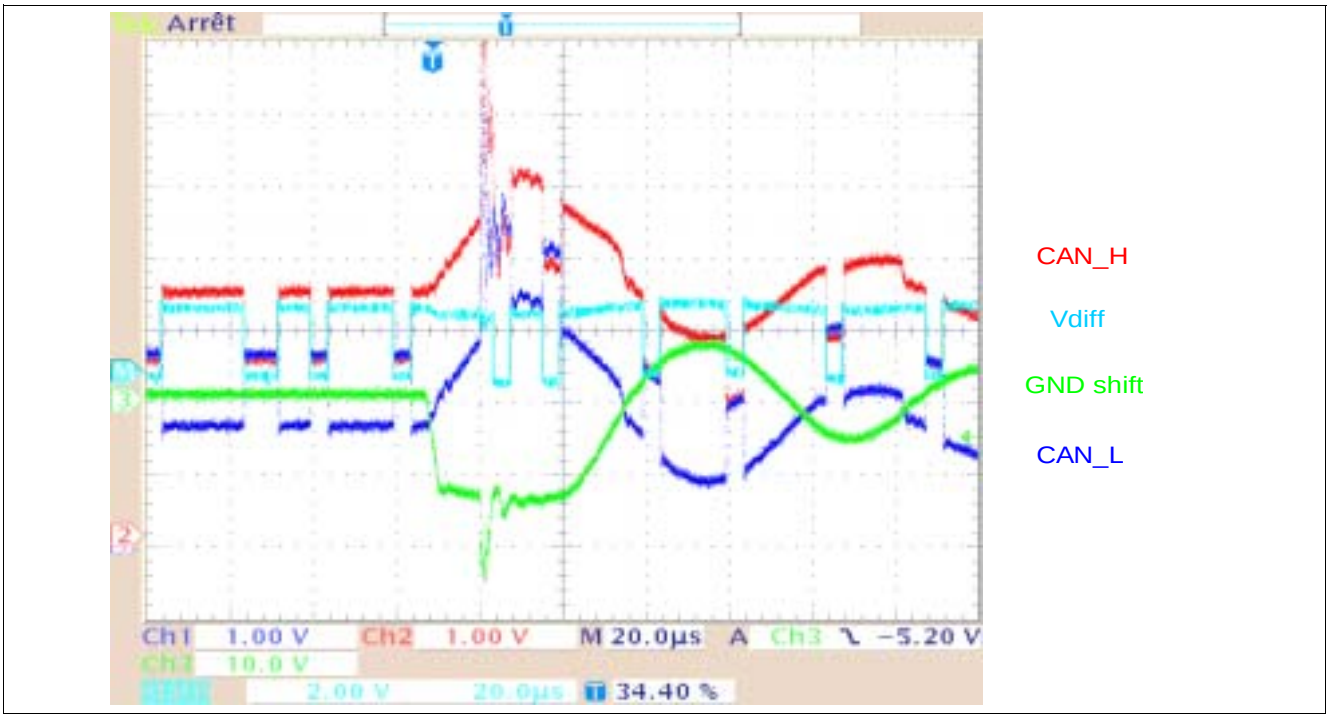


Figure 12 CAN signals with AC ground shift.

2.3.7 Loss of ground.

In case of loss of ground, the voltage regulator output (V_{cc}) might goes to the battery voltage. It means the V_{cc} input of the transceiver might be at the 12V battery potential. The transceiver is of course no longer supplied, so it behaves as unpowered state, but brings a pull-up to battery to the bus, via the input resistors of the receiver. From a system point of view, the behavior is like a short circuit to battery via a weak pull up, the transceiver is the weak pull-up. The CAN signals are no more in conformance with the ISO standard but the communication between the non-affected module remains OK, since the high speed CAN protocol is differential and a limp home functionnality is possible.

I

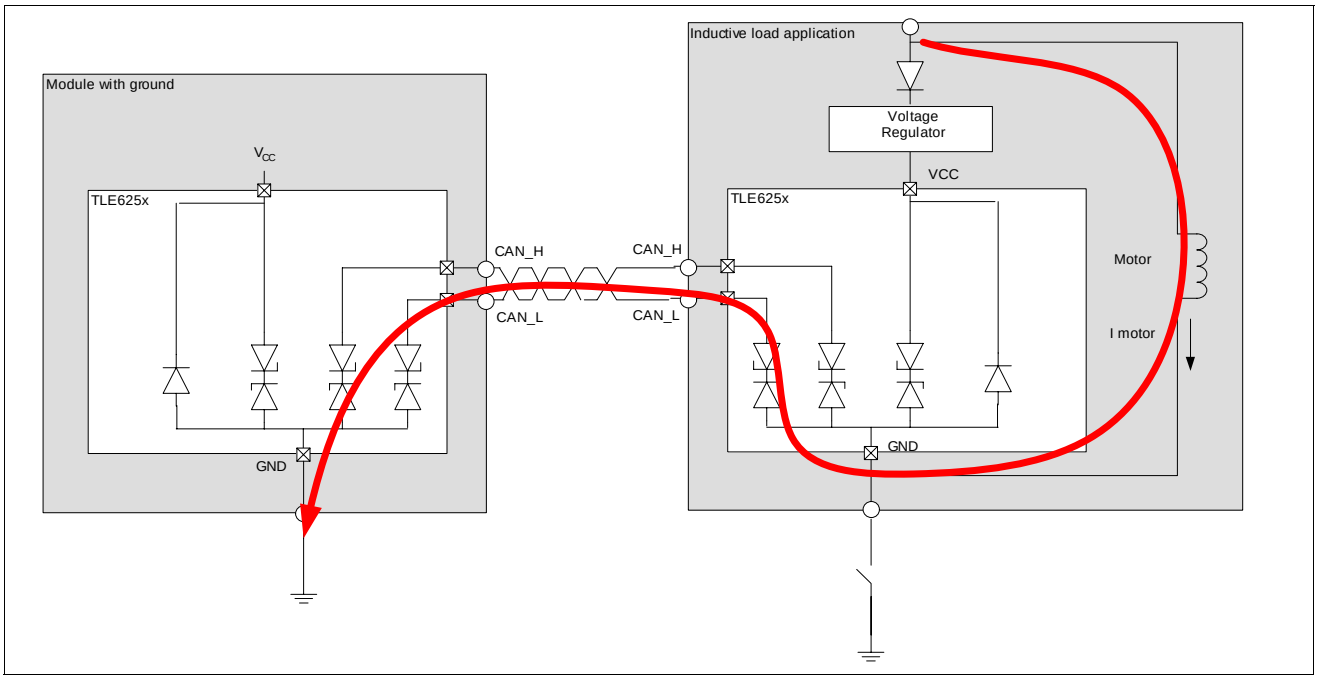


Figure 13 Loss of ground with inductive load

If the application is using an inductive load, a risk of destruction is possible, if the inductive load has no freewheeling diode. **Figure 13** shows the issue. When the ground disconnects, the coil has to be demagnetized and the current is flowing in the less ohmic path available. One of the lowest ohmic path on the application is the CAN transceiver. The inductive load increases the voltage until turning on the ESD protection and the current is flowing. The ESD protection isn´t designed to withstand such a long energy and the transceiver is very quickly destroyed by E.O.S. (Electrical Over Stress). The only solution is to plan a free wheehling diode on the inductive load. No protection can be done at the transceiver level.

2.3.8 Loss of Battery.

In case of loss of battery, no issue can be expected, and the device behaves as in unsupplied state. Please refers to the **Chapter 3.1.1** (TLE6250G), **Chapter 3.2.1** (TLE6251DS) and **Chapter 3.3.1** (TLE6251G) for additional information on the behavior of the device, when unsupplied.

3 Power management, transceiver supply.

Each transceiver product has its own power management features, from the basic features of the TLE6250G to the complex power management of the TLE6251G. The following chapter will describe which power consumption on the different supplies pin will be achieved with the different devices.

3.1 TLE6250G.

The TLE6250G is the first High Speed Transceiver product Infineon has introduced the market. This part has no power management. Anyhow, the part includes an inhibit functionality, to switch the device completly. This device is perfectly matching application on the KL15 powernet, so unsupplied when the vehicle is parked.

3.1.1 TLE6250G in unsupplied mode.

When the TLE6250G is unsupplied, it brings on the bus an pull down resistors specified in the datasheet (parameter R_i)

3.1.2 TLE6250G in inhibit mode.

In inhibit mode, the power consumption on the Vcc, (specified in **[1]** $I_{CC, STB}$) is below 10µA. The complete device is disabled. The TLE6250G brings on the bus an pull down resistors specified in the datasheet (parameter R_i).

3.1.3 TLE6250G in normal mode.

In normal mode, the device needs a current on the Vcc of maximum 70mA in dominant state, and 10mA on recessive state **[1]**. To estimate the power consumption in normal mode, a cyclic ratio of 50% can be assumed, because we can consider the communication is overall 50% dominant, 50% recessive. In normal mode, the device will need a maximum average current of:

$I_{CC, AVG} = (I_{CC,REC} + I_{CC, DOM}) / 2 = 40mA.$

3.1.4 TLE6250G in fault condition.

3.1.4.1 Average maximum current in fault condition.

In presence of bus failure, the Vcc supply current for the transceiver can increase significantly, in case of CAN_H shorted to ground. (case 4, see **Figure 30**). It is recommended to dimension the Voltage regulator for the worst case, especially when the Vcc also supplies the micro controller. It is important to notice the Vcc supply current increase only in dominant state, the recessive current remains almost unchanged. With the same assumption as the **Chapter 3.1.3**, the average fault current will be:

$I_{CC, AVG, fault} = (I_{CC,REC} + I_{CANH, SC}) / 2 = 105,5mA$

This current is the maximum average current the device will demand on the Vcc supply line.

3.1.4.2 Peak maximum current and decoupling capacitor.

The peak current is higher than described in **Chapter 3.1.4.1**, and it is recommended to filter the maximum peak current by the decoupling capacitor's the Voltage regulator needs for stability reason. The worst case scenario is to have 17 dominant bits in a row. At the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RxD and thus forces an Error Frame due to the bit failure condition. The first bit of the error frame again is not reflected at RxD and forces the next error frame (Tx Error Counter + 8). Latest after 17bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the error passive limit and stops sending dominant bits. During this 17bits, the maximum current will be $I_{CANH, SC}$. To filter this peak current, we need first to compute the delta current the capacitor should deliver.

$\Delta I_{CC MAX, SC} = I_{CANH, SC} - I_{CC,REC} = 190mA.$

The worst case bypass capacitor then calculates to:

$C_{buff} = \Delta I_{CC, MAX, SC} \times t_{DOM, MAX} / \Delta V_{max}$

Figure 14 gives the result, function of the baud rate of the decoupling capacitor value, with an allowed ΔV_{max} of 200mV. This value is an excess value, since the voltage regulator will react. This reaction time is only dependant on the device used and so cannot be described here.

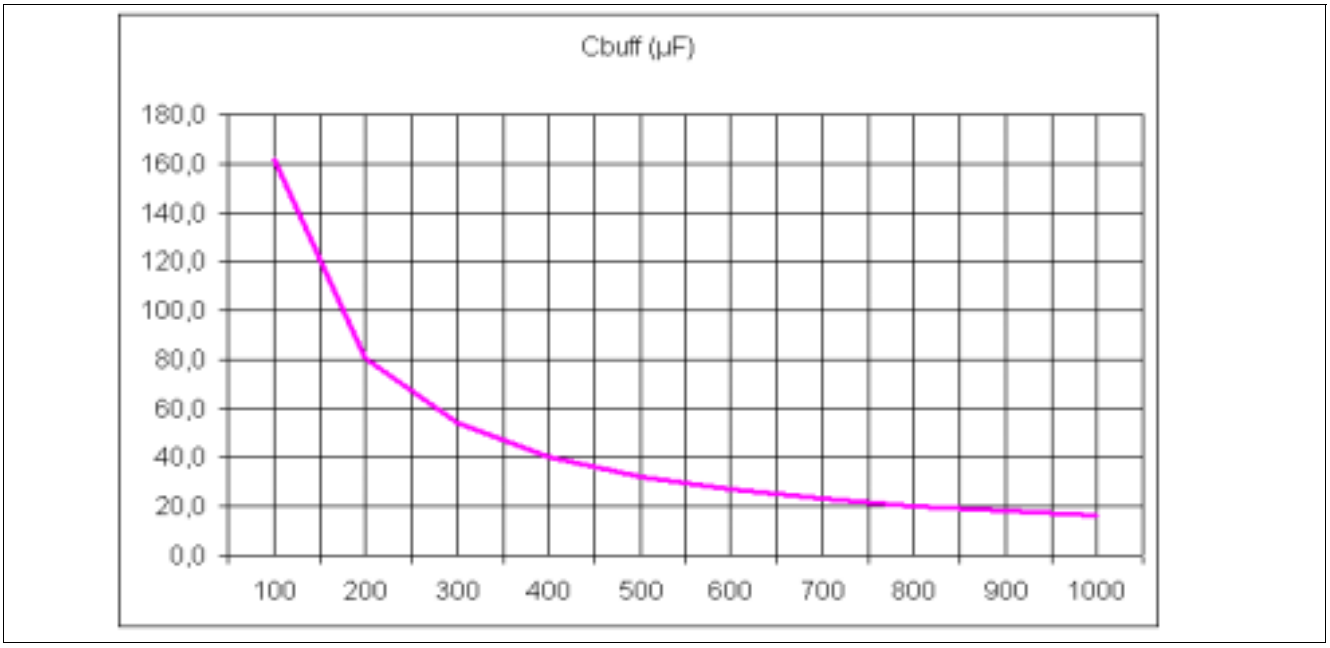


Figure 14 Buffer capacitor in function of the baud rate.

3.1.5 TLE6250G junction temperature.

In the **Chapter 3.1.3**, we have seen the worst case current consumption in normal condition, with a 5V supply. This leads to a nominal power dissipation of : 0,5 x (70mA x 3,5V + 10mA x 5V) = 150mW. The SO8 package offers an Rthja of 185K/W in the worst case. The junction temperature is then increased by 28K worst case. In case of short circuit, the power dissipation will increase of course. The transceiver might go to thermal shutdown. In that case, the receiver is still active, only the power stage is disabled, behavior is identical to receive only mode.

3.2 TLE6251DS.

TLE6251DS offers a standby mode. In this mode, the device is still able to receive some data, with the target to wake up a micro controller. This device is then compliant to Clamp 15 as well as Clamp 30 (see **Chapter 2.1**) powernets and thanks to the very high ohmic behavior in unsupplied mode (**Chapter 3.2.1**), perfectly suitable for the Clamp 15 part of a mixed KL15 / KL30 network.

3.2.1 TLE6251DS in unsupplied mode.

TLE6251DS has an improved behavior during unsupplied case. The R_i resistors of the receivers are cutted, and the current flowing into the pin CAN_H / CAN_L is limited. The datasheet **[2]** gives the value (paramater $I_{CANH, L, lk}$) to 5µA worst case. It leads to a equivalent resistor of 1MΩ minimum. Thanks to this, the device perfectly fits the request of the Clamp 15 mixed with Clamp 30. The pull down resistor will be limited, compared to the TLE6250G.

3.2.2 TLE6251DS in stand by mode.

In that mode, the TLE6251DS needs a maximum current supply $I_{CC, STB}$ of 30µA, 20µA typical [2]. Figure 15 shows how to compute the quiescent current of the application, (actuators excluded).

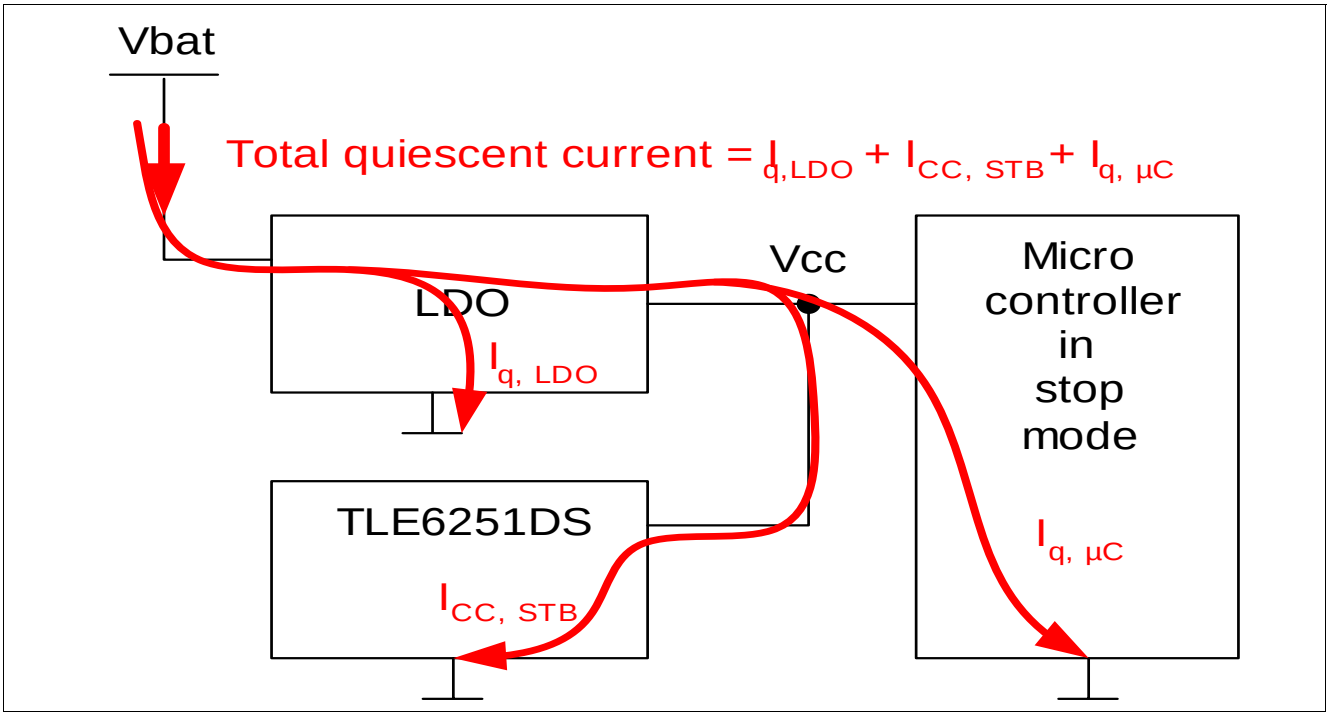


Figure 15 Quiescent current computation in stand by mode.

It is important to notice that in this quiescent current “grand total”, the biggest part is often the Voltage regulator contribution ($I_{q, LDO}$), if the Voltage regulator is designed in standard bipolar technology. (TLE42xx or TLE44xx Infineon products). To get rid of this issue, it is recommended to use the new Voltage regulator family from Infineon, in the SPT5 technology, (TLE72xx and TLE74xx). For example, the supply current of the TLE4275 is worst case 200µA [7] at 25°C when the TLE7270 is 30µA [8], for similar maximum output current and functions. With an SPT5 Voltage regulator and TLE6251DS, the leakage current the module will need in a parked car should be in the range of 70µA (depending on the micro controller stop mode supply current).

3.2.3 TLE6251DS in normal mode.

In normal mode, the TLE6251DS behaves as the TLE6250G. Please refers to Chapter 3.1.3

3.2.4 TLE6251DS in fault condition.

Please refer to Chapter 3.1.4.

3.2.5 TLE6251DS junction temperature.

Please refer to Chapter 3.1.5.

3.3 TLE6251G.

The TLE6251G has an enhanced energy management, allowing the device to control the entire supply chain of the electronic module, targeting to achieve the lowest quiescent current. It perfectly fits the Clamp 30 application. There’s no voltage supply sequencing. Vcc, VµC and Vs can be powered in indifferent orders.

3.3.1 TLE6251G in unsupplied mode.

Same remarks as for the TLE6251DS, see **Chapter 3.2.1**.

3.3.2 TLE6251G in sleep mode.

In sleep mode, the quiescent current of the device is 25µA typical, 35µA worst case on the Vs pin **[3]**. If the V_{cc} and $V_{\mu C}$ are OFF, using the INH functionality (see also **Chapter 4.3.8**), then the entire module will need no more current (actuators excluded).

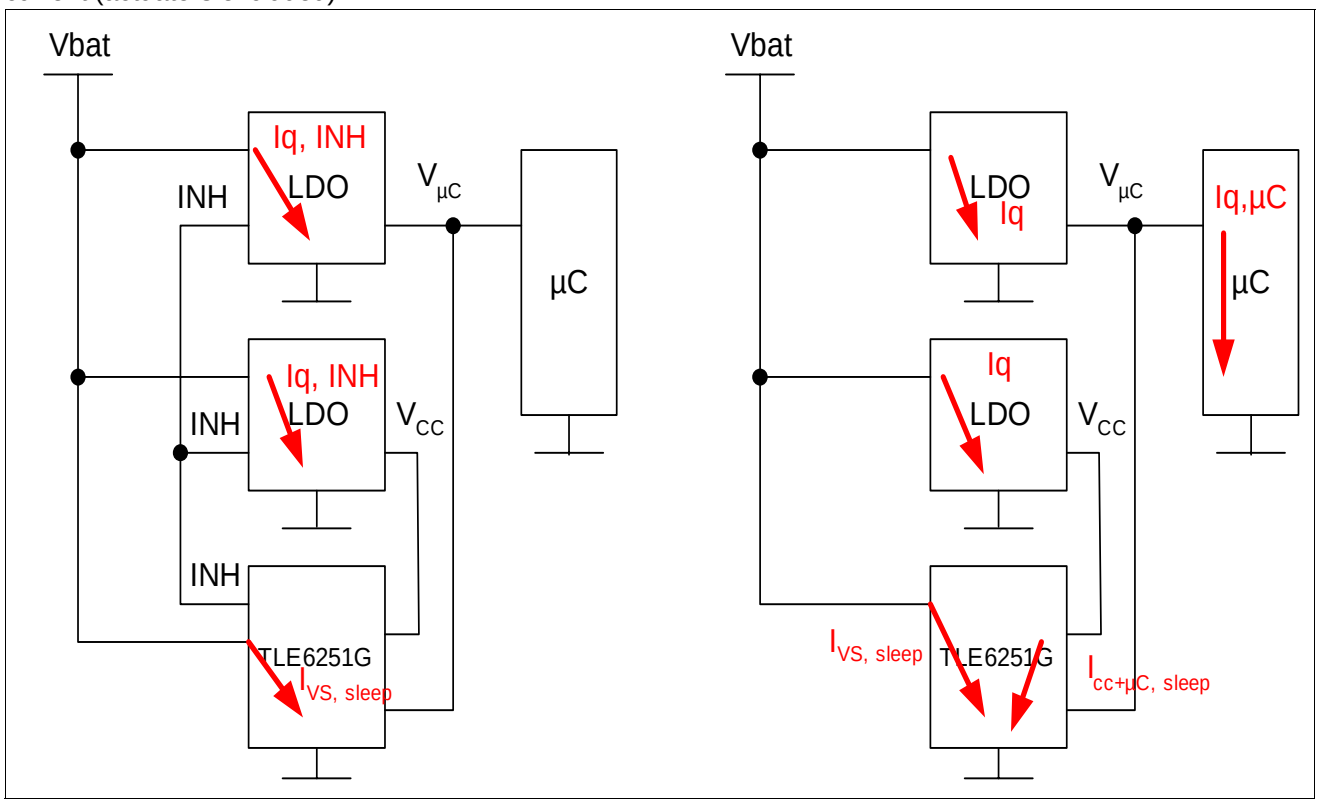


Figure 16 Quiescent current computation in sleep mode, with and without inhibit functionnality.

In case the V_{cc} and / or $V_{\mu C}$ are supplied, an extra leakage current has to be taken into account, and the overall quiescent current of the module will increase dramatically. **Figure 16** shows the two cases. The $I_{q, INH}$ values are given in the data sheet and are typically in the range of one µA.

3.3.3 TLE6251G in Stand by mode.

The stand-by mode is entered at power up or after under voltage as Vs. Compared to sleep mode, the TLE6251G turns ON the high side switch of the INH output so an extra leakage current has to be taken into account. 25µA maximum to turn ON and supply the high side internally **[3]**. It is also necessary to compute the extra current of the INH load which is connected to the INH output, which is application dependant.

The TLE6251G includes a under voltage detection on its three supply pins, Vs, Vcc and $V_{\mu C}$. In case the application requires to keep the device in standby mode for a long time (higher than the minimum under voltage blanking time, see also **Chapter 4.3.5.2**), then, both Vcc and $V_{\mu C}$ have to be present. Otherwise, the TLE6251G will go automatically to sleep mode. It means the quiescent current of an application with TLE6251G remaining in stand by mode is bigger than the sleep mode, since the voltage regulators must remains ON, even if no or few current are consumed.

3.3.4 TLE6251G in receive only mode.

In receive only mode, the device is functional and needs the same current as in normal mode, recessive state.

3.3.5 TLE6251G in normal mode.

In the normal mode, the TLE6251G behaves as the TLE6250G so please refers to **Chapter 3.1.3**, with the correct values given in the data sheet **[3]**.

3.3.6 TLE6251G in fault condition.

As for the TLE6250G and TLE6251DS, the current consumption on the V_{cc} pin will increase dramatically. Please refer to chapter **Chapter 3.1.4**. Since the bus error management is only valid after four transitions of bus (from recessive to dominant), the worst case scenario with 17 consecutive bits dominant has to be taken into account as well.

3.3.7 TLE6251G junction temperature.

In normal condition, the device needs 40mA on the 5V V_{cc} supply. The SO14 package offers a R_{THJA} of maximum 120K/W, leading to a junction temperature increase of 24K, compared to the ambient temperature.

3.3.8 Choice of the voltage regulator.

The voltage regulator has to be chosen in the family of the low drop output (LDO), as the Infineon's TLE42xx, TLE44xx, TLE72xx and TLE74xx. These LDOs families allow input voltage down to 5.5V at their input pin. To filter the bounces on the battery supply line, the application requires a big input capacitor. This capacitor has to be protected against reverse polarity by adding a diode. This diode has to be chosen with the lowest voltage drop (Schottky diode, typical 200mV) in its forward path. So to say that the LDO delivers a proper 5V with a minimum of 5.7V battery voltage. Below, the 5V cannot be warranted anymore, and the LDO follows the battery voltage. For the transceiver it means as well the level will be smaller, and follows the battery line, until a threshold when the communication will stop completly. It should be able to deliver 40mA DC current (see **Chapter 3.1.3**), only for the transceiver. The LDO should also allow to work with a peak current of 105mA (see **Chapter 3.1.4.1**) for the transceiver. Since the 105mA are not DC condition after a while, the Error Frame counter will stop the communication, it is not needed to warranty 105mA DC condition. The decoupling capacitor at the output of the LDO is described in **Chapter 3.1.4.2**. If the LDO is used only to supply the transceiver, the TLE4266-2G.**[9]**, offering a minimun of 150mA peak current, an INH input, in SOT223, fits perfectly.

4 Interface with micro controller.

A CAN transceiver is the physical layer between the protocol controller (micro controller, state machine), to the physical transmission medium. Following is a description, of TLE6250 and TLE6251 family, of the interface between the micro controller and the Infineon's used transceiver.

4.1 TLE6250G/GV33.

Figure 17 shows the pin out and a brief description of the logic pins of the TLE6250G and TLE6250GV33, adapted to 3.3V logic level. Following is a description of the logical pin and **Figure 21** and **Figure 22** gives the standard schematic of the application.

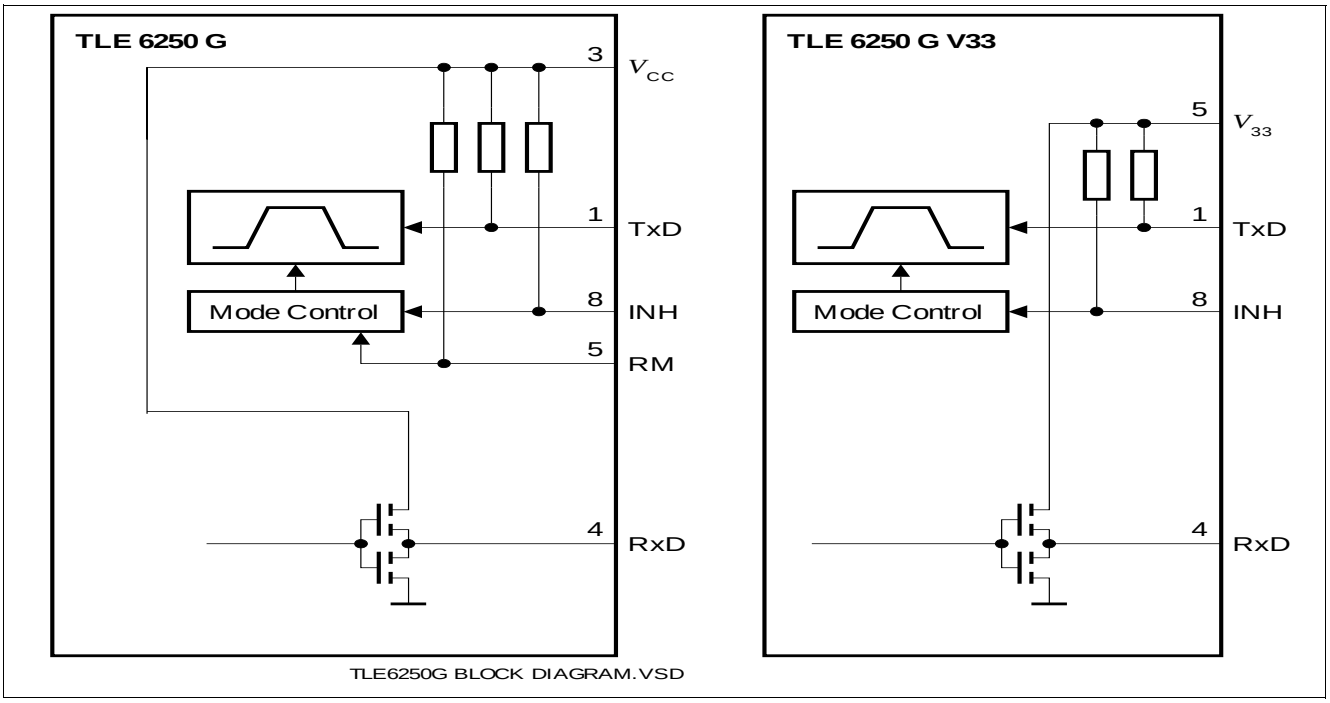


Figure 17 Block diagram of TLE6250G/ TLE6250GV33

4.1.1 Pin V_{cc}

The pin V_{cc} gives the proper 5V supply to build the CAN_H and CAN_L signal, as well as the receiver supply and internal voltage reference supply to build the recessive state level. In case of TLE6250G use, the logic pins are pulled up to Vcc. **Chapter 3.3.8** gives additional information about how to size correctly the voltage regulator supply.

4.1.2 Pin RM (only for the TLE6250G version).

The pin RM or Receive only Mode is a special feature from the TLE6250G. This pin allows to inhibit the data streaming on the TxD pin, which blocks the transmission. Main functionality of the receive only mode is to allow diagnostic (to avoid the aknowledge bit realized by software), to check modules connections, see **Figure 18**, or to avoid miss-communication on the medium due to a micro controller failure. To enter the Receive-only Mode, a logical zero has to be applied on the pin. To set the device in normal operation, so to activate the data streaming from the micro controller on the TxD pin, the RM pin has to be set to a logical 1. Since the TLE6250G integrates a pull up resistor, by default the device is in normal operation. In case the Receive only mode is not used, the pin can to be left opened.

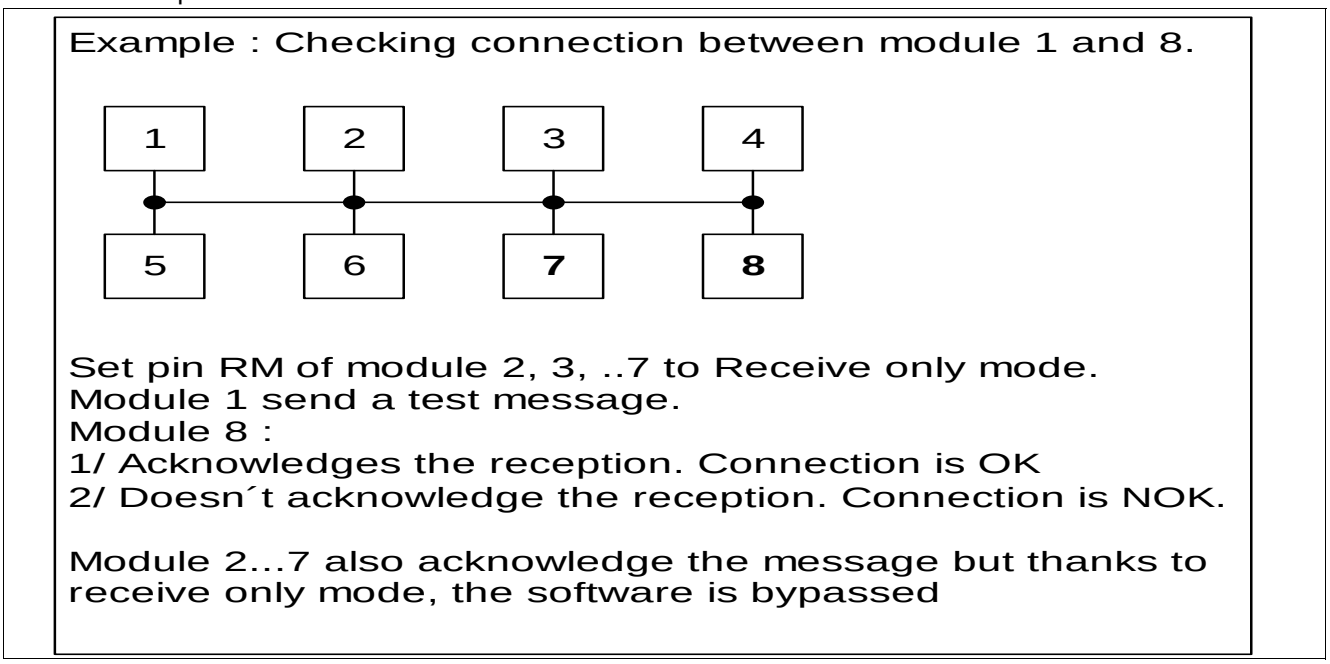


Figure 18 Module connection verification, using receive only mode functionnality

4.1.3 Pin INH.

The pin INH is used to set the device in stand by mode or normal operation. The stand by mode is used to reach the lowest quiescent current possible on the Vcc pin. To enter the stand by operation mode, the pin has to be at a logical 1. As the device integrates an internal pull up, by default, the device is in stand by mode.

To enter the normal operation, a logical 0 has to be applied. In that case, the maximum current flowing out the INH pin is 525µA. In case the INH mode is not needed, the pin has to be set to ground directly.

4.1.4 Pin V_{33} or V_{io} (only for TLE6250GV33).

The pin V_{33} or V_{io} is needed for operation with 3.3V I/O micro controllers to get the correct level between the micro controller and transceiver. This pin needs some current, mainly to supply the RxD pin (see **Chapter 4.1.6**). This pin can also be supplied by a 5V voltage regulator of course, when the application is requesting a separate supply for the micro controller and the transceiver. In case the V_{io} voltage is 0V, the TxD pin is 0V as well and the risk is to have a permanent dominant signal on the bus. The TLE6250GV33 includes the functionnality to not react to the TxD pin if V_{io} is 0V. In that case, the CAN_H and CAN_L output switches are OFF and the device is recessive. In the opposite case, if V_{cc} is OFF, and V_{io} is ON, the RxD might be permanently low (dominant), and could trouble the software. To avoid this, in case V_{cc} = 0V, the RxD pin is permanently high (recessive).

4.1.5 Pin TxD.

The transceiver receives the digital bit stream to be transmitted from micro controller onto the bus via the pin TxD. Sometimes, the signal at TxD show steep edges at bit transitions, likely to degrade the EMC performance of the total module. In this case it is recommended to place or to plan a serial 1kΩ resistor into the TxD line between the transceiver and the micro controller. Along with the TLE6250G internal capacitance (value) this would help to smooth the edges to some degree. For high speed communication up to 1Mbit/s, the resistor might generates on extra delay and this has to be taken into account, please refers to **Figure 19**. The parasitic capacitor C_{TxD} is not specified, for testing reasons. The standard value used for the Infineon's transceiver is 10pF, 15pF to consider the worst case.

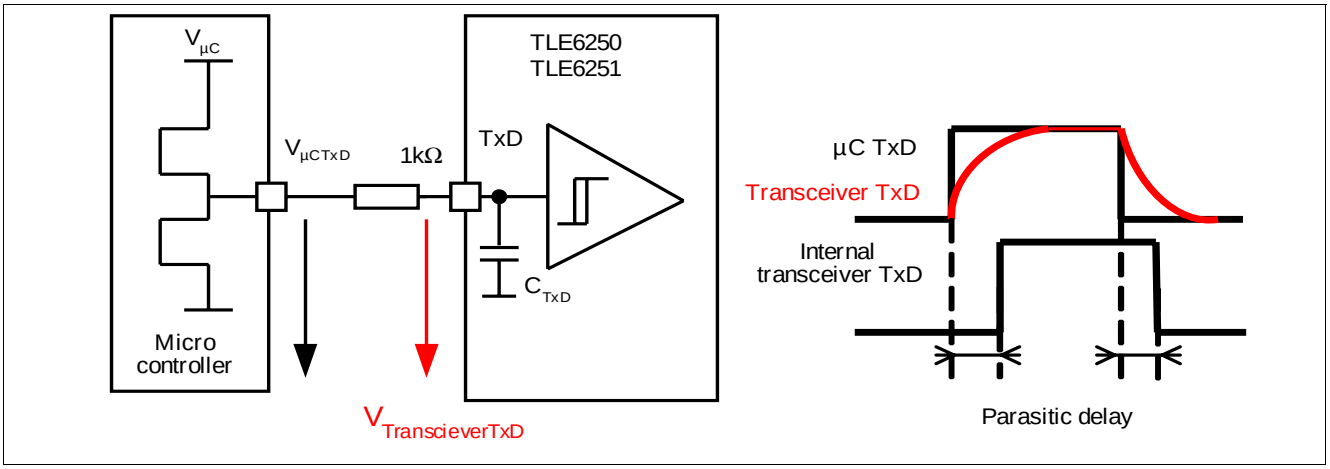


Figure 19 parasitic delay in case of serial resistor.

4.1.6 Pin RxD.

The analog bit stream received from the bus is output at pin RXD for further processing within the micro controller. As with pin TXD a series resistor of about 1kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1Mbit/s are used. The output stage of the RxD pin is a push pull stage. The output is not protected against over-current. Nevertheless, in case the RxD pin is in short circuit, a current of about 15mA typical can flow in or out (depends on short to ground or short to Vcc). This typical failure happens when the pin is forced to ground or 5V. The pin RxD follows the bus, meaning it also repeats what the TxD pin sends. The **Figure 20** shows the propagation delay concept.

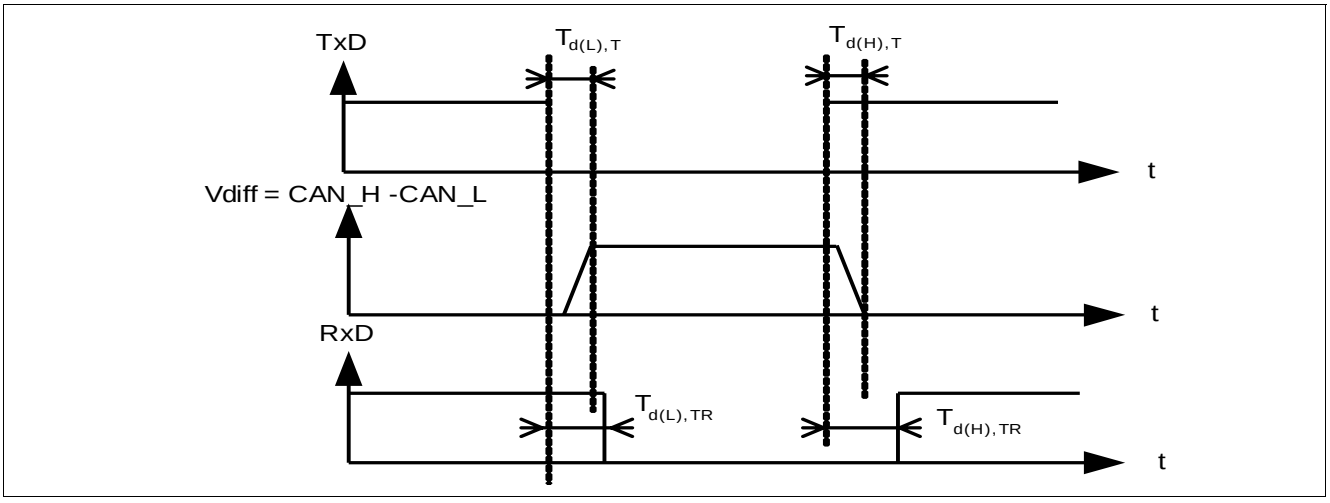


Figure 20 receiver timing

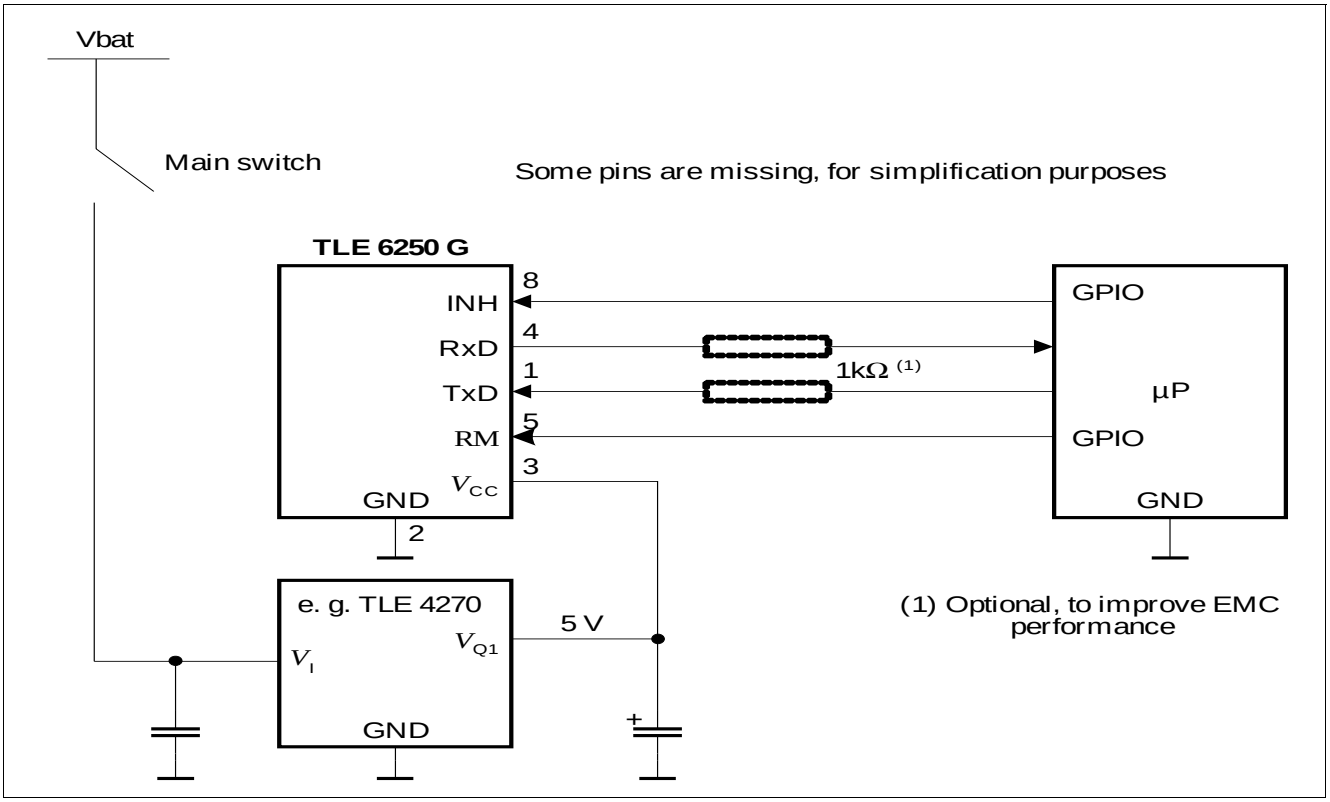


Figure 21 Typical application for TLE6250G

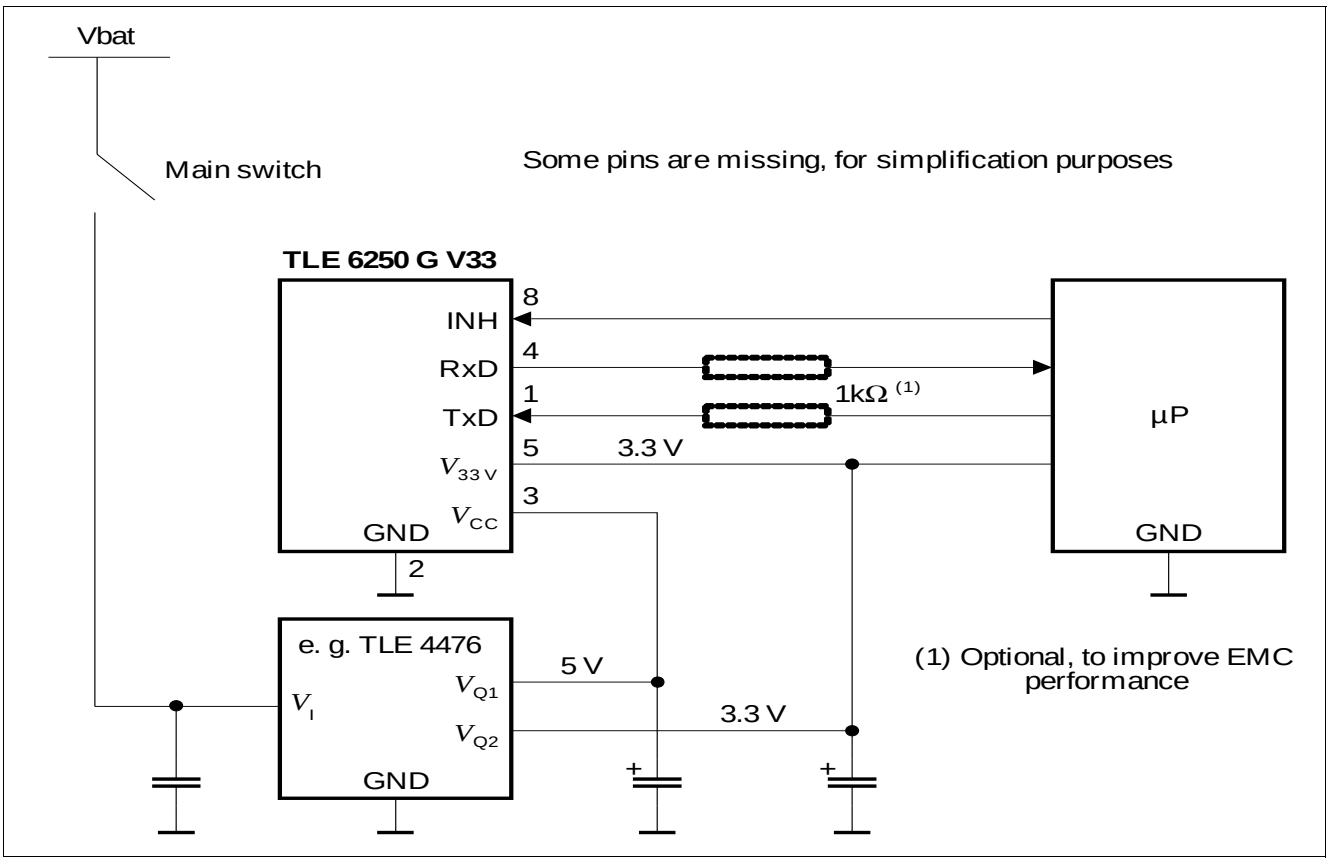


Figure 22 Typical application for TLE6250GV33.

4.2 TLE6251DS.

Compared to the TLE6250G, TLE6251DS has almost the same pin out (see **Figure 23**). The TLE6251DS is able to wake up the micro controller on bus activities. We will now describe the logic pins of the TLE6251DS. **Figure 27** describes the typical application interface between TLE6251DS and micro controller. TLE6251DS fits only to 5V micro controller interface.

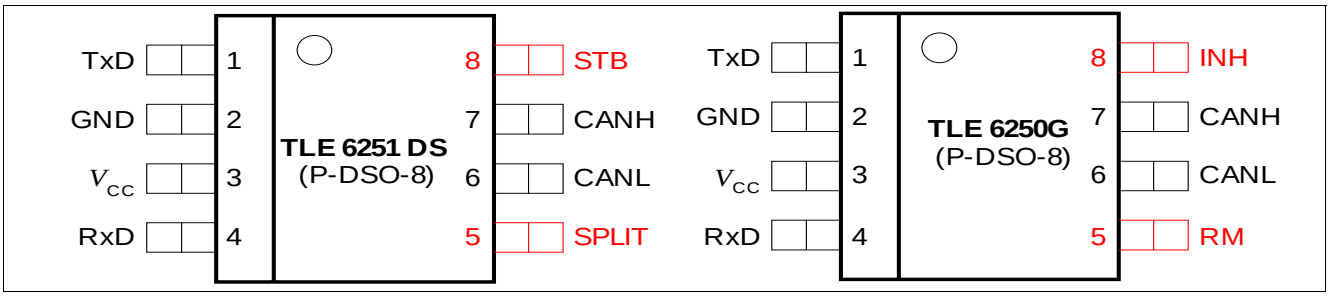


Figure 23 Pin out comparison TLE6251DS and TLE6250G

4.2.1 Pin STB.

The STB pin (STand By) is used to set the TLE6251DS in the standby or normal mode. To set the device to normal operation, a logical 0 has to be applied. (and logical 1 to set the device to standby mode). As the pin has an integrated pull-up, by default the device is in standby mode. In case the standby feature isn't needed, the pin should be connected to ground.

4.2.2 Pin TxD.

4.2.2.1 Hardware description.

Please refers to the **Chapter 4.1.5**, description of the TxD of the TLE6250G.

4.2.2.2 Time out function.

The TLE6251DS has a permanent dominant disable time. **Figure 4.2.3** describes this feature. It´s used in case the micro controller goes to faulty condition and sets the TxD pin to a permanent 0 logic level. In that case, the bus is permanently dominant and the entire network is down due to the faulty micro controller. To avoid this, the permanent dominant disable time will automatically relax the bus to recessive level if the TxD pin is low for more than t_{TxD}. The value can be found in the TLE6251DS data sheet **[2]**. To come back to normal operation, the TxD pin has to go back to a logical 1. No special filter timing for the recovery is applied. It means there's no constrained on the minimum time TxD pin has to be at logical 1 to leave the permanent dominant disable function. Anyway, the function is realized with a flip flop so the reset pulse should be longer than the propagation delay in the flip flop cell, so 20ns.

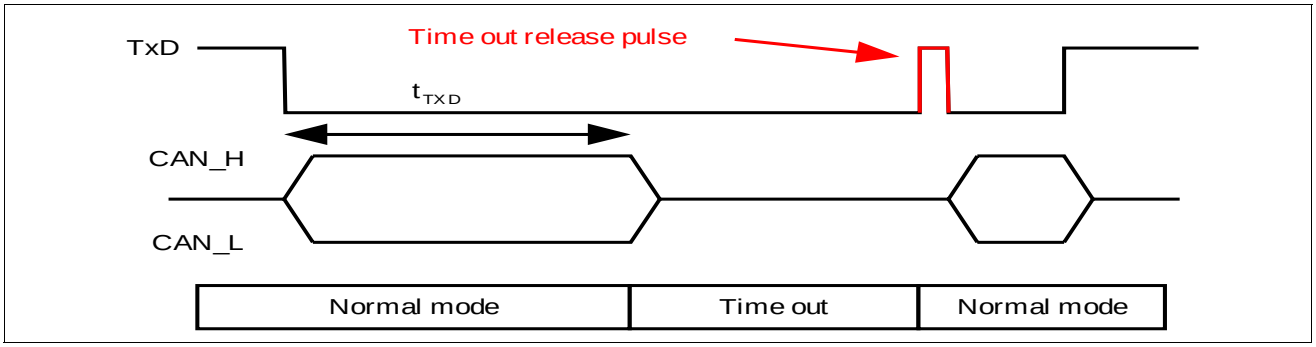


Figure 24 Permanent dominant time out feature.

4.2.2.3 Time out function. Baud rate limitation.

This feature limits the minimum possible baud rate. According to the CAN protocol a maximum of eleven successive dominant bits is allowed on TXD only (worst case of five successive dominant bits followed immediately by an error frame). With a minimum value given in the data sheet for TxD of 300µs **[2]**, so to say that 11 bits should be faster than 300µs, the baud rate of the application must be higher than 36.6kbit/s to be sure to comply to the CAN protocol. Min baud rate = max dominant bits / t_{TXD}.

4.2.3 Pin RxD.

4.2.3.1 Hardware description.

The RxD pin is as for the TLE6250G, see **Chapter 4.1.6**, a push pull stage. In case of short circuit to ground or V_{cc}, the current is limited to maximum 20mA (see datasheet **[2]** I_{scRxD}).

4.2.3.2 Wake up behavior.

The RxD pin is used to wake the micro controller up. To realize the wake up mechanism, the micro controller should be in stop mode and the RxD pin should be an interrupt input in order to wake. **Figure 25** gives the timing of the wake function. The parameter t_{WU} is given in the data sheet of the TLE6251DS **[2]** and is directly copied from the ISO 11898-5 norm**[6]**. It has to be understood as:

1. In case the pulse on the bus is shorter than the minimum value of t_{WU}, the device will/has to never wake up. This is to avoid parasitic wakes up due to Electro Magnetic disturbances for example.
2. In case the pulse on the bus is in between the minimum value and the maximum value, the device might wake up, depending on the temperature, production spread, etc....
3. In case the pulse on the bus is longer than the maximum value of t_{WU}, the device will/has to wake up.
4. Since the application micro controller might missed the first edge, the TLE6251DS is following the bus toggling.

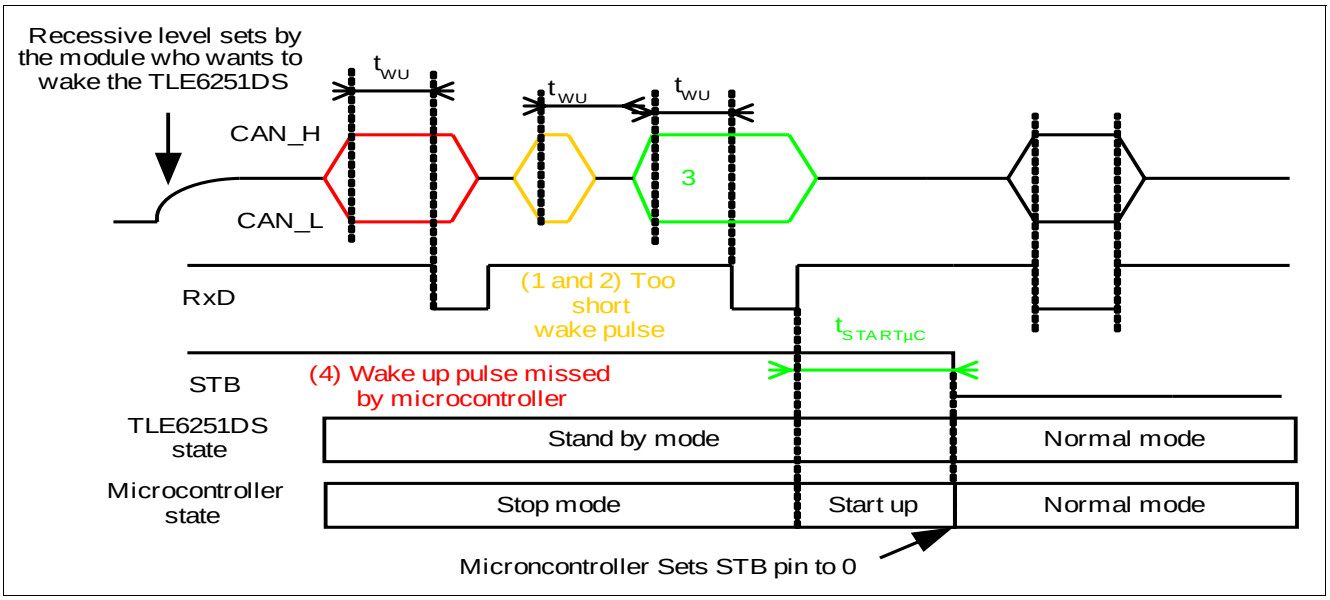


Figure 25 Wake up timing.

4.2.3.3 Delay from stand by to normal mode.

To achieve a very good quiescent current in standby mode, the TLE6251DS has two receivers, a low power mode and a normal mode. When the micro controller set the device to normal operation with the STB pin, and the bus is dominant, a parasitic pulse on the RxD pin is observed. This is due to the commutation from the low power receiver to the normal receiver. **Figure 26** describes the timing of this possible parasitic pulse. Unless this parasitic pulse maximum duration isn´t specified, it is never longer than 50µs.

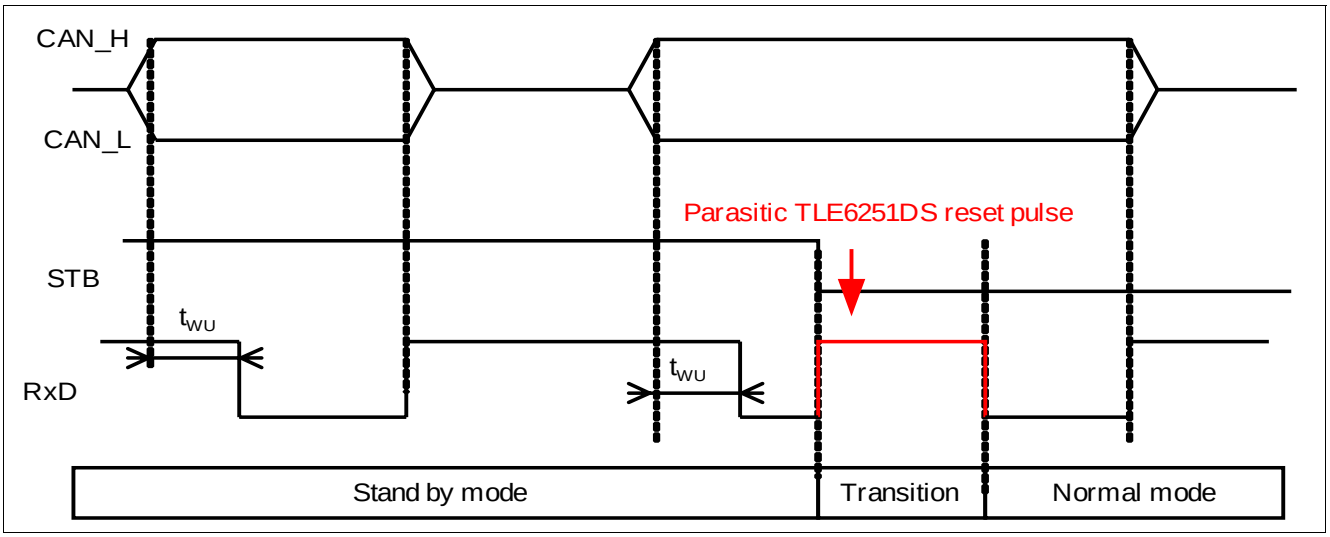


Figure 26 Delay from stand by to normal mode timing.

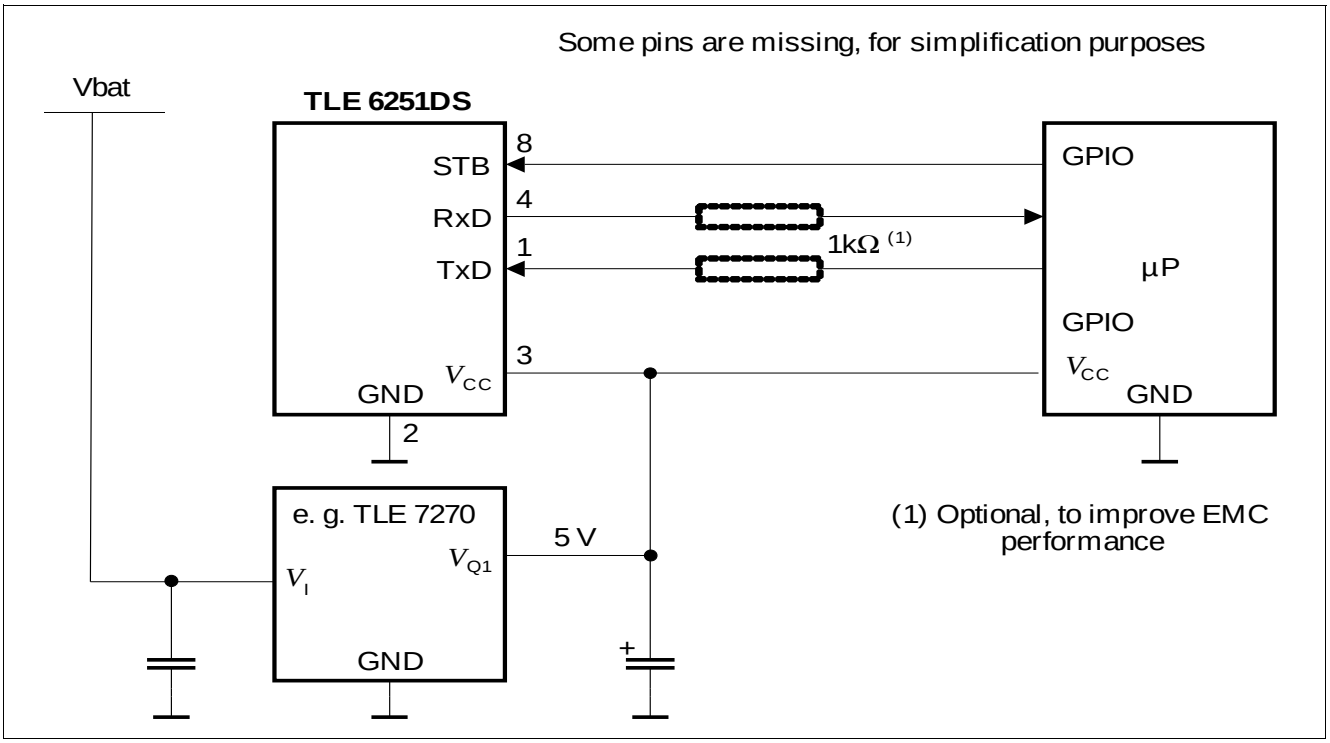


Figure 27 Typical application for the TLE6251DS.

4.3 TLE6251G.

TLE6251G has the same pin-out compared to TLE6251DS (see **Figure 28**), with inverse logic for the STB pin, and with additional functionalities. The TLE6251G is able to wake a micro controller, as well as the power supplies on bus activities. We will now describe the logic pins of the TLE6251G. **Figure 34** describes the typical application interface between TLE6251G and the micro controller.

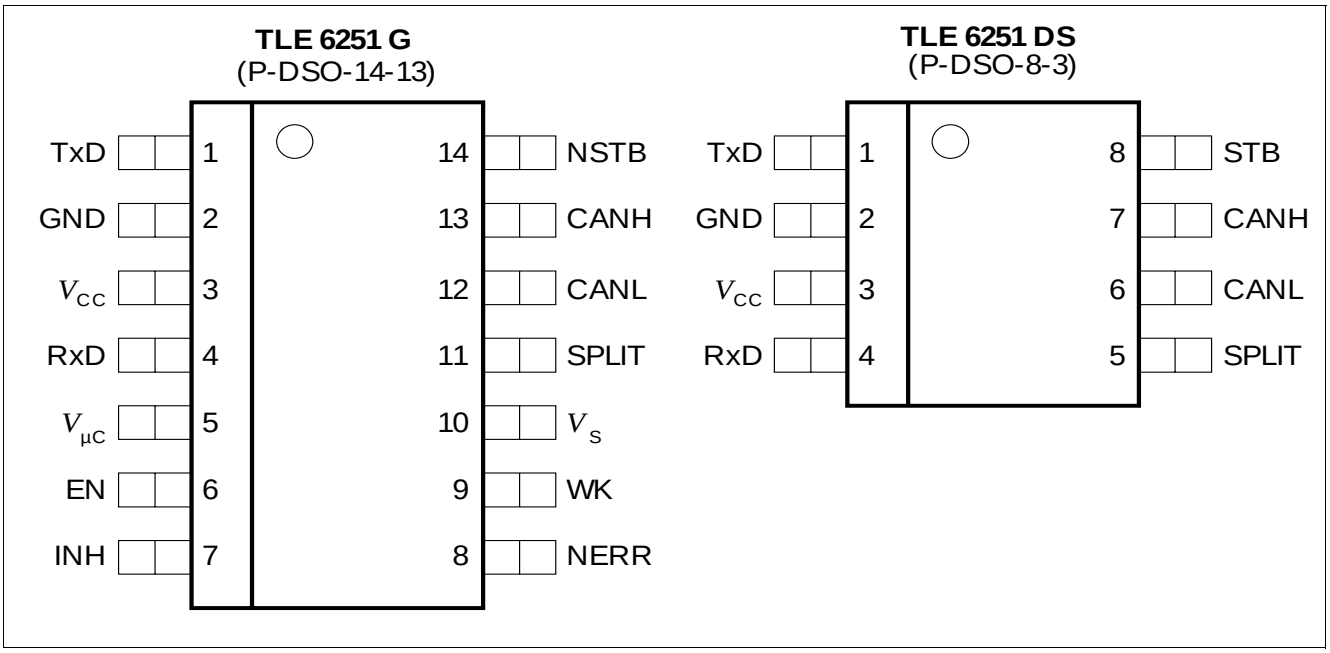


Figure 28 Pin out comparison TLE6251DS and TLE6251G

4.3.1 Pin TxD.

Please refer to **Chapter 4.2.2**

4.3.2 Pin RxD.

Please refer to **Chapter 4.2.3**, TLE6251DS without the wake behavior.

4.3.3 Pin EN.

The EN pin (enable) is used to set the TLE6251G to normal operation. The device is disabled with a logical 0, and enabled with a logical 1. The EN pin has a pull down integrated. By default, the device is disabled.

4.3.4 Pin NSTB.

The NSTB pin is used to switch the device to receive only mode (See **Chapter 4.1.2**) and also used to bring the device to sleep mode via the go-to-sleep state. **Figure 29** shows the different operating mode of the TLE6251G can be. The NSTB pin has an integrated pull down. By default, the device is in stand-by mode.

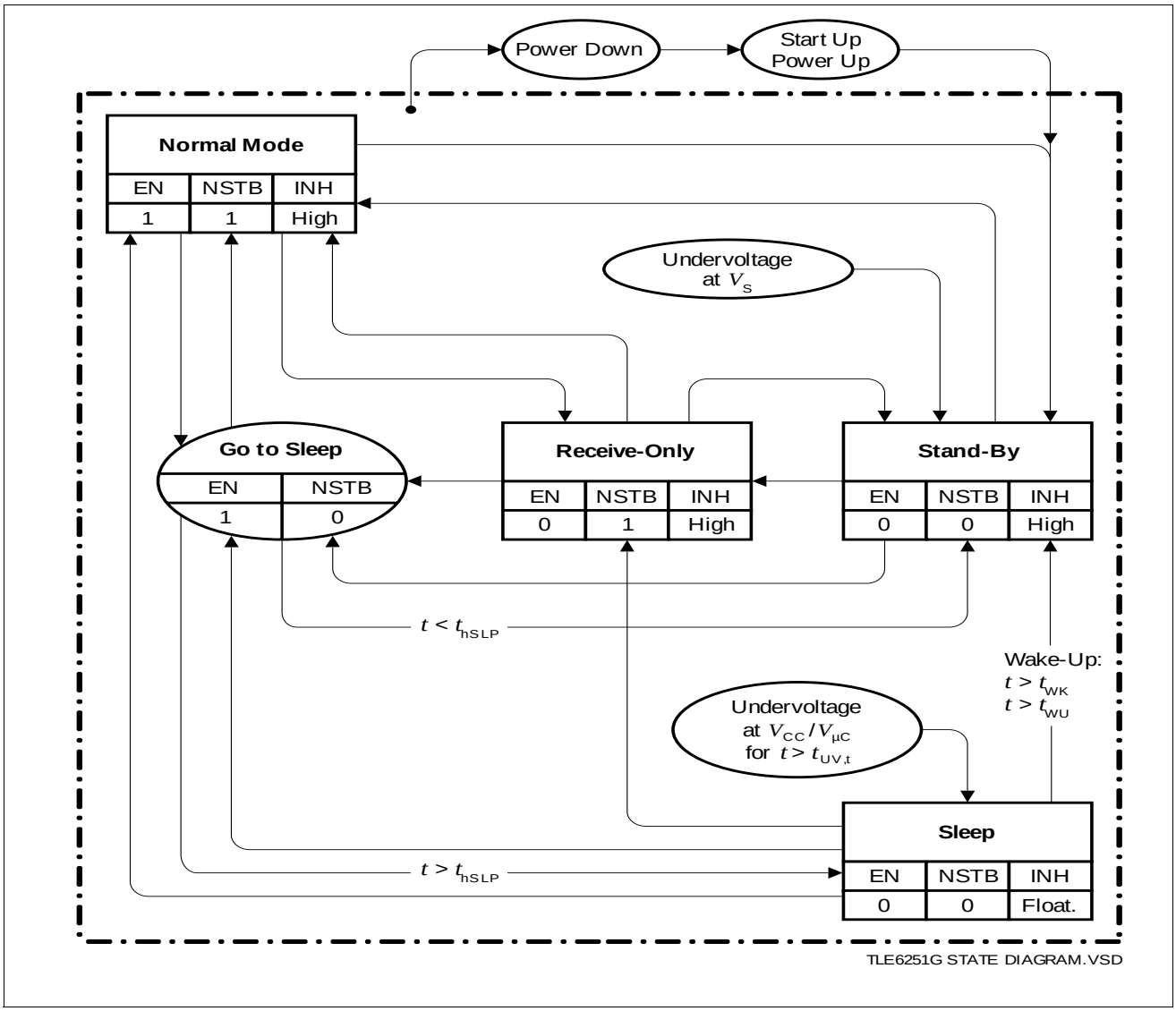


Figure 29 TLE6251G Mode state diagram

4.3.5 Pin $V_{\mu C}$.

The $V_{\mu C}$ pin is used to supply the pins in direct contact with the micro controller, to get the voltage reference of the micro controller threshold, in order to use the device both with 3.3V and 5V micro controller. In case the micro controller has the same supply as the CAN transceiver, the $V_{\mu C}$ and V_{cc} should be connected together.

4.3.5.1 $V_{\mu C}$ pin´s maximum current.

The push-pull for the RxD, as well as the NERR pin are supplied by $V_{\mu C}$. In case the RxD pin and/or the NERR are in short circuit to ground, a non-negligible current (please refers to TLE6251G data sheet [3], I_{SC_NERR}, I_{SC_RxD}) will be demanded to the micro controller supply.

4.3.5.2 $V_{\mu c}$ under voltage detection.

The $V_{\mu C}$ voltage level is monitored by the TLE6251G. Benefit of this solution is to avoid any undesired communication on the bus when V_{cc} is present but the micro controller is down. In case of under voltage detection on pin $V_{\mu C}$, the device is going to sleep mode. Since the device can command the micro controller supply, with the

INH output pin, a quite long filter time is implemented (refer to TLE6251G data sheet), to allow the micro controller supply to rise the voltage. There's no sequencing requested with the others voltage supply (V_{cc} and Vs).

4.3.6 pin V_{cc}.

The V_{cc} pin is used to supply the IC to get the proper CAN signal on the bus, the voltage reference and receiver stage when the IC is in normal mode. The V_{cc} voltage is monitored as the $V_{\mu C}$ pin. Please refer also to **Chapter 4.3.5.2**. There's no sequencing requested with the others voltage supply ($V_{\mu C}$ and Vs).

4.3.7 Pin NERR.

The NERR pin is used as flag indicator of a failure event on the bus. The output stage is a push-pull, connected to $V_{\mu C}$. The following section will describe the NERR behavior.

4.3.7.1 Possible bus errors cases.

Figure 30 gives the all possible failures that can be encount by the bus wiring. In case one or several of these failures occur, the pin NERR is set to a logical 0. It's important to notice that some errors can only be detected after certain amount of transition recessive to dominant states. For example, a CAN_L shorted to ground (case 5) failure cannot be detected as long as the bus is dominant. While some events can be detected by the protocol (cases 1, 2, 3, 4, 7), some others are only detectable by this transceiver feature (5 and 6)

4.3.7.2 Pin NERR in short circuit.

In case the NERR pin is shorted to ground, as the output stage is a push-pull, a high current can flow out. This current is internally limited. Please refer to TLE6251G's data sheet **[3]** parameter I_{SC_NERR}. This current has to be taken into account when dimensioning the $V_{\mu c}$ supply for a safe design. (see **Chapter 4.3.5.1**)

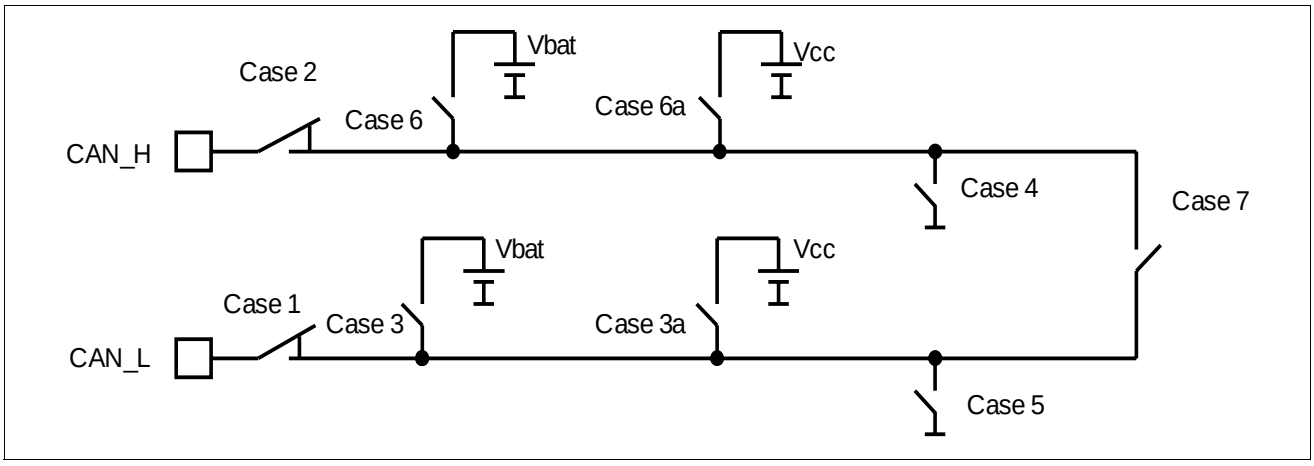


Figure 30 Possible failure cases failures on the bus word list. (According ISO 11898)

4.3.8 Pin INH.

The INH pin is not a real logical pin. The function of this pin is mainly digital and described in the following section. This pin is not a power output. It is a P channel DMOS switch to gives a "high voltage logic" indication.

4.3.8.1 Pin INH purpose.

Main purpose of the INH pin is to indicate a wake event from either the WK pin or the CAN line. The INH pin is always high, meaning equal to the battery voltage, minus a voltage drop (please refer to TLE6251G data sheet **[3]**) except during sleep mode condition. In that case, the pin is high ohmic.

4.3.8.2 Pin INH power capability.

The pin is not suitable to drive a low ohmic load, and the output current should not exceed 5mA. It is then impossible to drive the input of a voltage regulator (LDO) directly but should be used to drive the inhibit input of the LDO. The INH input isn't protected against short circuit to ground and so should not be connected outside the E.C.U. In the case of a short to ground, or overload, the protection will be the thermal shutdown.

4.3.8.3 Pin INH driving the INH input of an Voltage regulator.

All Infineon LDO family are active when their INH input is high and OFF when the INH input is low. Since they all have an integrated pull down, it´s normally not necessary to add an external one. Anyway, for EMC issue, it´s reasonable to plan an external resistor with a value of 10kΩ, in case of parasitics coming into the INH pin. **Figure 31** shows the recommended circuitry for the pin INH.

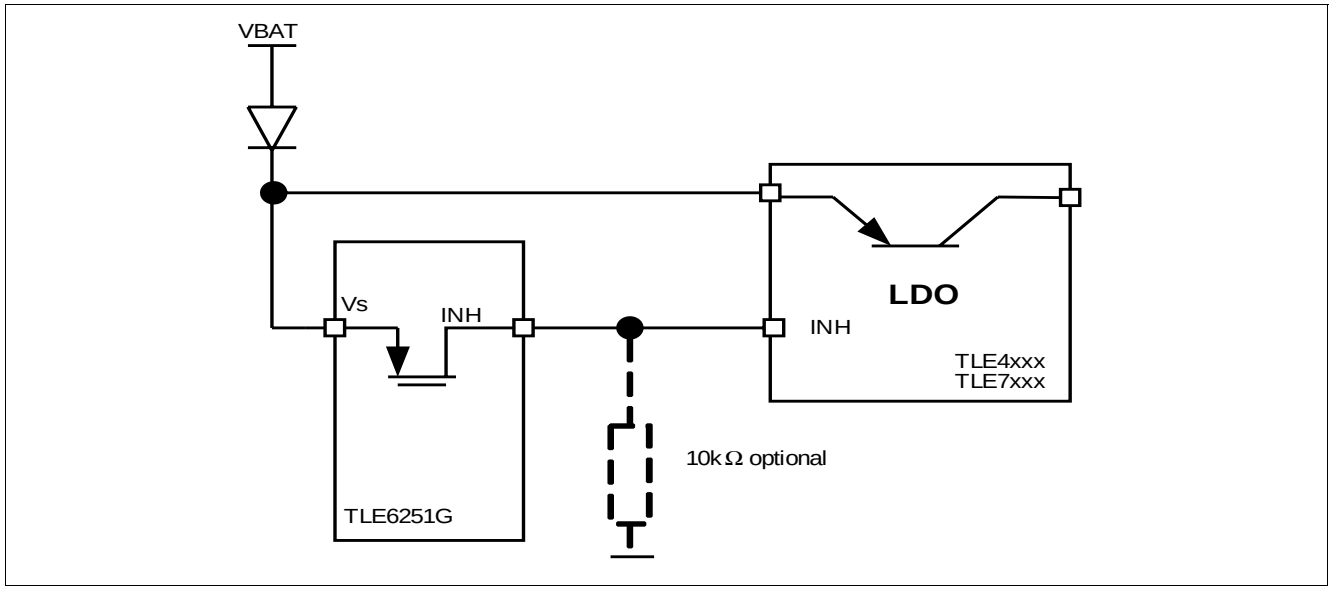


Figure 31 Circuitry for the INH output

4.3.8.4 Wake up timing with pin INH.

Using the INH pin to drive the voltage regulator INH, the wake up timing is shown on **Figure 33**. Please note the time scale isn't linear. The start up of a voltage regulator takes several ms when the logical signal are in ns. In some applications, only the inhibit input of the micro-controller voltage regulator, or the voltage regulator for the CAN transceiver is driven by theTLE6251G. The Vcc line necessary for proper supply of the transceiver, or the VµC for proper supply of the micro-controller is switched on by the micro-controller. If we assume a 2ms activation time for each LDO (see **Equation (4)**), and the necessary start-up time of the microcontroller, the time to go to normal operation increased significantly, like 10 to 40ms normally. Whenever this time is below 50ms (see **[3]**, parameter $t_{UV,t}$), the undervoltage mechanism is inhibited. It gives the time to react without entering into the sleep mode again, which will inhibit the microcontroller LDO and so entering infinite cyclic wakes.

Start up time of an Voltage regulator formula:

$$T_{max} = C_{max} \times V_{cc} / (I_{min} - I\ start\_up) \quad (4)$$

T_{max} represents the longest time needed to reach the regulated voltage (5 or 3.3V)

C_{max} is the total capacitance on the regulated voltage. (With capacitance tolerance)

V_{cc} is the regulated voltage (5 or 3.3V)

I_{min} is the minimum current the voltage regulator is able to drive as maximum.

I_{start_up} is the current the application (e.g micro controller) need during start up phase.

Example, with the TLE4278G.

The TLE4278G is a 5V Voltage regulator. Data sheet **[4]** specifies a minimum value for the maximum current the Voltage regulator is able to drive of I_{min} = 200mA. Assuming :

C_{MAX} = 60µF (20% tolerance on a 47µF capacitor) decoupling capacitors on the V_{cc},

I_{start_up} = 20mA to supply the application (microcontroller, logical circuitries...) the maximum time the Voltage regulator needs to reach 5V, starting from 0V is then:

Tmax = 60 x10^{-6} x 5 / (200 10^{-3} - 20 10^{-3})= 1,7ms.

4.3.9 pin WK.

The WK pin (Wake) is also a high voltage pin. It is used mainly to signal a local wake up event on the transceiver. A signal change is only necessary to wake up the device. There´s no pull-up or pull-down, so it can be used to wake via a switch to ground, or via a switch to battery. The wake up pin is sensible to voltage edges. In case the Wake pin is unused, it is recommended to connect the pin directly to ground. (to avoid parasitic wake up). See **Figure 32** for possible usage description.

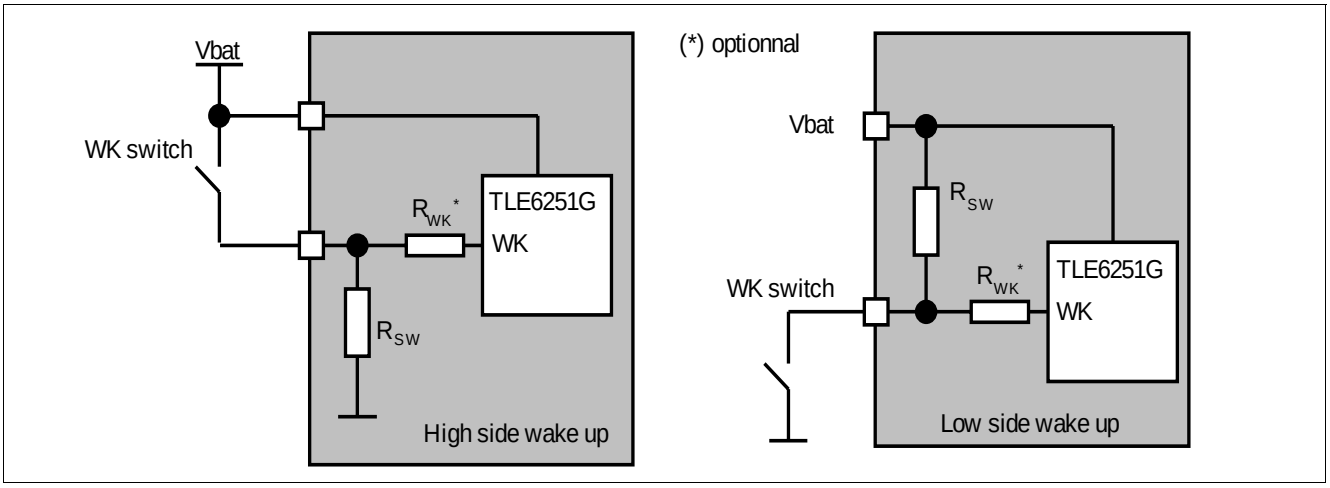


Figure 32 Possible wake up circuitries.

R_{WK} should be planned, to improve the robustness to ISO pulses. If the ISO pulses test shows good results without, R_{WK} is useless, because the absolute maximum rating (see **[3]**) allows enough safety margin. R_{SW} is necessary, to polarize the WK pin to the sleeping state. The value of R_{SW} should be set according to the cleaning current of the switch.

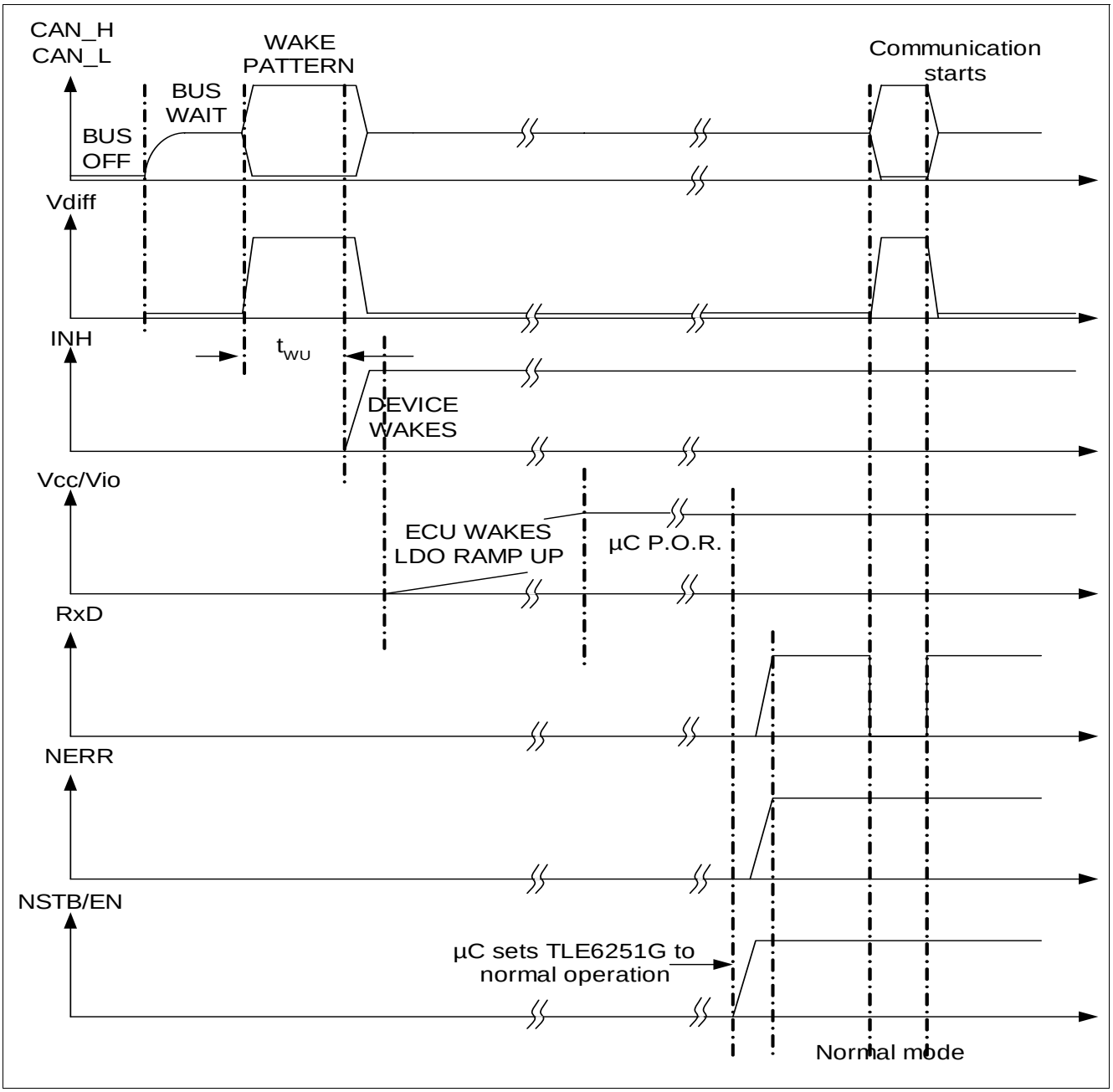


Figure 33 Wake up timing with INH function. Cold start.

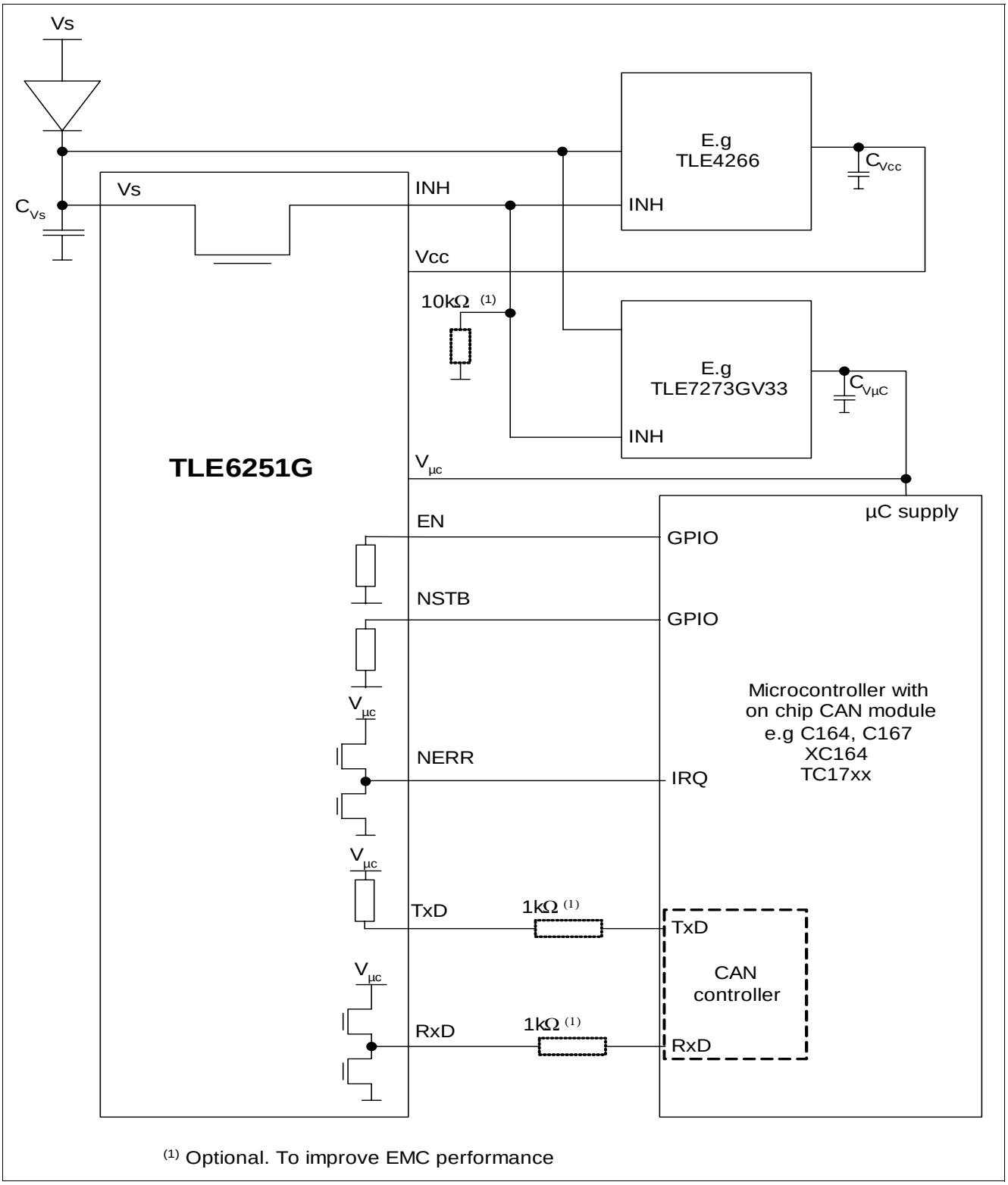


Figure 34 Typical application circuit for TLE6251G, with separate 3.3V VµC and 5V Vcc supply

4.3.10 Software issues consideration for TLE6251G.

4.3.10.1 Cold start.

The power ON flag of the TLE6251G indicates to the microcontroller whether a microcontroller cold start was caused by a wakeup from Sleep mode or by a first battery power application. This information is often needed for the application to initiate some possible calibration procedures upon first battery power application.

The pin NERR reflects the power ON flag when entering the power ON /Receive only mode from stand by, sleep or go to sleep mode. Moreover, in case of wake up from Sleep Mode, the TLE6251G provides information on the wake up source. Entering the Normal mode the pin NERR reflects the wake up source flag. A logical 0 signal indicates a local wake up via the WK pin whereas a logical 1 indicates a remote wakeup via the bus.

In case battery power is applied the first time, an internal hardware reset is given to the transceiver for initialization. Subsequently, the power ON flag is set and the pin INH is pulled to Vbat, activating the voltage regulator(s) and ramping up the V_{cc} supply. See also **Chapter 4.3.8**. Along with the V_{cc} the pins RxD and NERR go to logical 1. With ramping up V_{cc}, the micro controller comes up. As almost all micro controllers feature a weak pull down or floating behaviour at their port pins, the TLE6251G comes up in stand by mode after first battery power up. See also **Chapter 4.3.2** and **Chapter 4.3.7**. This is the starting point for the application program taking over the control now. If the microcontroller comes up with a logical 1 at its port pins, the TLE6251G enters the normal mode and the power ON flag information is irretrievably lost. Please refer to the **Figure 33** for timing characteristics.

Figure 35 suggests a software flow for an ECU cold start. It considers primarily the issues related to the TLE6251G rather than representing a complete software flow. After the transceiver and microcontroller have performed their initialization, the transceiver is put in power ON / Receive Only Mode for reading the power ON flag. If a logical 0 signal is read on the pin NERR, the ECU cold start was initiated by the first battery power up. The microcontroller performs the correspnding system startup procedure. If a logical 1 is read, the cold start was initiated by a wake up from sleep mode. In order to get information on the wake up source, the Normal mode is selected. If reading of the pin NERR yields a logical 0, there was a local wake up via the pin wake. If reading yields a logical 1 signal, the wake up came via the bus. Afterwards, the cold start procedure is finished and normal operation is ongoing.

4.3.10.2 Hot start.

A warm start up is performed when the ECU wakes up from Sleep Mode. **Figure 36** suggests a software flow for an ECU warm start. The starting point assumes a TLE6251G transceiver in its Sleep Mode and the host microcontroller in a dedicated power down mode. If the transceiver receives a wake up either via the pin WK, the internal wake up flag is set and signalled at the pin NERR and RxD. These signals can be used for wakeup of the microcontroller from its power down mode. The starting application program can now take control over the transceiver. If the power ON flag is of interest, the microcontroller can force the transceiver into Power ON / Receive Only Mode for reading the Power ON flag. Otherwise the microcontroller can force the transceiver directly into Normal mode for reading the wake up Source flag at the pin NERR.

As the microcontroller remains powered by the V_{cc} supply, the microcontroller can monitor its port pins for possible wake up events. Upon detection of a wake up event the microcontroller can initiate a wakeup by forcing the transceiver directly into normal mode. Then reading of the Power ON flag or wake up Source, flag is not necessary.

4.3.10.3 Enter the Standby mode.

When the network management decides to put the bus system into standby, each ECU must receive the appropriate standby command. The flow diagram seen in **Figure 37** shows the different steps in order to put the TLE6251G into Standby mode. Upon receiving a standby command (like a CAN message), the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus anymore, caused by other nodes, the bus must have been recessive for a suitable time before the TLE6251G is put in Standby Mode by setting NSTB and EN to logical 0. If there is no system dependant “waiting period”, implemented there would be the risk that a node sends out a last message while another one is already on the way towards

Standby mode. This would cause a wake up event thus making it impossible to enter a system wide low power state.

4.3.10.4 Enter the Sleep mode.

The procedure to put an ECU into sleep mode is shown in **Figure 38** it is similar to the previous one for entering the Standby mode. Upon receiving a sleep command the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus anymore, the bus must have been recessive for suitbale time before the TLE6251G is put into Sleep Mode by selecting NSTB to logical 0 and EN to logical 1. The difference now is that the microcontroller checks periodically for a wake up as long as Vcc is not yet down. This is necessary since it might happen that a wake up event just appears while the Go To Sleep Command is processed. In this case the INH of the TLE6251G will keep high and the Vcc will not drop down. Instead the wake up request is forwarded to the application via RxD and NERR. Without this check the microcontroller would assume that a sleep phase follows with disabled Vcc, thus waiting forever for a power ON reset caused by a wakeup which will never happen.

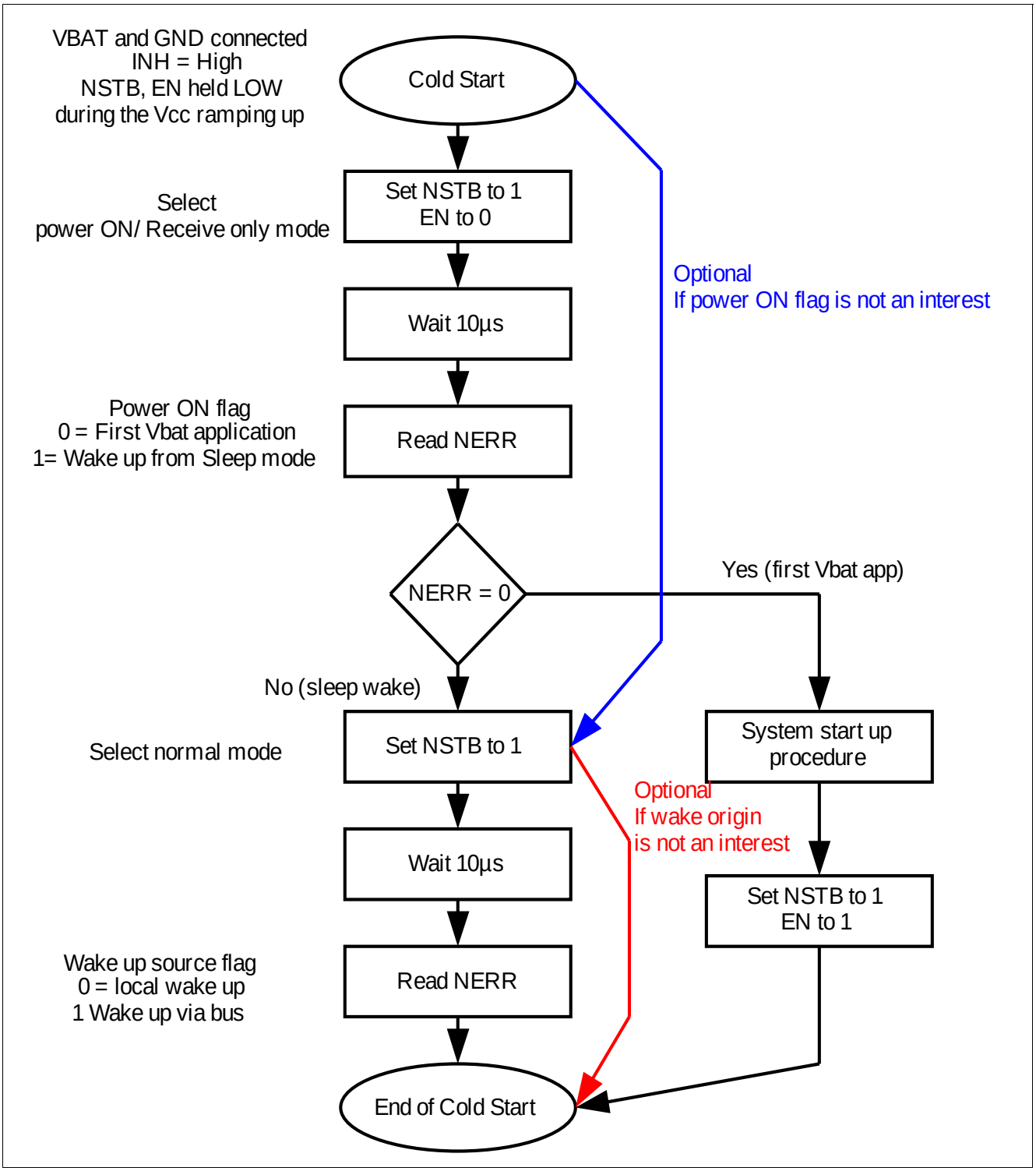


Figure 35 Flow diagram for an ECU cold start.

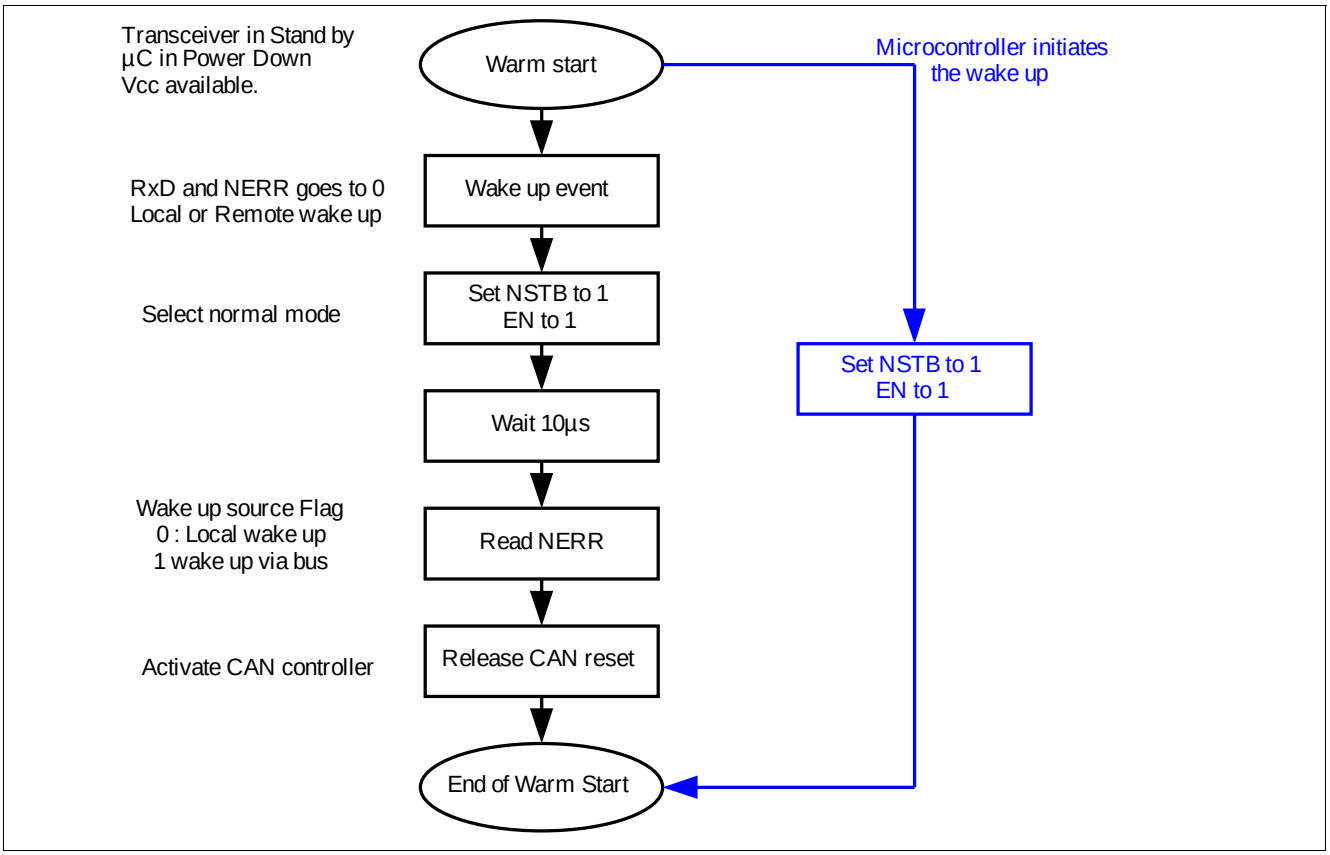


Figure 36 Flow diagram for an ECU warm start.

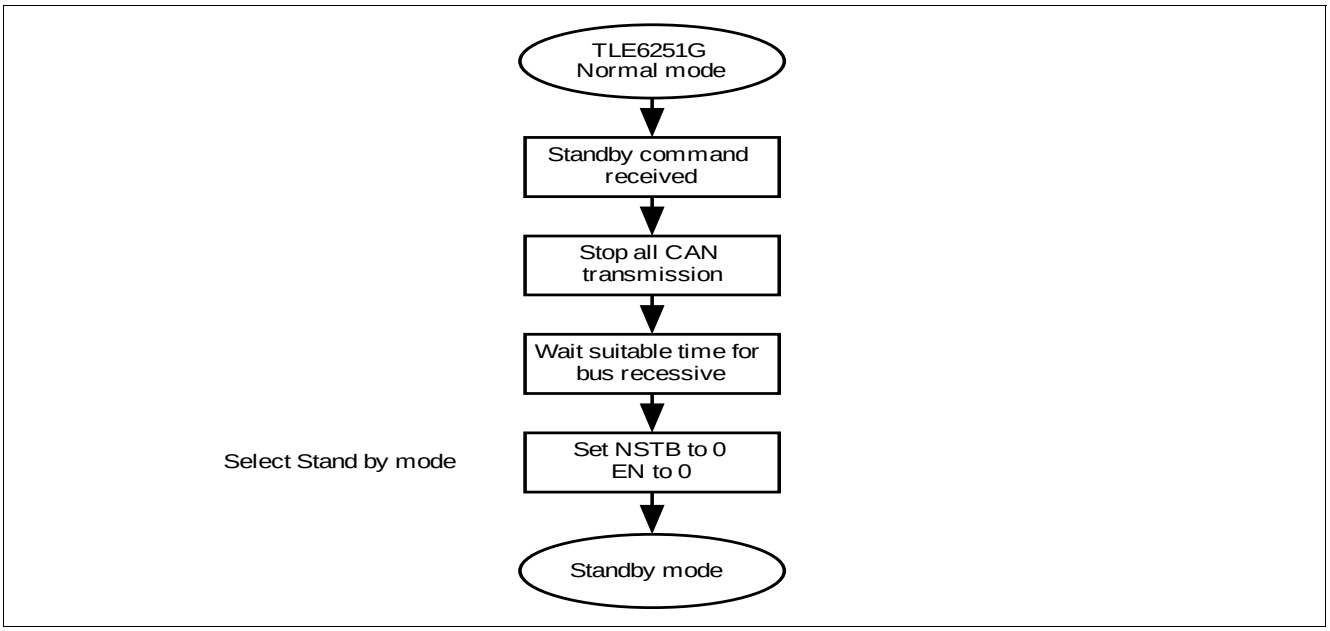


Figure 37 Flow diagram to enter Stand by mode

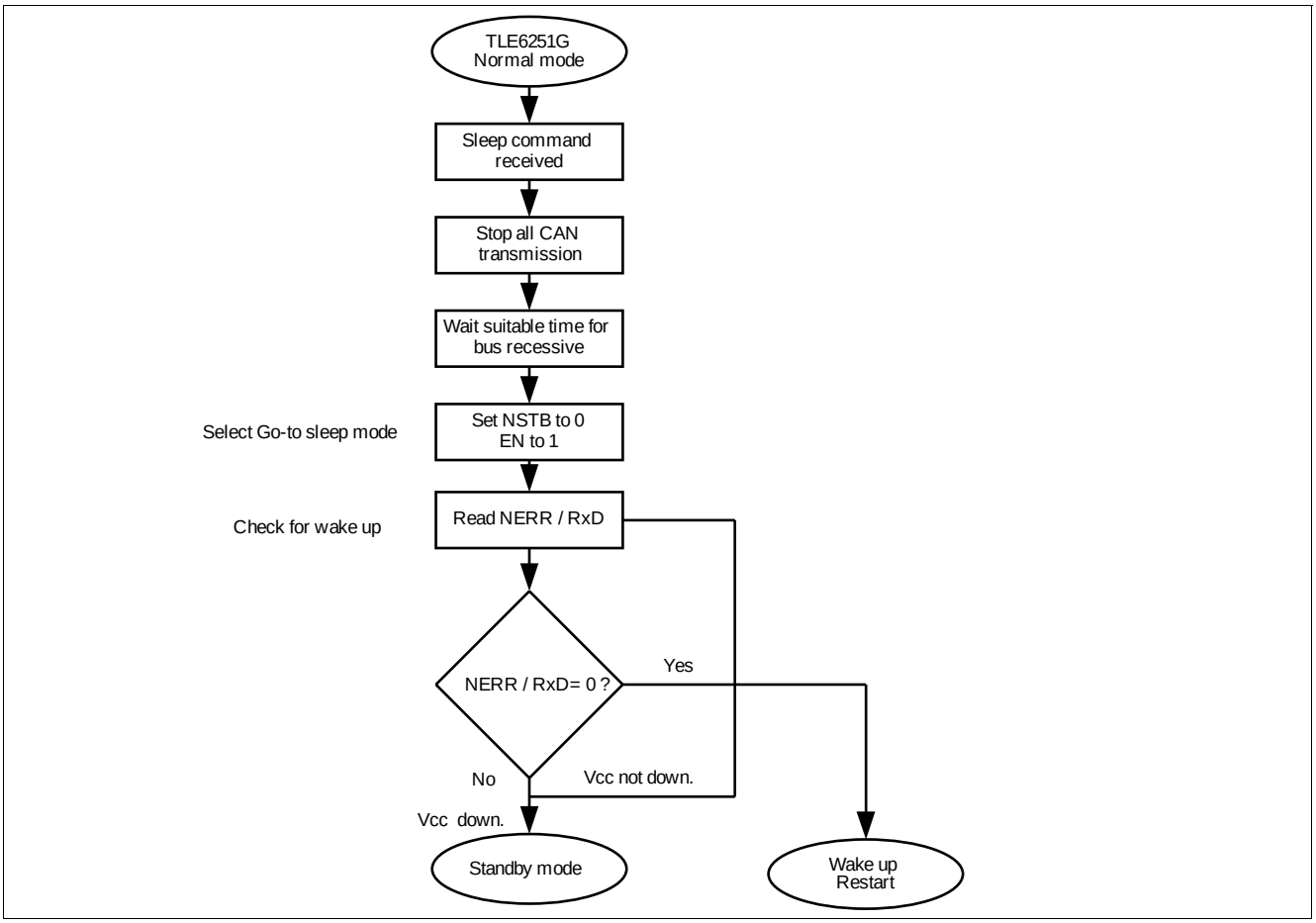


Figure 38 Flow diagram to enter Sleep mode

5 Bus pins. Terminations concepts.

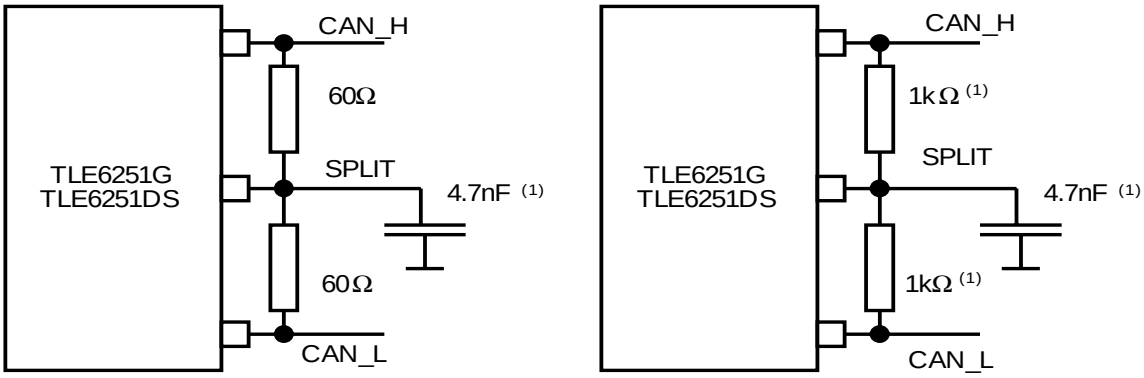
The transceiver is connected to the bus via the pin CAN_H and CAN_L. Some concept also includes a so called SPLIT pin. The purpose of this pin is to improve EMC behavior of transceiver, by increasing the symmetry between CAN_H and CAN_L. See **Figure 1**.

5.1 Termination resistors.

The ISO 11898-2 **[5]** and ISO 11898-5 **[6]** request for the system a 60Ω resistor bus termination. This bus termination resistor is needed to reduce the reflexions on the bus. Where and how to apply this 60Ω resistor is up to the OEM, several concepts are possible and used today, depending on the usage, the topology, etc... Some applications have only one termination resistor, mainly for stars topology. Some applications have two termination resistors of 120Ω, for linear topology, and some even have one termination resistor on each nodes, the total impedance should be equaled to 60Ω. However, it is recommended to put a weak termination resistor of 1kΩ at least for EMC improvements of the system, in terms of emission. It is important to not forget the short circuit issue, described in the **Chapter 2.3.4.1**.

5.2 Split pin.

The recommended application circuitry is described on **Figure 39**.



(1) Suggested value, has to be according to the car maker requirements.

Figure 39 Application circuitry for the split pin.

5.2.1 Recessive voltage in a mixed Clamp 15 / 30 network, without SPLIT.

When the system requires two types of modules, some connected to the CL15 (see **Chapter 2.1.1**), some connected to the CL30 (see **Chapter 2.1.2**), the unsupplied modules bring to the bus an extra impedance to ground. The result is the recessive voltage tends to go to 0V.

The recessive voltage with a mixed network, without split pin can be computed with the **Equation (5)**, with the usage of the TLE6250G.

$$V_{rec} = V_{ref} \times m / (m+n) \quad (5)$$

m represents the number of nodes supplied and enable (CL30)

n represents the number of unsupplied nodes. (CL15)

Vref is the recessive voltage when the device is alone. See **Table 1**. Typically V_{cc} / 2

The equivalent DC electrical schematic of the system is given on **Figure 40**, assuming (for simplification) all internal impedances and voltage regulators identical. **Figure 42** gives the voltage value, for m=2, function of n.

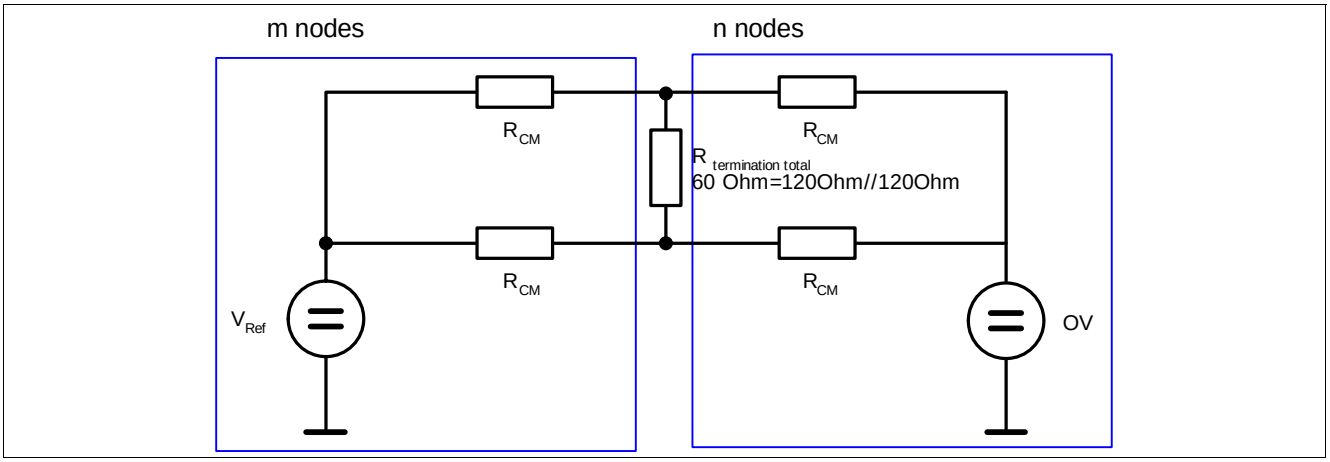


Figure 40 Equivalent electrical schematic for a mixed network without split pin

5.2.2 Recessive voltage in a mixed Clamp 15 / 30 network, with SPLIT.

TLE6251DS and TLE6251G integrate a SPLIT pin. The internal schematic of the split pin is quite complex, but can be simplified as a voltage regulator at V_{SPLIT} with an internal resistor R_{SPLIT}, **[2] [3]**. The purpose of the SPLIT pin is to improve the symetry of the signal, by maintaining the recessive voltage at mid value of the dominant voltage of CAN_H and CAN_L.

Using the SPLIT pin, the equivalent DC circuitry looks like **Figure 41**. The recessive voltage with a mixed network, with SPLIT pin can be computed with the **Equation (6)**, assuming all devices identical (for simplification purposes).

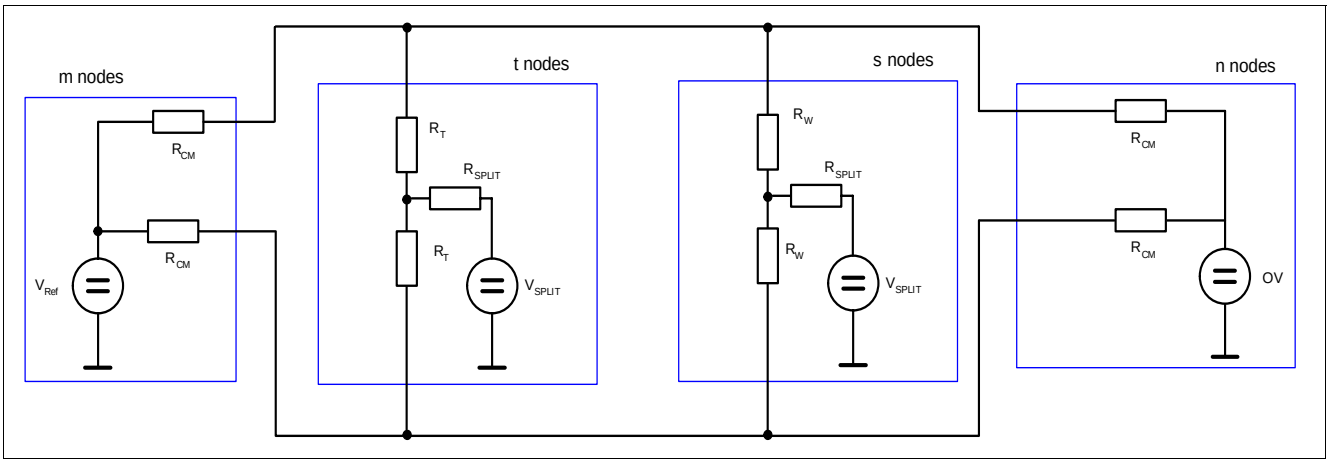


Figure 41 Equivalent electrical schematic for a mixed network with SPLIT pin

m represents the number of supplied and enabled nodes with and without split pin.(min 2)

t represents the number of SPLIT nodes with R_T = 60Ω termination resistors (min 0, max 2)

s represents the number of SPLIT nodes with R_W > 1kΩ weak termination resistors

n represents the number of unsupplied nodes.

(6)

$$Vrec = Vref \times \frac{1}{1 + \frac{n}{m + t \times \frac{Rc}{Rs + Rt} + s \times \frac{Rc}{Rw + Rs}}}$$

The influence of the SPLIT is seen, since Rc >> Rs, Rw or Rt.

Figure 42 gives the System recessive level, for several conditions. Worst case of two nodes in communications, others are disabled.

It is important to notice that both TLE6251DS and TLE6251G offer a very weak connection to gournd when they are unsupplied (specified in the datasheet **[2] [3]** as a current I_{CANHL_lk}) of about 1MΩ so to say the problem is less forseen for an application using these devices unsupplied.

Last but not least, a capacitor of about 4.7nF as shown on **Figure 39** but without connection to the SPLIT pin circuitry shows improve as well the recessive level value.

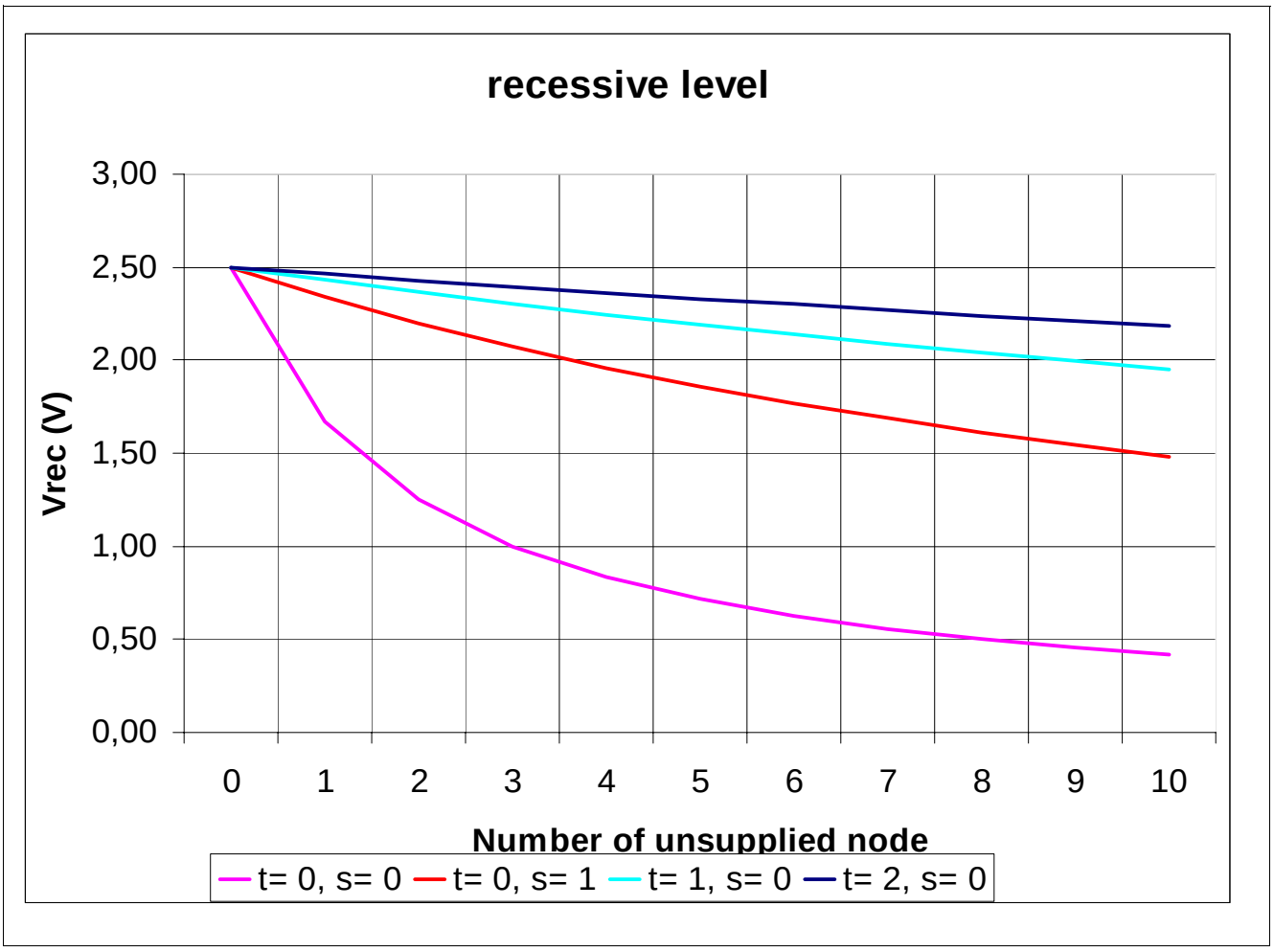


Figure 42 Recessive level for different configurations in a mixed network with split.

t=0, s=0 corresponds to the case without split termination concept. (**Equation (5)**)

t=0, s=1 correesponds to the case with a split pin at a weak termination resistor (1kΩ)

t=1, s=0 corresponds to the case with a split pin at the bus termination resistor (60Ω)

t=2, s=0 corresponds to the case with a split pin at both bus termination resistor.

5.3 CAN_H / CAN_L.

The CAN_H and CAN_L are the interface to the bus network. The challenge for these pins are multiples. EMC, ESD, that we will see in **Chapter 6** and **Chapter 7**. The challenge is also regarding short circuit discussed in the **Chapter 3.1.4** mainly. Last but not least, the CAN_H and CAN_L have parasitic capacitors to ground, due to the DMOS cells as well as the ESD structure. These parasitics capacitors are not specified, due to testing issues but the maximum observed value are in the range of 50pF for CAN_H, half of it for CAN_L for the TLE6250G. The reason for this unsymmetry is that CAN_L is a N channel, when the CAN_H is a P channel output stage. As a rule of thumb, the P channel cell is twice bigger to get the same Rdson.

6 ESD Aspects.

Among all the disturbances a CAN transceiver can encounter in a vehicle, the ESD discharge is one of the most critical. Since the basic application of networking is to be present in the whole vehicle, the risk of ESD discharge is very important. To get an impression of the issue, the **Figure 43** shows the current flowing into the TLE6250G, function of the ESD HBM discharge voltage; The ESD pulse is applied on the CAN_H pin, and the current is measured on the ground line. The device is unsupplied. ESD robustness is strongly dependant to the air humidity condition. ESD robustness is increasing with air humidity.

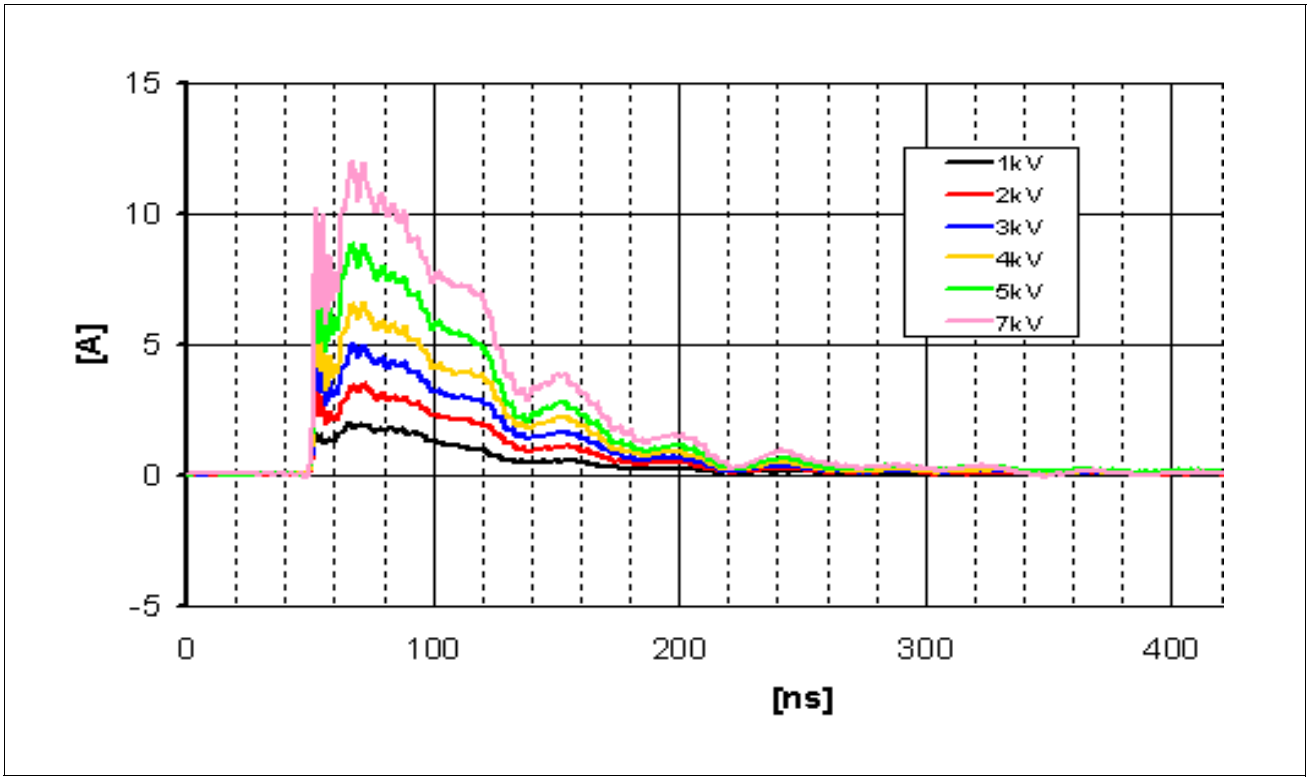


Figure 43 Current flowing in the TLE6250G ground, function of the ESD voltage. Device unsupplied

6.1 ESD tests definition.

6.1.1 Human Body Model test. (MIL-STD 883).

The HBM test is a modification of the Method 3015.7, MIL-STD-883. The test is realized on one pin, versus all the others. The semiconductor industry is keen to specify the ESD with HBM, because it represents the typical aggression during the processing of the module, of the operator in the facility touching the device. The model is equivalent to a capacitor of 100pF loaded to the ESD voltage. The discharge is applied via a 1.5kΩ resistor (1500Ω is your standard resistance value...). This test doesn´t represents the normal ESD aggression during the life of the vehicle or during the car manufacturing, because the risk of somebody touching the device when the module is built is very low. **Figure 45** shows the test protocol. Infineon realize the HBM test inhouse. The HBM values are specified in all Infineon's datasheet. The standard value is +/-2kV, but can reach higher values for the off board pins.

6.1.2 Gun test. (IEC 61000-4-2).

The IEC 61000-4-2 ESD test represents the typical case of somebody carrying a metallic object (screw drivers, pliers...),touching the connectors or the housing of the module. It´s also called gun or pistol test. It applies the same

voltage, as the HBM but loaded into 150pF and discharged via 330Ω. This test is more representative of the real ESD disturbance during the car manufacturing. The **Figure 44** shows the difference between the HBM and the gun test, for same voltage level. It´s obvious that the IEC61000-4-2 is a much more severe test in terms of energy. The test is realized on all the off board pins (CAN_H, CAN_L, Wake and Vs pin) versus ground. **Figure 45** shows the test protocol. For communication applications, as CAN and LIN physical layer, Infineon is performing the test in an external independant test facility (I.B.E.E. in Zwickau, Germany). The value isn't specified in the Infineon's datasheet, because the test is also application's dependant. Values reached can be given, on request.

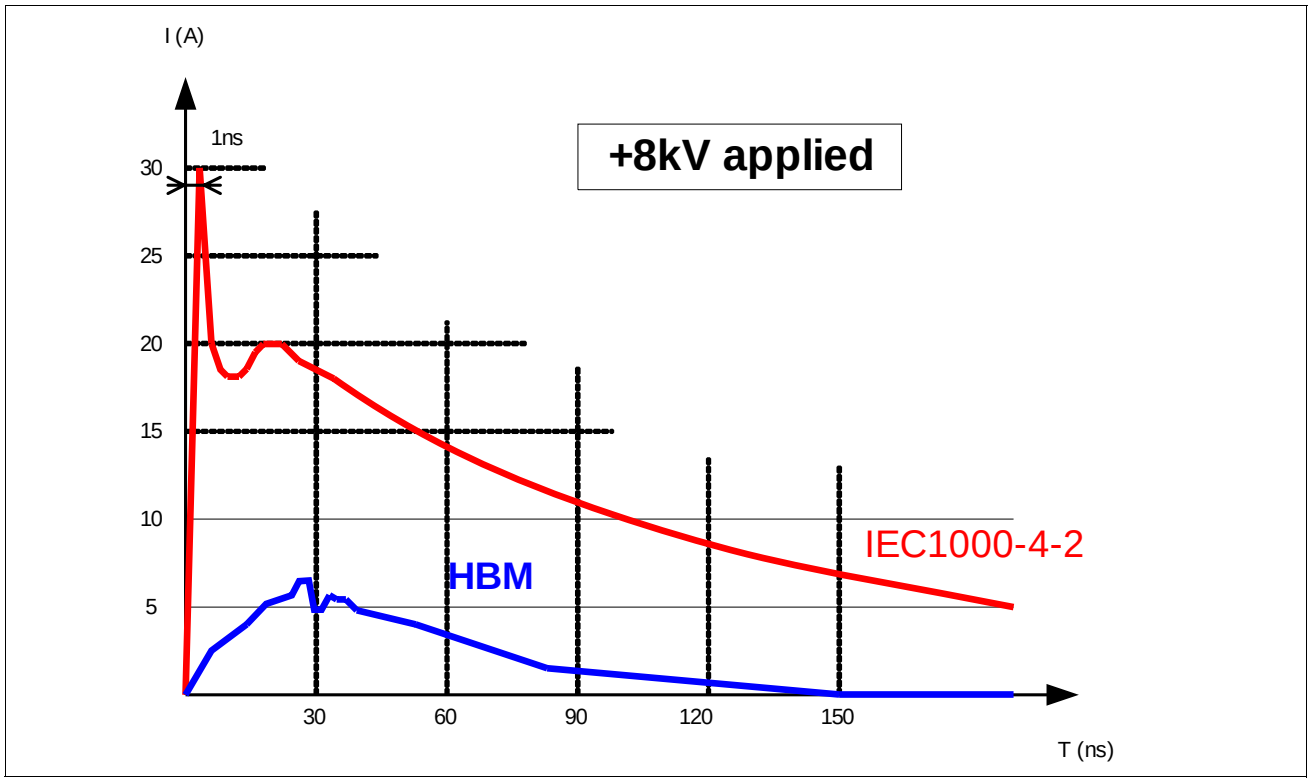
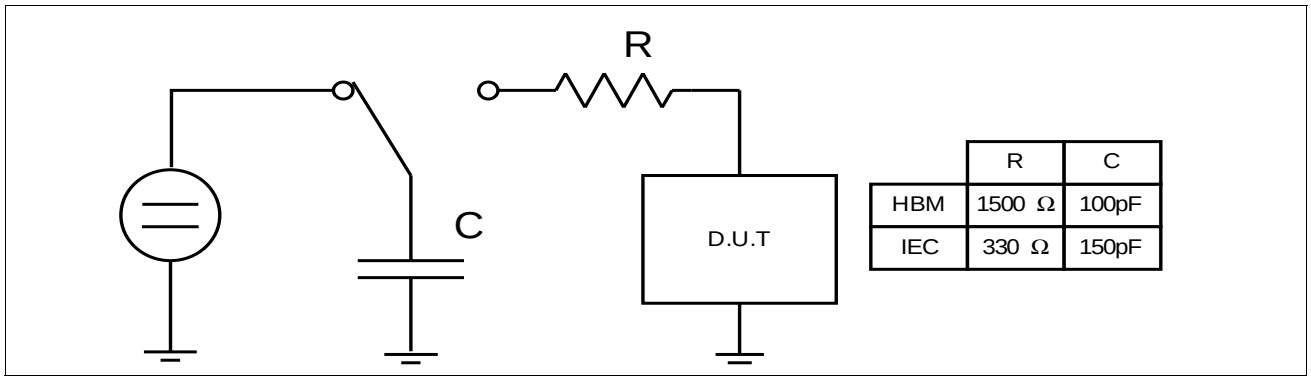


Figure 44 Comparison of the current between HBM and gun test.



	R	C
HBM	1500 Ω	100pF
IEC	330 Ω	150pF

Figure 45 ESD test equipement

6.1.3 Charged Device Model (CDM).

A device may also become charged. If it then contacts the insertion head or another conductive surface, a rapid discharge may occur from the device to the metal object. This event is known as the Charged Device Model (CDM) event, and can be more destructive than the HBM for some devices. Although the duration of the discharge is very short (often less than one nanosecond) the peak current can reach several tens of Ampere.

6.1.4 Machine Model (MM).

A discharge similar to the HBM event also can occur from a charged conductive object, such as a metallic tool or fixture. Originating in Japan as the result of trying to create a worst-case HBM event, the model is known as the Machine Model. This ESD model consists of a 200pF capacitor discharged directly into a component with no series resistor. As a worst-case human body model, the Machine Model may be over severe. However, there are real-world situations that this model represents, for example the rapid discharge from a charged board assembly or from the charged cables of an automatic tester.

6.2 ESD protection.

All infineon's product includes an internal ESD protection. The concept of the Infineon's ESD protection differs from the others silicon supplier. The ESD protection is turned ON as soon as the voltage reach a certain values. This values is actually specified in the datasheet **[1]**, **[2]**and **[3]**, as the absolute maximum rating. The avalanche voltage of the technology has to be higher than the ESD protection threshold.

The **Figure 46** shows the ESD proctection behavior. The standard protection is the most commonly used by semiconductors suppliers. The improved ESD protection is the typical behavior of the ESD protection all new Infineon's transceiver includes. Compared to the standard protection, it reduces the energy and heat into the device. Moreover, the Infineon's SPT technology allows low thermal resistance to the leadframe. The heat is then spread into the whole device, reducing the risk of hot spots (local overheat).

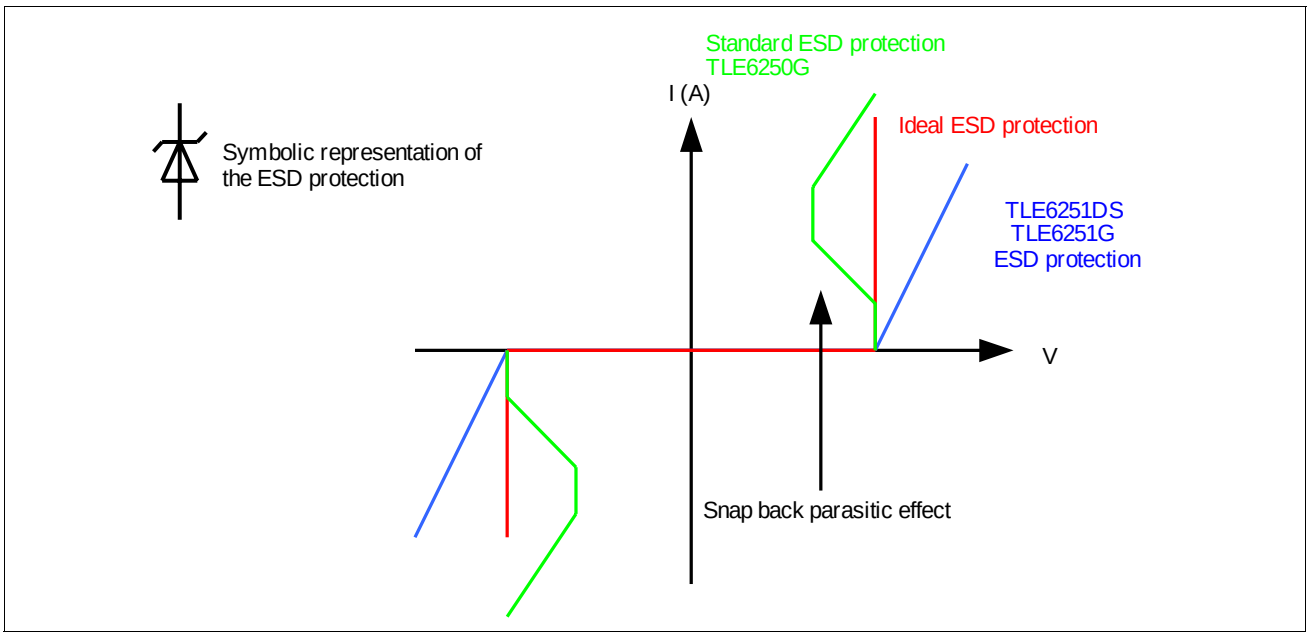


Figure 46 Standard and Infineon ESD protection

6.3 Modules under ESD gun test.

Figure 47 shows the test set up for the following section, with the respective external component.

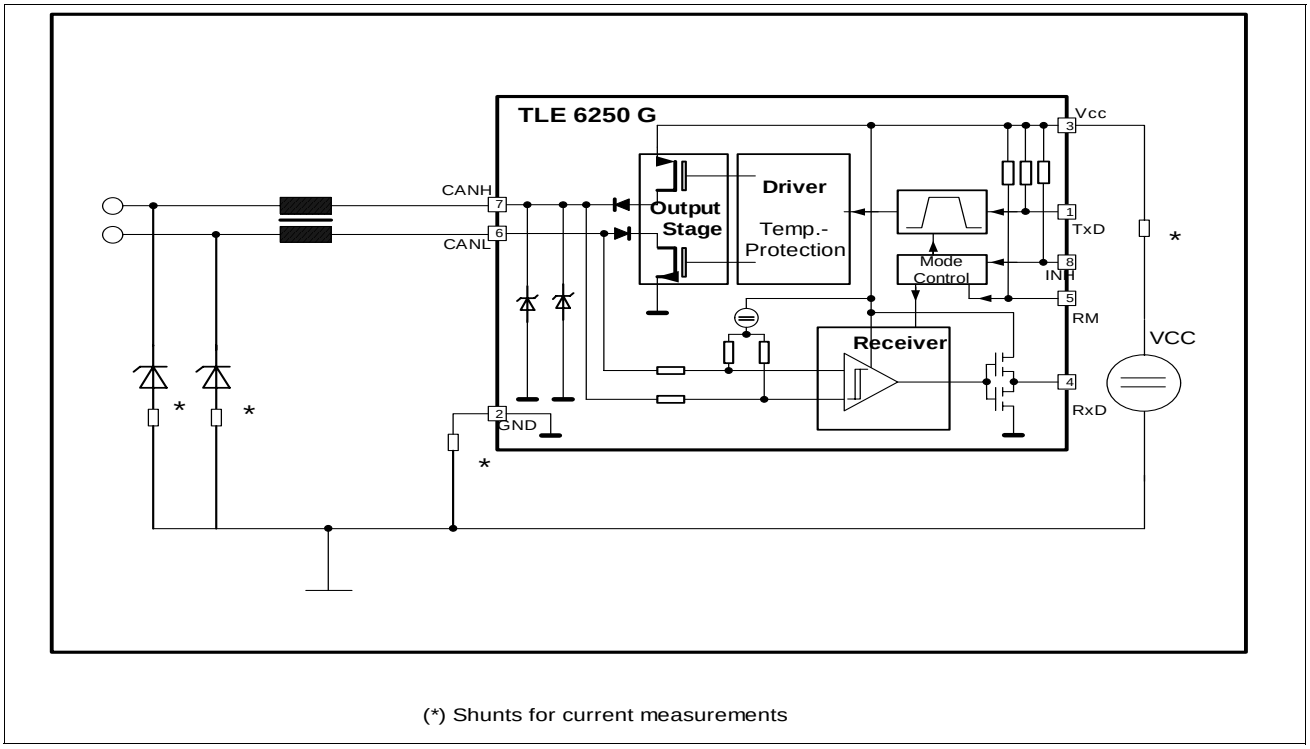


Figure 47 Schematic of the test

6.3.1 Device without any external protection circuitry.

The **Figure 48** and **Figure 49** shows the measurement realized at the ground line and Vcc line (device is supplied to the 5V), with 1kV gun test for the **TLE6250G**. The ESD discharge is applied on CAN_H.

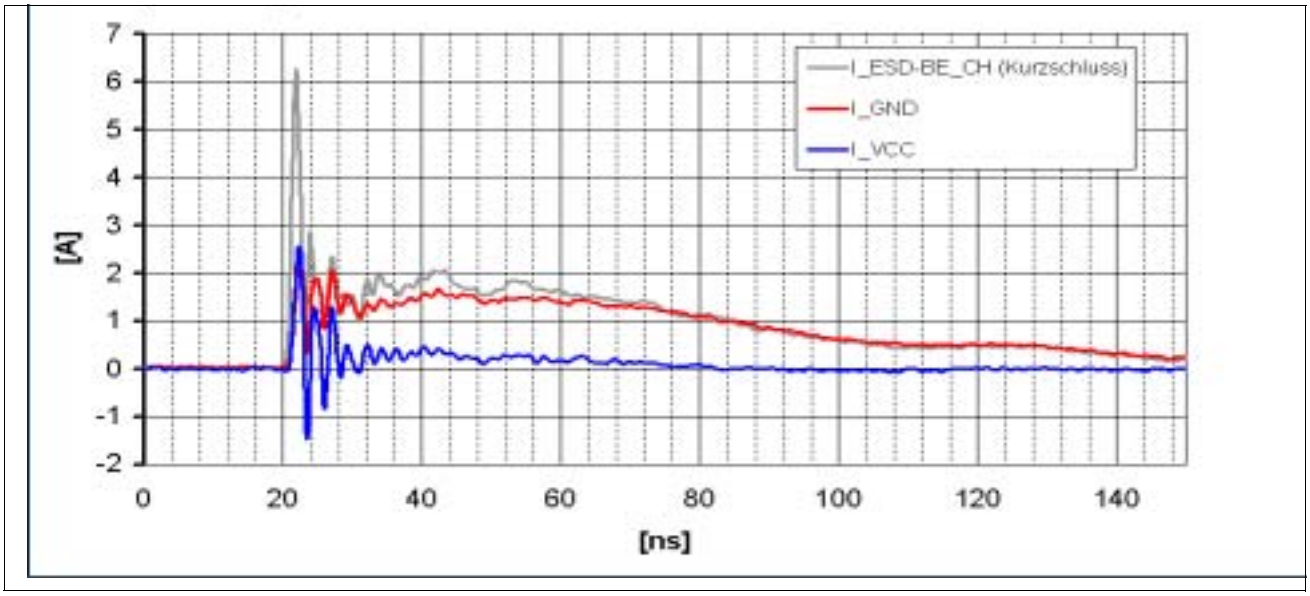


Figure 48 Positive ESD discharge, device supplied. Read out of the ground and supply current.

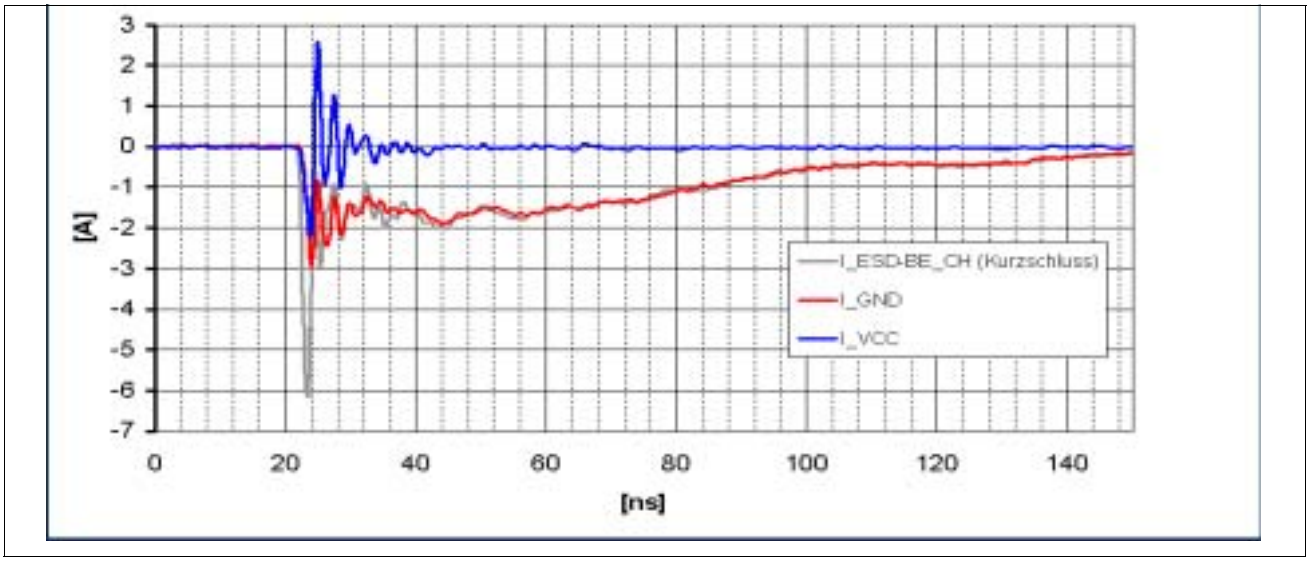


Figure 49 Negative ESD discharge, device supplied. Read out of the ground and supply current.

6.3.2 ESD level reached with a choke coil.

The purpose of the choke coil is described in the **Chapter 7**. The **Figure 50** shows the typical current flowing into the ground line during the ESD discharge. The measurements show that the choke coil has no real influence on the results and could not be considered as an efficient solution for ESD protection.

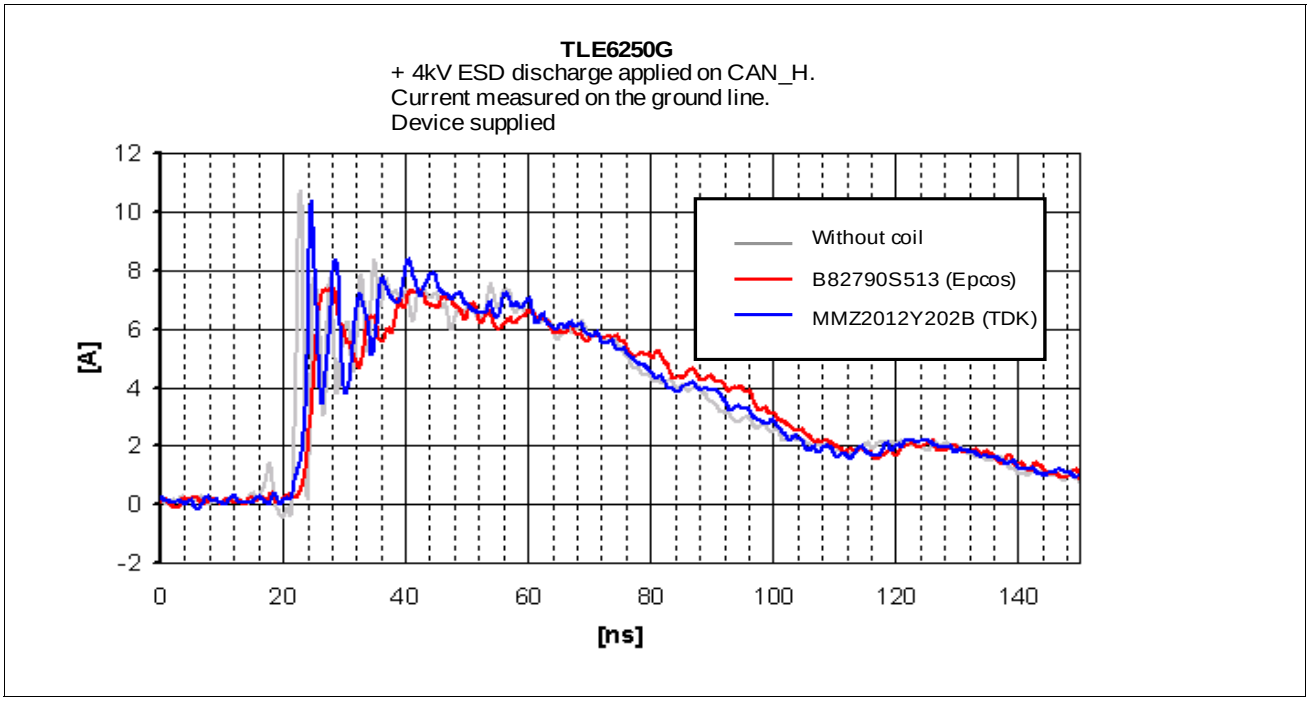


Figure 50 ESD discharge, device supplied. Read out of the ground current. With choke coil.

6.3.3 ESD level reached with a choke coil and ESD diode or varistor.

The **Figure 51** and **Figure 52** show the results on an ESD positive and negative discharges on the pin CAN_H, device supplied. The influence is clearly seen, when using both varistor and choke coil. Using the varistor alone doesn't influence too much the results, because the varistor isn't fast enough. Using these external components,

the current is no more flowing in the device but in the external protection circuitry. In this condition, the ESD robustness can reach very high values like 20kV.

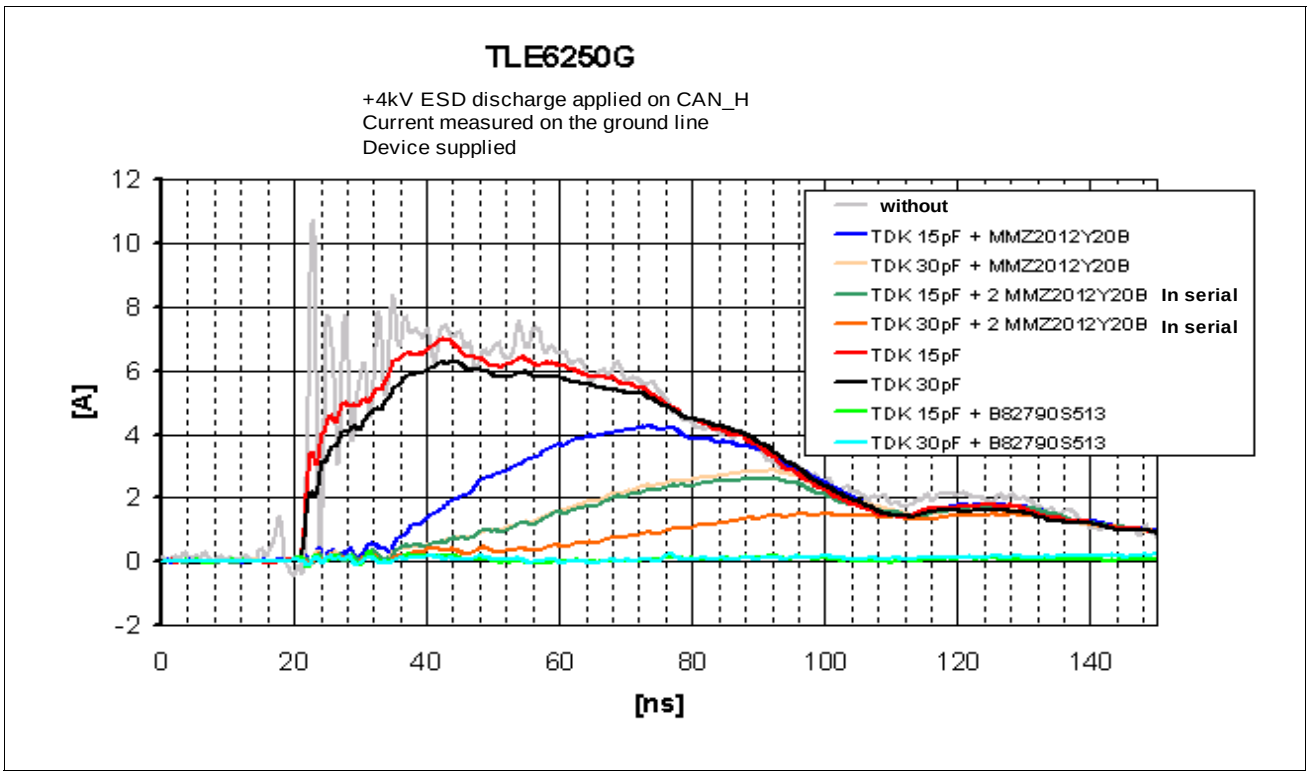


Figure 51 Positive ESD discharge, device supplied. Read out of the ground current. With varistor.

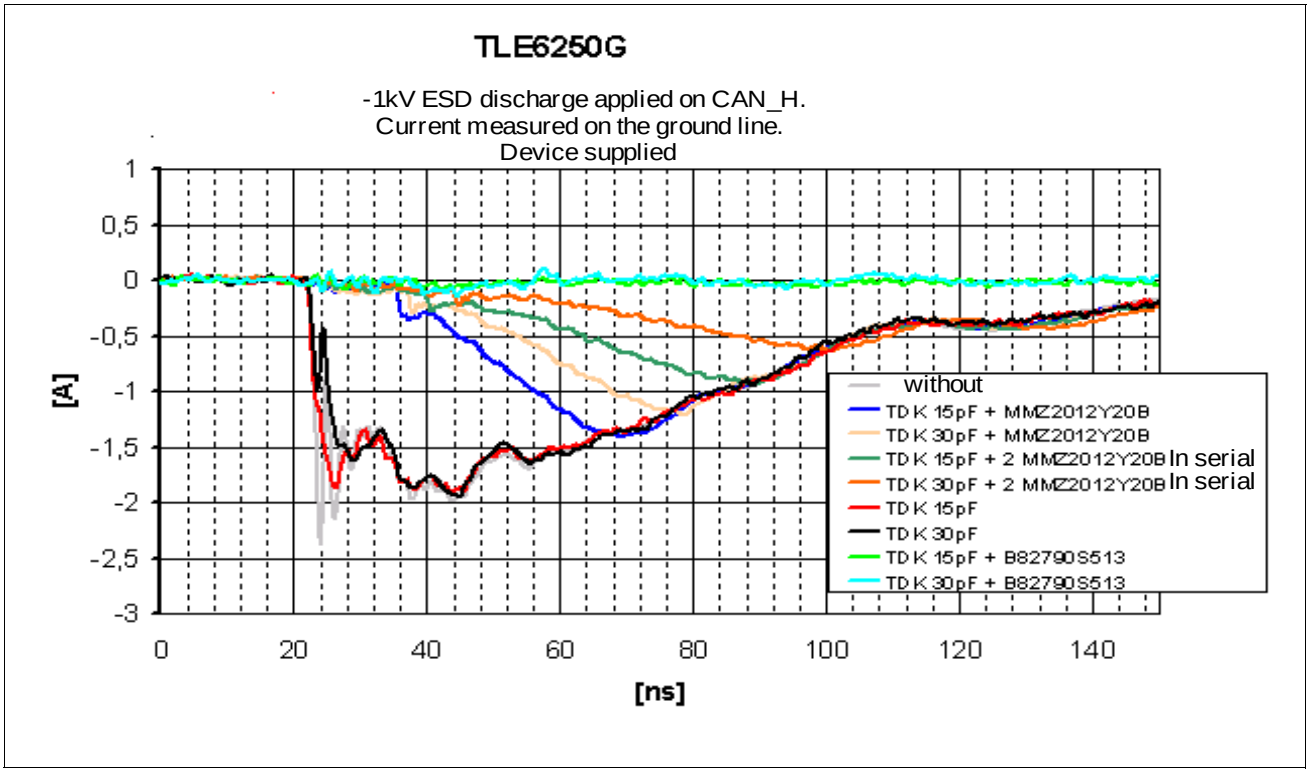


Figure 52 Negative ESD discharge, device supplied. Read out of the ground current. With varistor

6.4 PCB layout.

Knowing all this, and applying the good protection corresponding to the ESD requirement of the application, it is not given to pass successfully the ESD test. We saw in the **Chapter 6.3** that the ESD current is flowing in the ground of the device (or in the ground of the external protection). But the ground of the device can be something else than the ground of the module. To equal the two grounds, the PCB layout has to be designed with care.

The **Figure 53** shows the typical case where the ESD discharge is becoming an issue for the module.

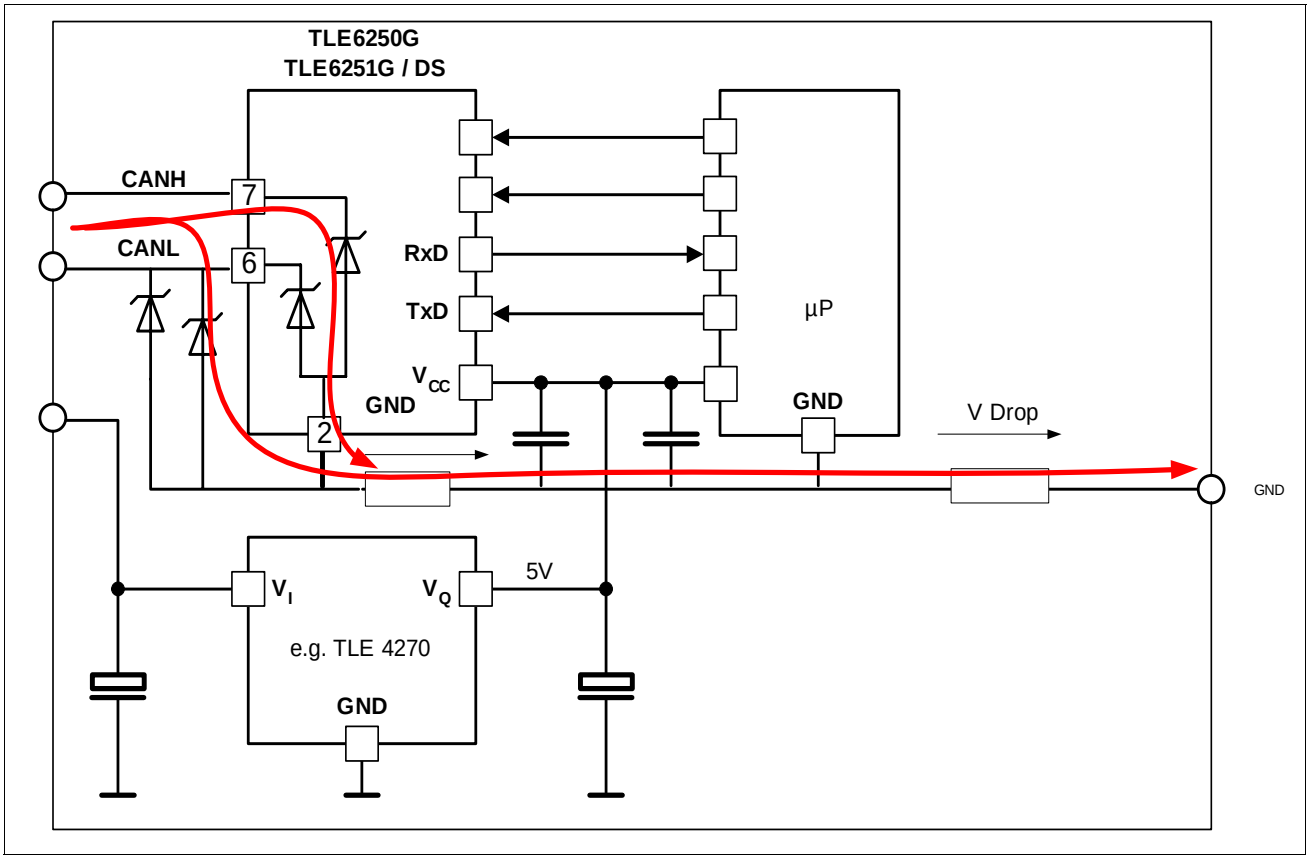


Figure 53 Bad PCB example for ESD.

In the case of the ESD discharge on CAN_H or CAN_L pin, if the ground connector is situated far from the transceiver, and with digital components as microcontroller in between, the ground line resistance cannot be neglicted. The resultance is an overvoltage, locally on the ground pin of the micro controller, and it can be easily destroyed !

The **Figure 54** shows the proper PCB design to avoid these issues. The ground connector has to be as close as possible to the transceiver.

6.5 Conclusion.

For the application targeting to have a good ESD robustness, layout of the board is very important. Providing external ESD protection described in **Chapter 6.3.3** can allow even more robust design. As the external protection is influencing the terminations concept, it is also necessary to check the **Chapter 5** to comply the bus requirements. In case of varistor usage, a choke coil or at least two coils are necessary. It´s tempting to reduce the varistor threshold voltage. This will improve the ESD robustness of course, but the EMI (**Chapter 7**) results will be definitly jeopardized.

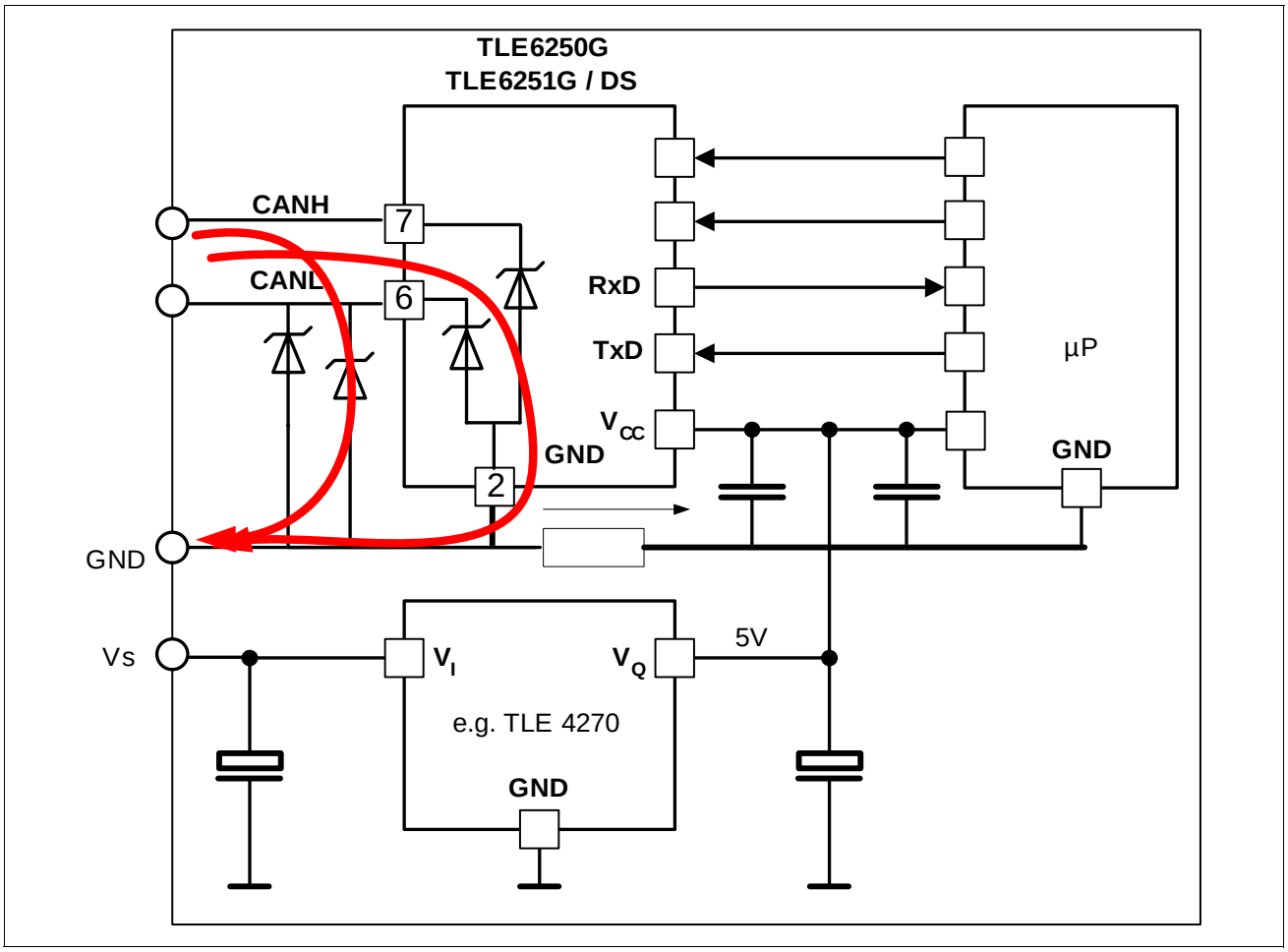


Figure 54 Good PCB design for ESD robustness

7 EMC aspect.

The Electro-Magnetic-Compatibility is a challenge to achieve with CAN applications. Main reason is the wiring harness of the CAN system running into the complete vehicle. The chance to encounter interferences, or to create interferences in the neighbor of the cables is very high without any design care. In EMC, two domains are considered, immunity (EMI) and emission (EME).

7.1 EM Immunity against transcients.

The transcients that the transceivers are facing are mainly defined in the international standard ISO 7637 part 1 and 2. It consists on checking whether the device is still running properly, or withstand the disturbances and goes back to normal operation afterwards, or might be destroyed. The behavior requested is up to the OEM. The ISO pulses 1, 2 and 3 are representing the disconnection of an inductive load in the wiring harness.

7.2 EM Immunity against RF disturbances.

The RF disturbances can be tested by several means. They are described in the ISO11452.

7.2.1 The Stripline test. ISO 11452-5.

The stripline test provides a uniform transverse electromagnetic field with the electric field across the strips and the magnetic field parallel to them. Parallel-plate or co-planar lines are used with the lower plate bounded to the shielded enclosure in which the test takes place. Such lines allow units to be subjected to plane waves over a wide frequency range, and with high field strengths.

7.2.2 The Bulk Current Injection test. (BCI). ISO 11452-4.

Bulk Current Injection (BCI) is a test technique pioneered in the aircraft industry which uses current probes (both pick-up and injection) to couple a 50Ω test and measurement system to a conductor or bundle of conductors such as a vehicle wiring harness. The probes themselves are RF transformers. An injection probe is driven from the output of an RF amplifier and couples the current into the harness of the equipment under test by acting as the primary of a transformer - the single turn of the harness acting as the secondary. Pick-up probes act in a similar way but this time allow the bulk current in a harness to be monitored using a power meter.

7.3 Infineon transceivers in the EMI disturbances.

7.3.1 Immunity against transcients.

The device design is optimized to withstand the ISO pulses. To check it, all devices are checked by an independant laboratory, the IBEE. They do apply two tests, the damage and the malfunction test.

7.3.1.1 Damage test.

Purpose of the damage test is to check whether or not the device withstands the ISO pulses, without any destruction. The levels of voltage applied are indicated in the **Table 4**. All infineon high speed transceivers withstand the distrubances, without destruction.

Table 4 Damage test

Test pulse	Vs max (V)	Pulse repetition frequency (Hz)	Test duration (mn)	Remarks
1	-100	2	10	t2 = 0s
2a	+100	2	10	t2 = 0s
3a	-150	10	10	
3b	+150	10	10	

7.3.1.2 Malfunction test.

During the malfunction test the voltage is increased, for each pulses, until the device is definitively broken.

The reached values can be given, on request.

7.3.2 Immunity against RF disturbances.

The TEM cell, as well as the BCI tests, are tests at module's level. The results are stongly dependant on the application. It would be possible to test the device in these condition, but the interpretation of the device robustness would be impossible, since there's as much set-up as there are applications. To avoid this and to get the information on the RF disturbances robustness, the Direct Power Injection (DPI) test is implemented.

7.3.2.1 BCI test limitation

The **Figure 55** shows the typical case of the limitation of BCI, for component test. The transceiver is alone on the board (for component test). The current probe is injecting 200mA for example. In that case, and assuming the device is recessive or OFF, so having an impedance of 30kΩ as a minimum, the voltage on the pins CAN_H and CAN_L will reach 100mA x 30kΩ = 3000 V theoretical (In practice the ESD diode is turning ON). The question is no more to know if the device will be perturbated, but to know if it can overcome the test ! As soon as a capacitor is present, this computation isn´t relevant anymore. But then, it´s no more component test but a test at module's level.

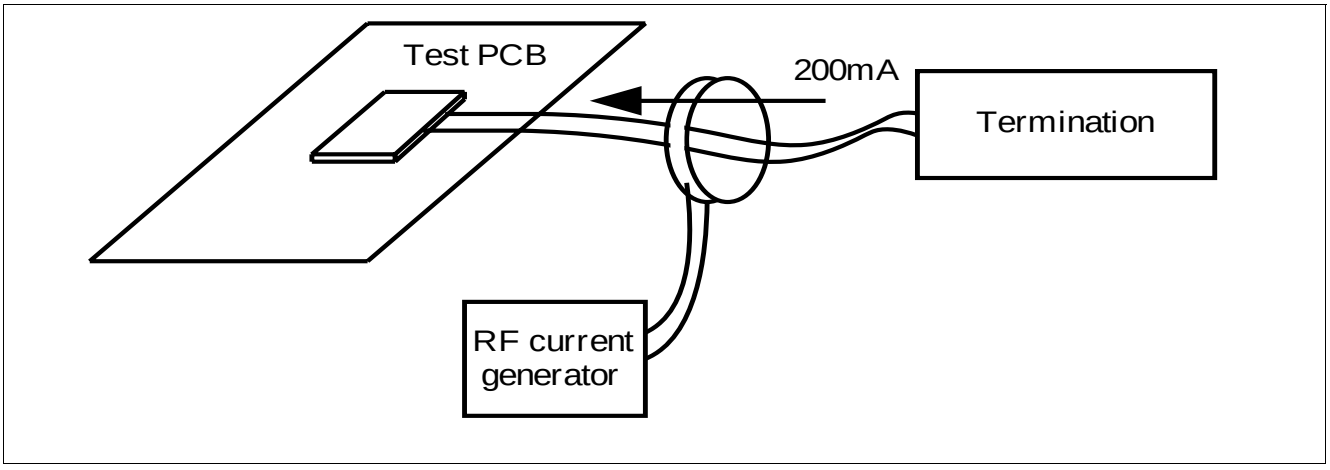


Figure 55 BCI test limitation example

7.3.2.2 Principle of the DPI test.

The DPI test is, from a principle point of view, similar to the BCI test. The principle is to inject a certain AC voltage, modulated or not, and to check the integrity of the signal (via the RxD pin or the NERR pin of the transceiver). The test set up consists of 3 identical transceivers, soldered on a defined PCB. CAN bus is traced on the PCB. Instead of a current injection, the power is injected via a capacitor (C5 and C6 on **Figure 56**), and measured in dBm, or Watt. As for the BCI, the power injected is monitored to check the possible reflexions on the bus. One of the main benefit of the DPI method is to allow comparison between different supplier's design on an identical test bench, via a consortium as the ICT for example.

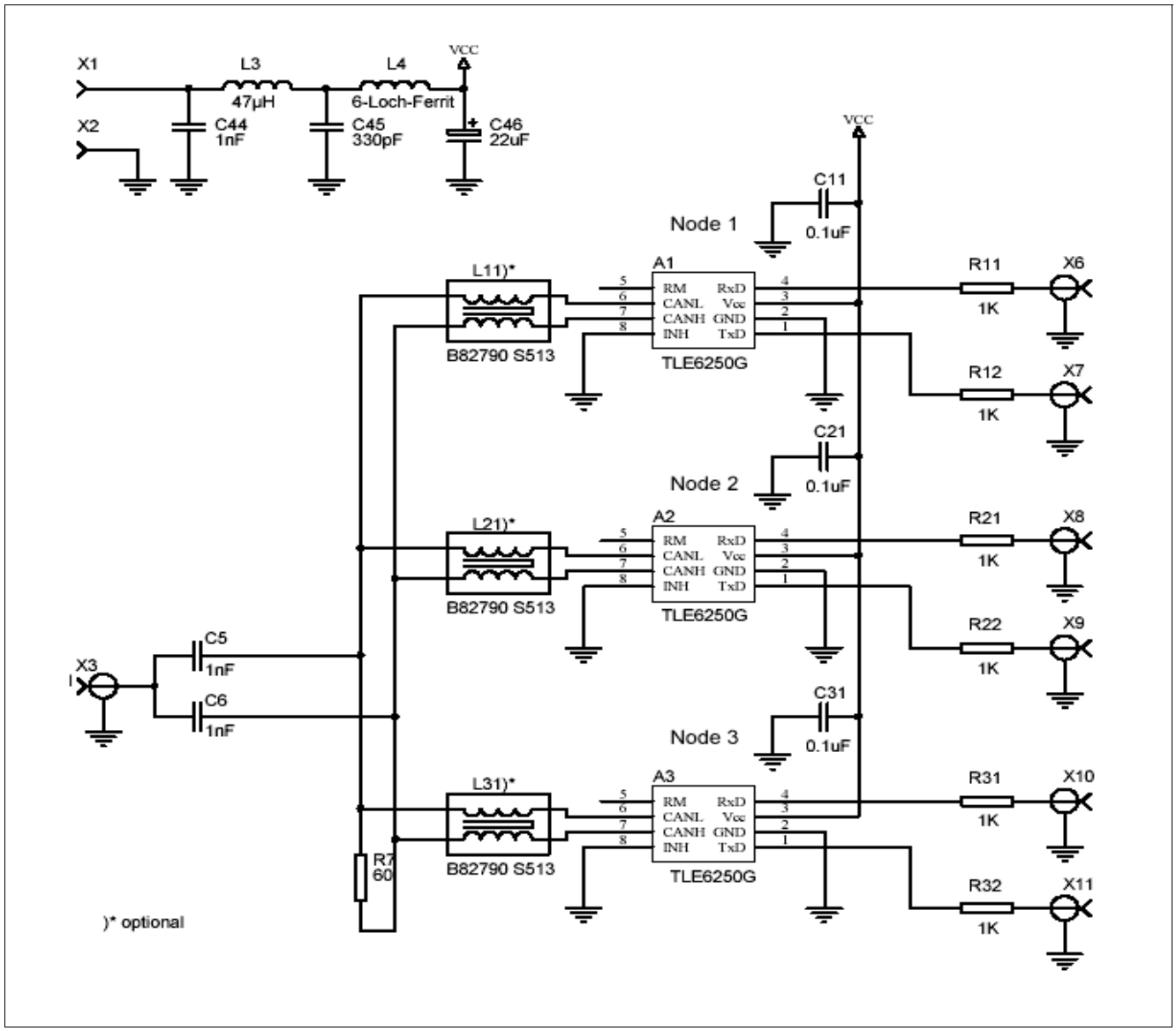


Figure 56 DPI test set up

From the DPI results, the BCI and TEM cell result can be easily assessed. The DPI shows the results we can reach with a perfect module design, on BCI and TEM cell.

7.3.2.3 Results of Infineon's transceiver under DPI test.

The results can be given on request. The **Figure 57** shows a typical DPI result curve on the well known TLE6250G. Others transceivers are available on request. On the X axis, we can find the frequency range. On the Y left axe, we can find the maximum power injected without failure. An ideal transceiver would have a straight curve, so 36dBm injected without any failure. On the Y right axe, we can find the voltage in Volt RMS of the power injected, reflecting the reflexions of the line.

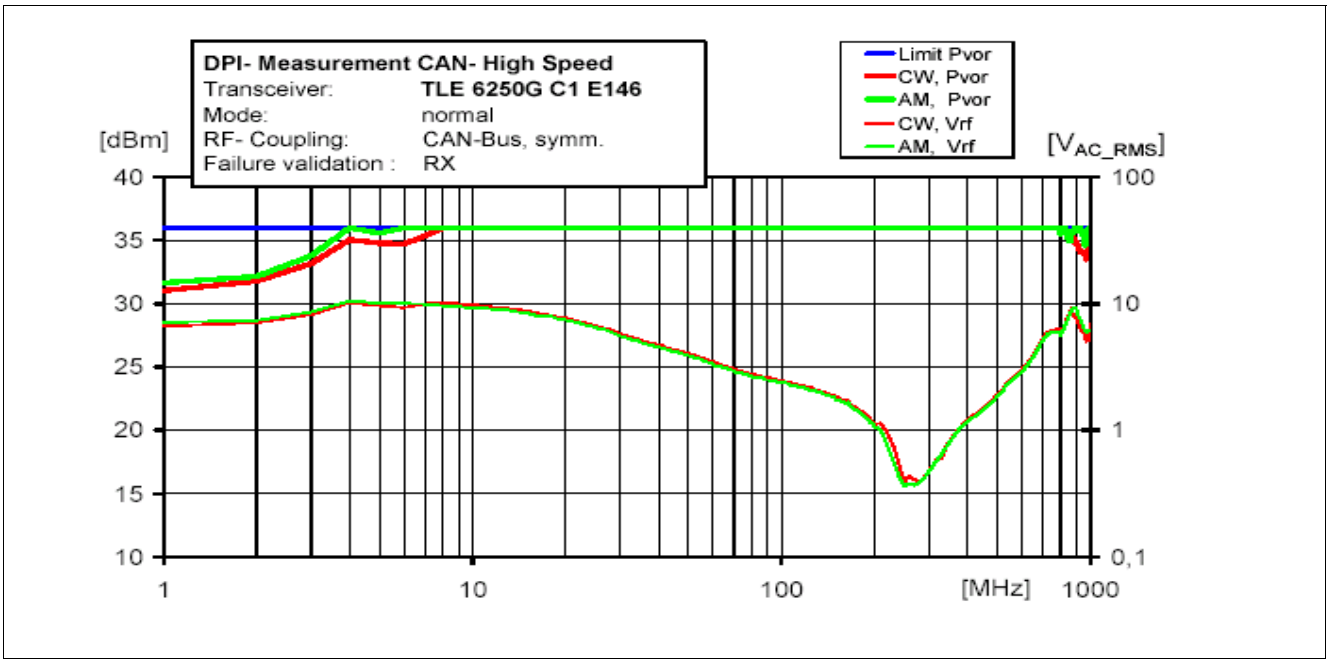


Figure 57 DPI test results example : The TLE6250G

7.3.2.4 Improvement of the DPI result. Use of choke coil.

When the transceiver shows weaknesses from the DPI test, a solution is to use a choke coil. The **Figure 58** shows the principle of the choke coil. The operation current IO induces a magnetic flow ϕO. The sum of both induced magnetic flow is ϕO - ϕO =0. So the common mode choke doesn´t influence the signal current at all. The common mode interference induces a flow ϕi that sums up to a flow ϕi + ϕi =2 ϕi. This magnetic flow „sees“ a strong damping by the system inductance of the magnetic ring (high permeability) and so it is also damping the resulting interference current of the system. The choke coil should be chosen within a high µ (L=11, 22, 33, 51µH), a low Q factor, very low (100...300mΩ) resistance and a high resonnance frequency. And of course, the coil should withstand the short circuit current so 200mA. The B82790S513 (51µH) from Epcos or the MMZ2012Y202B (51µH) from TDK for instance are matching these requirements.

It is important to notice the choke coil filters the parasitics coming in the module, as well as the eventual parasitics created by the transceiver itself, only if the disturbances are on both channels (like BCI and TEM cell). In case only CAN_H or CAN_L is disturbed / is disturbing, the choke coil is useless. To get rid of such parasitics, it´s preferable to use a capacitor and / or a coil.

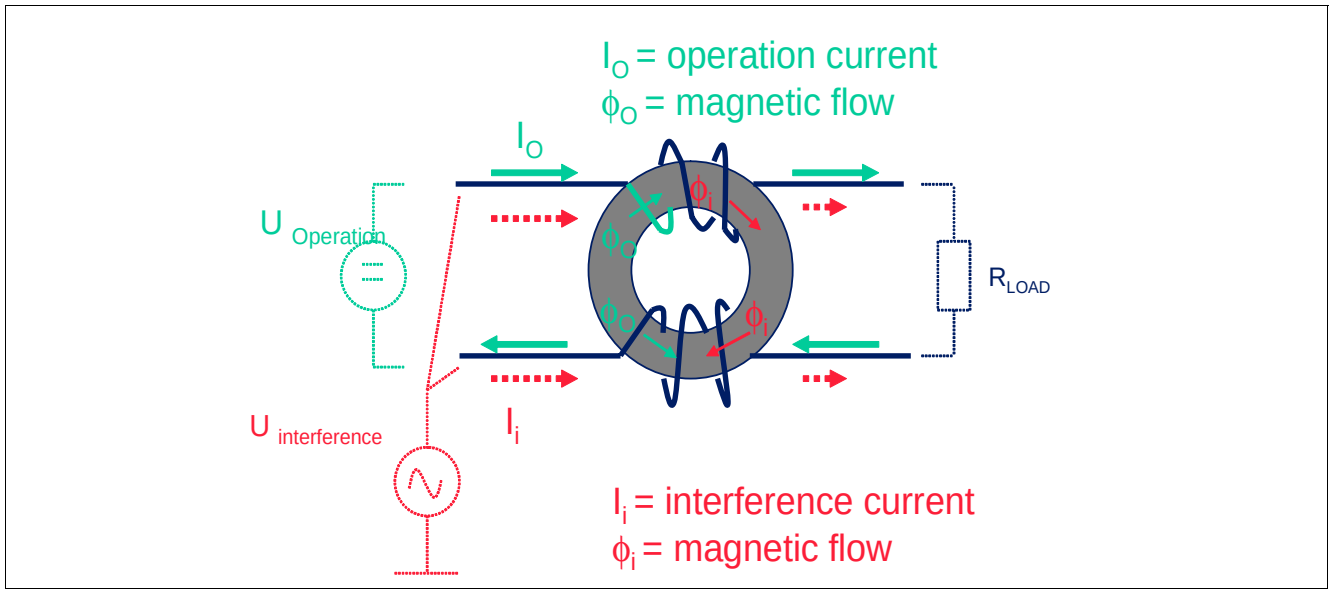


Figure 58 Choke coil principle

The **Figure 59** shows the results, witht the same set up as on the **Figure 57**, adding a chock coil, suppressing the traditionnal weakness at low frequency.

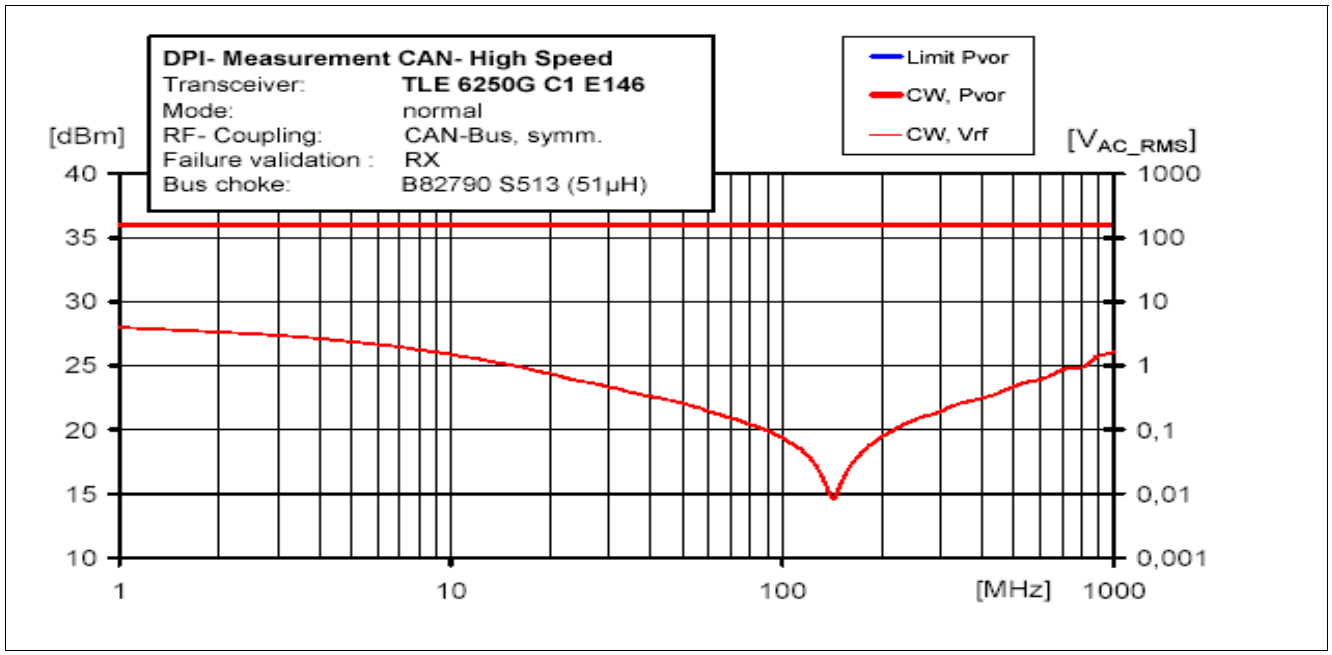


Figure 59 DPI test results with choke coil for the TLE6250G.

7.3.3 Emission

As well as for the immunity test, the emission can be performed on the same test bench as for the DPI method. To get emission, it is necessary the transceiver is emitting. The ICT has stated two test pulses. The first one is a square wave of 250kHz matching an high baudrate application. The second test signal is a 90% duty cycle, at a frequency of 50kHz, matching a low baudrate application. The **Figure 60** shows the results of the TLE6250G under these conditions. The disturbances are measured on the Y axe in dBµV, the X axe is showing the frequency.

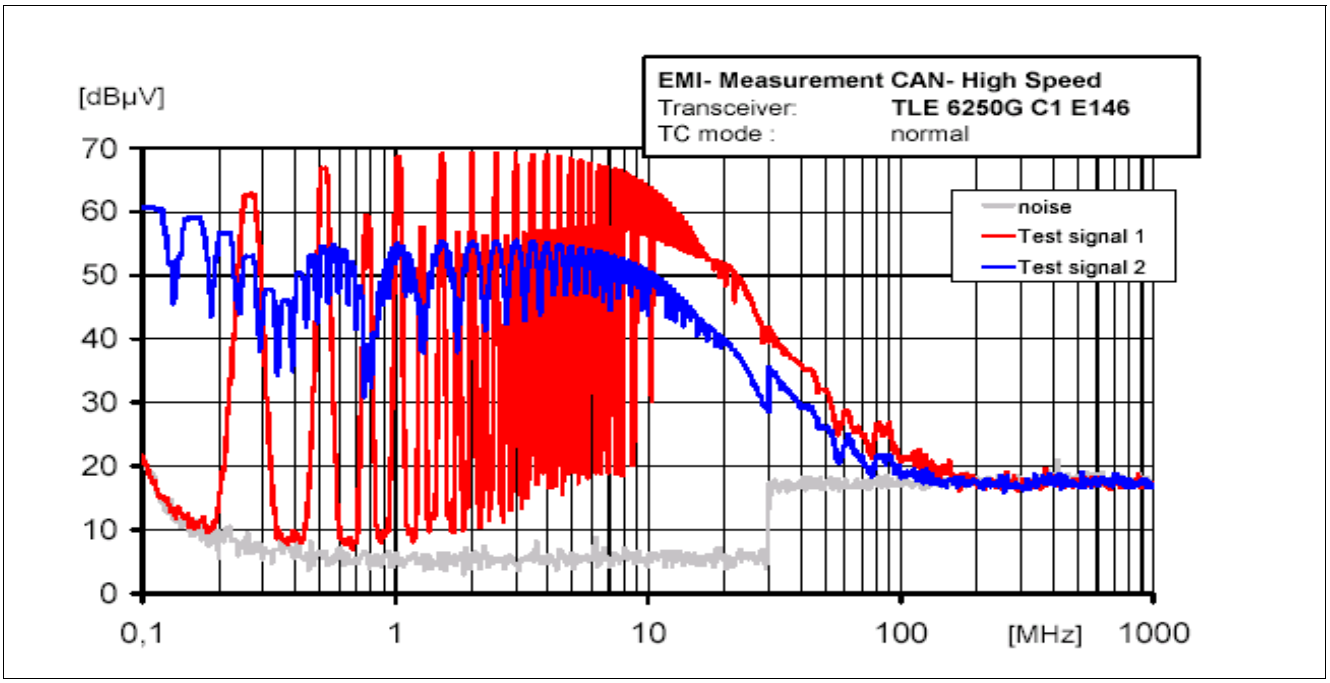


Figure 60 EME test results with TLE6250G, without chock coil

As well as for the immunity, a choke coil can be used. The **Figure 61** shows the benefit of the chock coil for the test signal 1 (square wave of 250kHz). At least 10dBµV reduction can be observed.

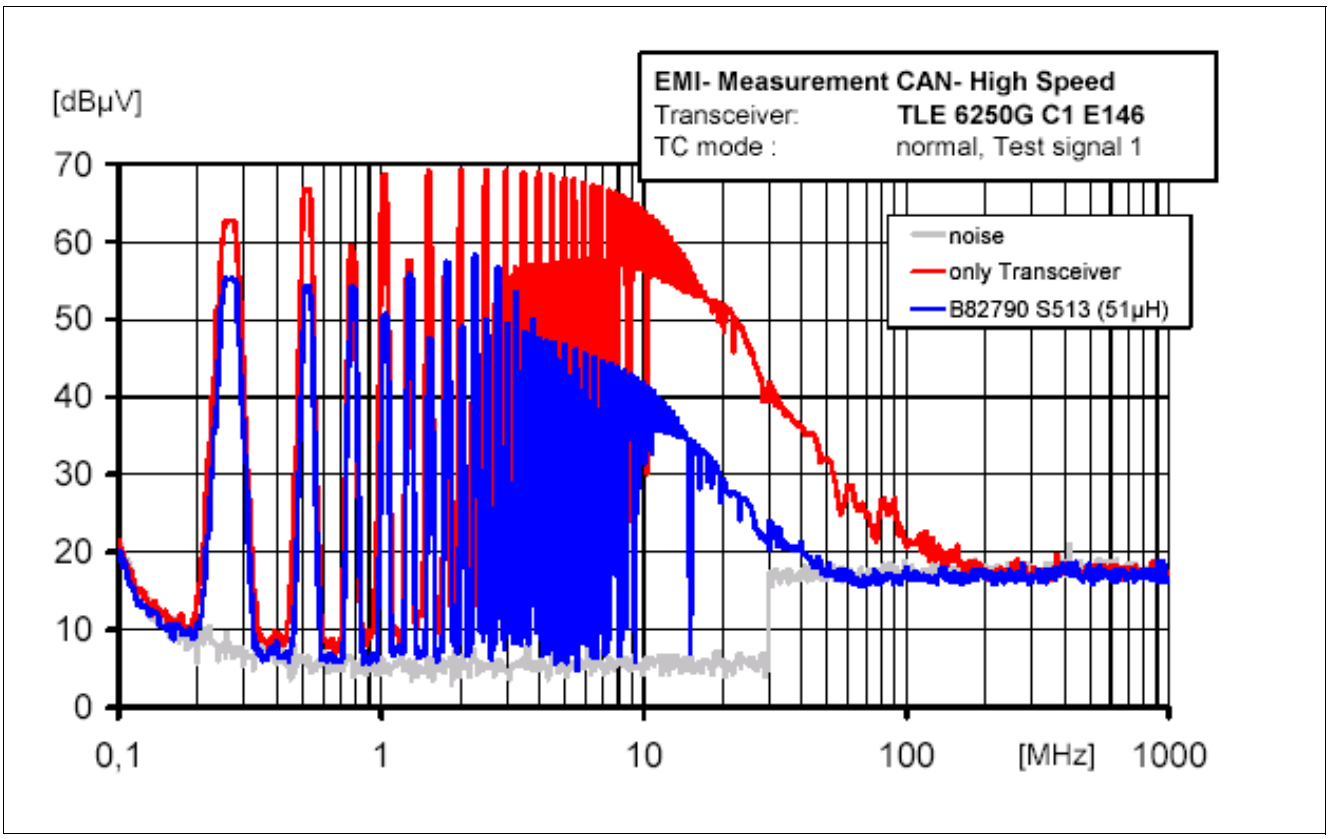


Figure 61 EME test results with TLE6250G with and without chock coil

7.4 Conclusion.

As well as for the ESD, the EMC performance of the application is strongly dependant on the design care. It is recommended to plan a choke coil, even if the EMC module test shows good results without. All Infineon's transceiver are tested according to the method described in this chapter and the reports for each particular parts are available on request. Similar to the comparison between the component test and the module test, the result of car test is difficult to predict.

8 Products summary

Functionality	TLE6250G	TLE6250GV33	TLE6251DS	TLE6251G	Unit	comments
Vcc supply	[4,5;5,5]	[4,5;5,5]	[4,75;5,25]	[4,75;5,25]	**V**	
Vio	no	[3.0 ;5,5]	no	[3.0 ; 5,25]	**V**	
Vs	no	no	no	[5 ; 40]	**V**	
Enable	Yes	Yes	Yes	Yes		
Bus wake up	No	No	Yes	Yes		
Bus bias in unpowered mode	GND	GND	weak GND	weak GND		
SPLIT pin	no	no	Yes	Yes		
ESD	6	6	6	6	**(+/-) kV**	
INH output	no	no	no	Yes		
Bus time out	no	no	yes	yes		

Abbreviation	Meaning	Comment
BCI	Bulk Current Injection	
CAN	Controller Area Network	
CDM	Charged Device Model	ESD test
DPI	Direct Power Injection	EMC test
DUT	Device Under Test	
EMC	Electro-magnetic Compatibility	
EME	Electro-magnetic Emission	
EMI	Electro-magnetic Immunity	
EOS	Electrical Over Stress	
ESD	Electro Static Discharge	
HBM	Human Body model	
HS CAN	High Speed CAN transceiver	
IBEE	IngenieurBurö für industrielle Electrotechnik / Electronik	
ICT	International Conformance and Testing	
IEC	International Electrotechnical Commision	
INH	Inhibit	
ISO	International Standard Organization	
LDO	Low Drop Output	Other name for Voltage regulator
MM	Machine Model	ESD test
OEM	Original Equipement Manufacturer	In the frame of this document, it means car maker
SC	Short Circuit	
SPT	Smart Power Technology	Bipolar CMOS and DMOS technology developped by Infineon

9 References.

[1] Data Sheet High speed CAN, TLE6250G Infineon Technologies AG - Version 3.8

[2] Data Sheet High speed CAN, TLE6251DS Infineon Technologies AG - Version 3.0

[3] Data Sheet High speed CAN, TLE6251G Infineon Technologies AG - version 3.1

[4] Data Sheet, TLE4278G Infineon Technologies AG - version

[5] International Standard ISO 11898-2, Road Vehicles - Controller Area Network (CAN) part 2 High speed medium access unit.

[6] International Standard ISO 11898-5, Road Vehicles - Controller Area Network (CAN) part 5 High speed medium access unit.

[7] Data Sheet, Voltage regulator TLE4275G Infineon Technologies AG version 1.4

[8] Data Sheet, Voltage regulator TLE7270G Infineon Technologies AG version 0.21

[9] Data Sheet, Voltage regulator TLE4266-2G Infineon Technologies AG version 1.2

www.infineon.com

Published by Infineon Technologies AG