ON Semiconductor

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MSQA6V1W5T2G, SZMSQA6V1W5T2G

ESD Protection Diode Array

Low Clamping Voltage

This quad monolithic silicon voltage suppressor is designed for applications requiring transient overvoltage protection capability. It is intended for use in voltage and ESD sensitive equipment such as computers, printers, business machines, communication systems, medical equipment, and other applications. Its quad junction common anode design protects four separate lines using only one package. These devices are ideal for situations where board space is at a premium.

Features

- Low Clamping Voltage
- Stand Off Voltage 3 V
- Low Leakage < 1 μA @ 3 V
- SC−88A Package Allows Four Separate Unidirectional Configurations
- IEC1000−4−2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Package is Available*

Mechanical Characteristics:

- Void Free, Transfer−Molded, Thermosetting Plastic Case
- Corrosion Resistant Finish, Easily Solderable
- Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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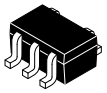
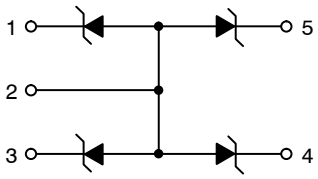
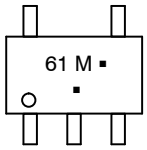


SCALE 2:1

SC−88A/SOT−323
CASE 419A



MARKING DIAGRAM



61 = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MSQA6V1W5T2G	SC−88A (Pb−Free)	3,000 / Tape & Reel
SZMSQA6V1W5T2G	SC−88A (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*T2 Suffix Devices are Packaged with Pin 1 Opposing Sprocket Hole.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation @ 20 μs @$T_A \le 25°C$ (Note 1)	P_{pk}	150	W
Steady State Power – 1 Diode (Note 2)	P_D	385	mW
Thermal Resistance Junction–to–Ambient Above 25°C, Derate	$R_{\theta JA}$	325 3.1	°C/W mW/°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Operating Junction and Storage Temperature Range	T_J T_{stg}	–55 to +150	°C
ESD Discharge MIL STD 883C – Method 3015–6 IEC1000–4–2, Air Discharge IEC1000–4–2, Contact Discharge	V_{PP}	16 16 9	kV
Lead Solder Temperature (10 s duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non–repetitive current per Figure 5. Derate per Figure 10.
2. Only 1 diode under power. For all 4 diodes under power, P_D will be 25%. Mounted on FR–4 board with min pad.

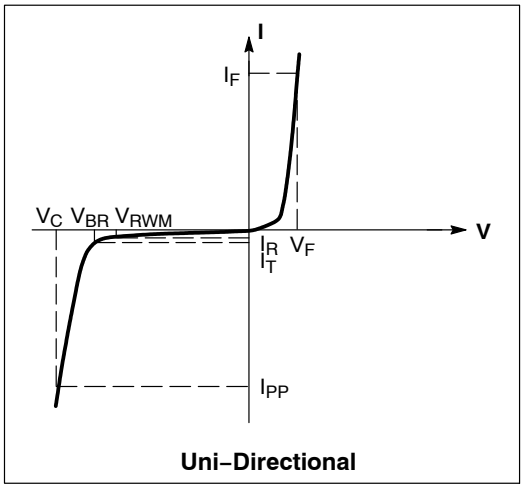
See Application Note AND8308/D for further description of survivability specs.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni–Directional

ELECTRICAL CHARACTERISTICS

Device*	Breakdown Voltage V_{BR} @ 1 mA (Vo) (Note 3)			Leakage Current I_{RM} @ V_{RWM} = 3 V (μA)	Capacitance @ 0 V Bias (pF)	Max V_F @ I_F = 200 mA (V)	V_C
	Min	Nom	Max				Per IEC61000–4–2 (Note 4)
MSQA6V1W5T2G	6.1	6.6	7.2	1.0	90	1.25	Figures 1 and 2 See Below

3. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

*Include SZ-prefix devices where applicable.

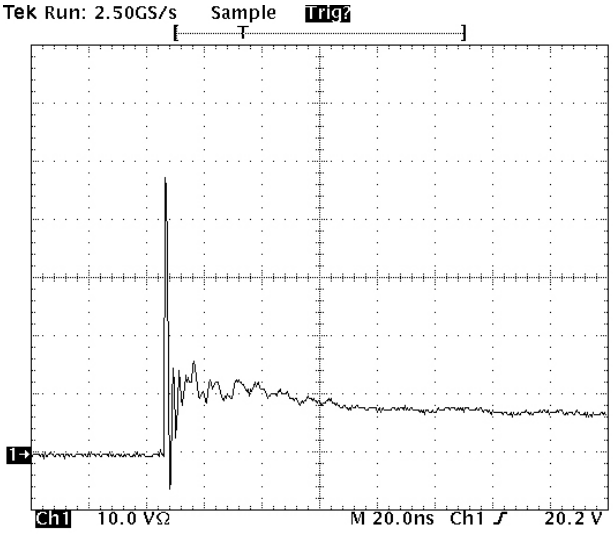


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

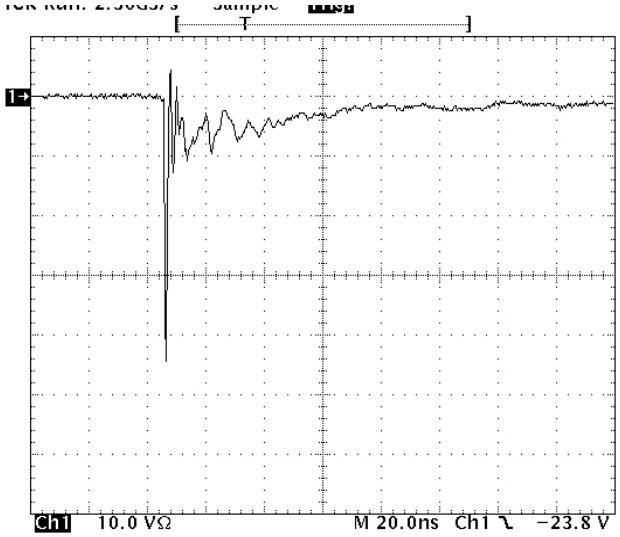


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

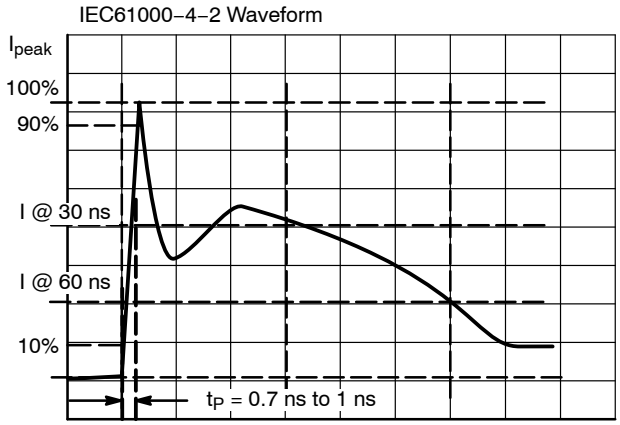


Figure 3. IEC61000−4−2 Spec

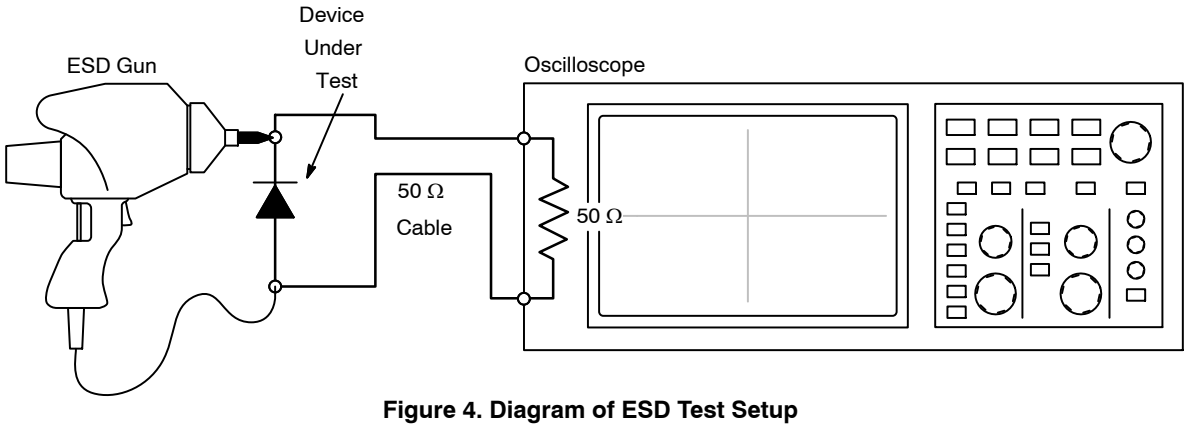


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

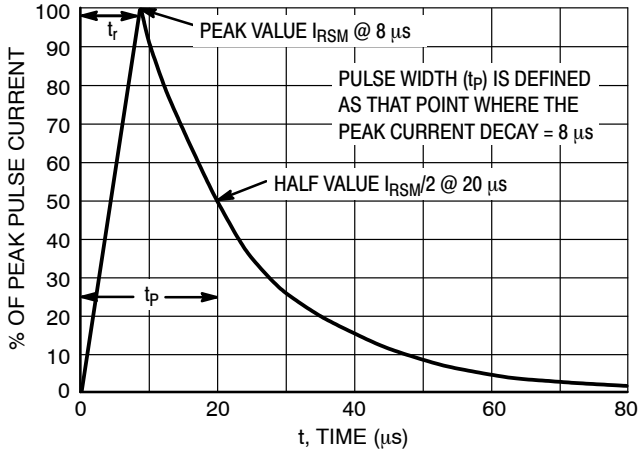


Figure 5. 8 x 20 μs Pulse Waveform

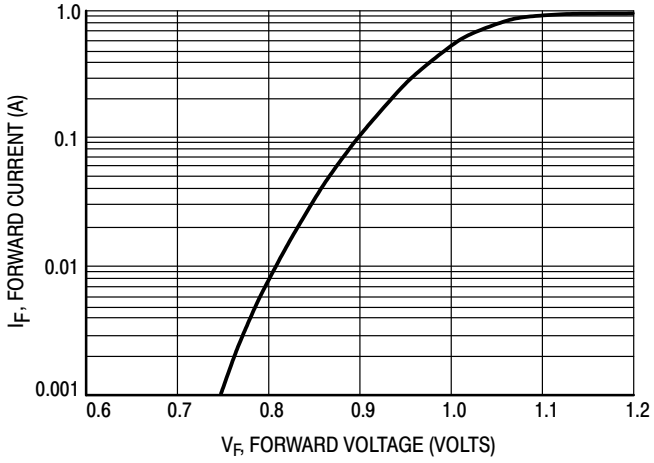


Figure 6. Forward Voltage

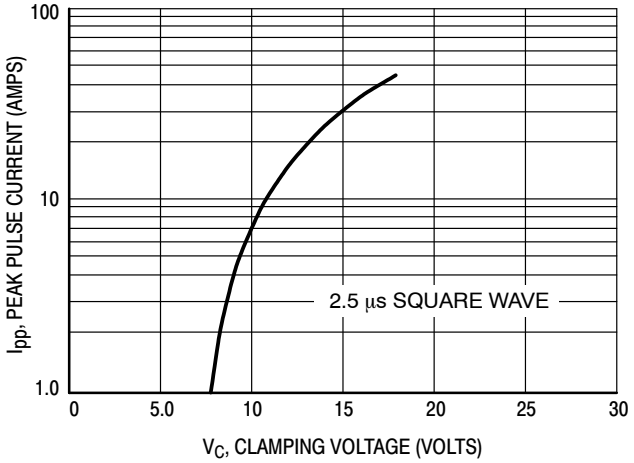


Figure 7. Clamping Voltage versus Peak Pulse Current (Reverse Direction)

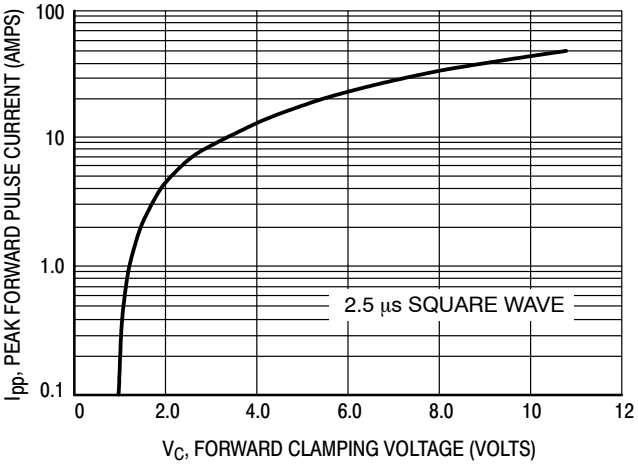


Figure 8. Clamping Voltage versus Peak Pulse Current (Forward Direction)

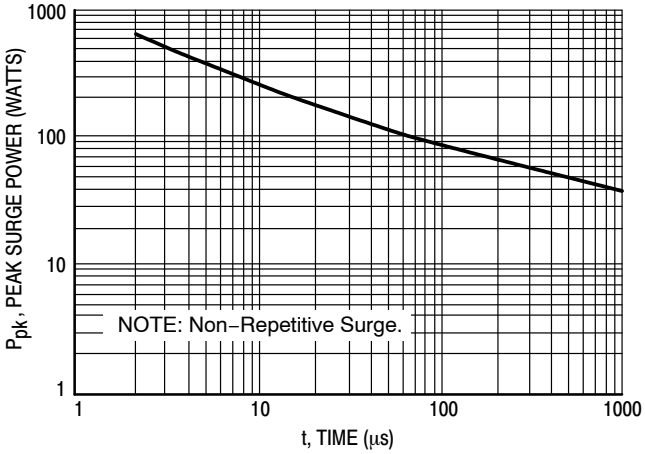


Figure 9. Pulse Width

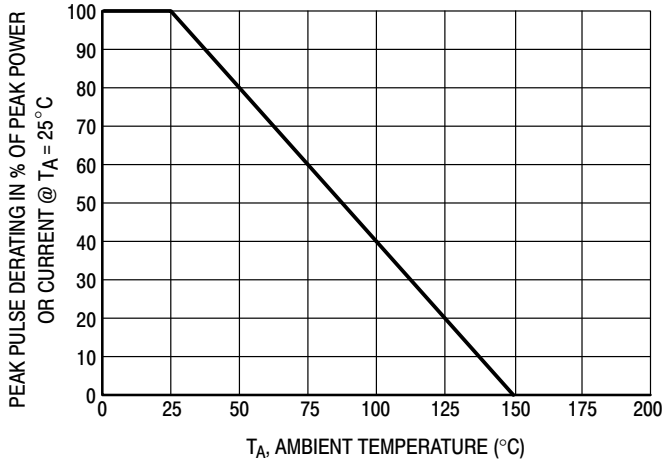


Figure 10. Pulse Derating Curve

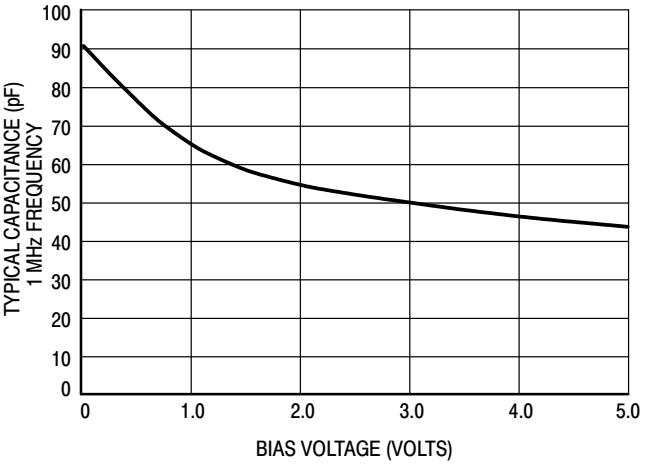


Figure 11. Capacitance

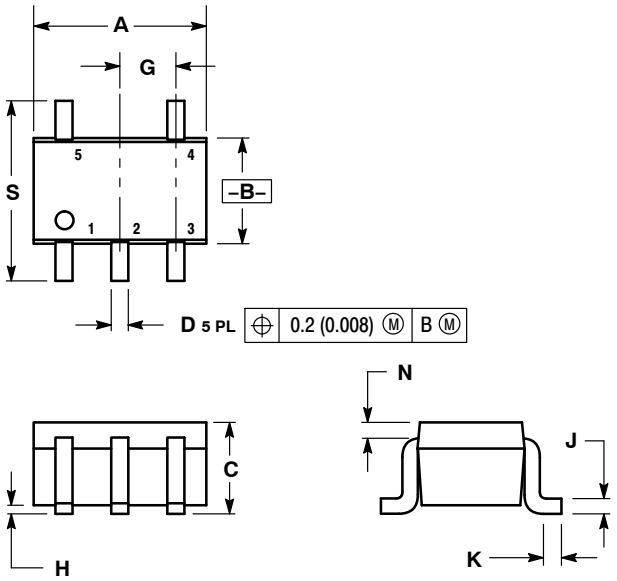
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

SCALE 2:1

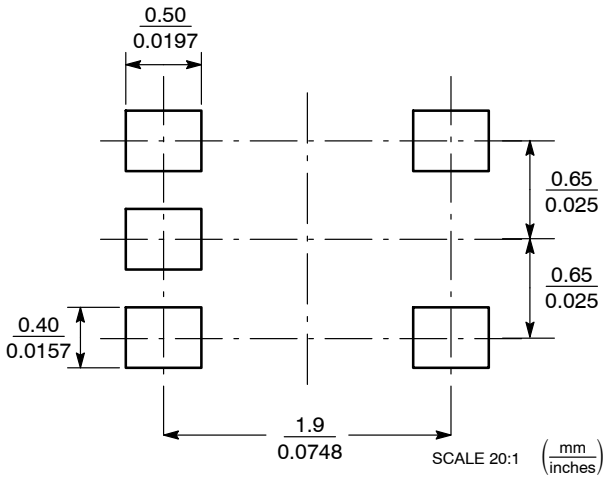
DATE 17 JAN 2013



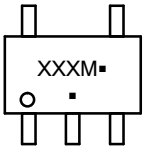
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

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