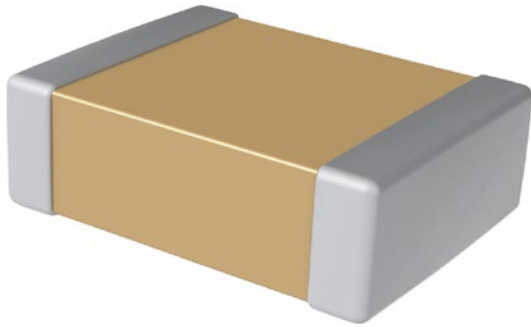


Multilayer Capacitors, SMD

Multilayer Ceramic Capacitors, 1210, X7R



SPECIFICATION:

Construction form	1210
Ceramic type	X7R
Dimensions L x H x W	3.2 x 2.5 x 2.5 mm
Temperature range	-55...+125 °C
Height	2.5 mm
Length	3.2 mm
Width	2.5 mm

PRODUCT RANGE:

Art. Nr.	Capacitance	Rated voltage	Capacitance tolerance
RND 150-1210B103K102N2	10 nF	1000 VDC	±10%
RND 150-1210B103K501N3	10 nF	500 VDC	±10%
RND 150-1210B104K201N3	100 nF	200 VDC	±10%
RND 150-1210B104K500N2	100 nF	50 VDC	±10%
RND 150-1210B105K101N1	1.0 µF	100 VDC	±10%
RND 150-1210B105K500N3	1.0 µF	50 VDC	±10%
RND 150-1210B106K250N1	10 µF	25 VDC	±10%
RND 150-1210B152K102N2	1.5 nF	1000 VDC	±10%
RND 150-1210B222K102N2	2.2 nF	1000 VDC	±10%
RND 150-1210B223K501N2	22 nF	500 VDC	±10%
RND 150-1210B224K101N2	220 nF	100 VDC	±10%
RND 150-1210B224K201N2	220 nF	200 VDC	±10%
RND 150-1210B225K100N2	2.2 µF	10 VDC	±10%
RND 150-1210B334K201N2	330 nF	200 VDC	±10%
RND 150-1210B473K201N2	47 nF	200 VDC	±10%
RND 150-1210B473K631N2	47 nF	630 VDC	±10%
RND 150-1210B474K101N1	470 nF	100 VDC	±10%
RND 150-1210B474K251N1	470 nF	250 VDC	±10%
RND 150-1210B474K500N2	470 nF	50 VDC	±10%
RND 150-1210B475K500N1	4.7 µF	50 VDC	±10%

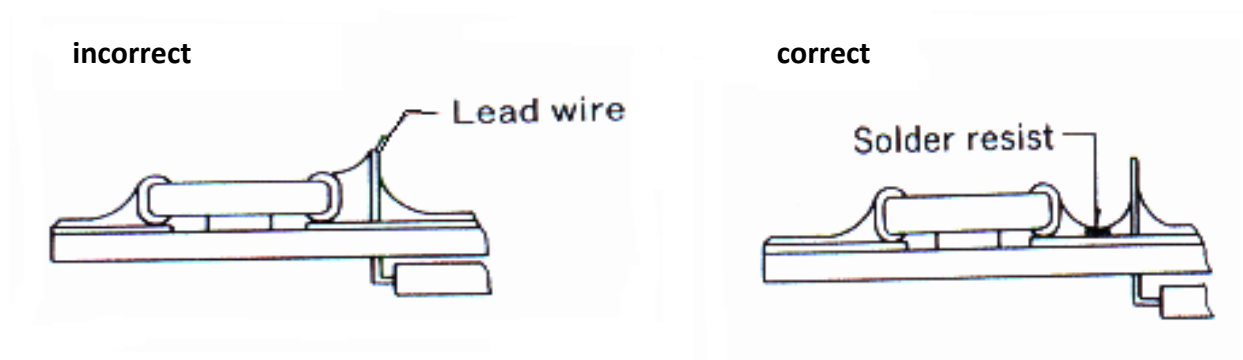
PCB design

Chip components are susceptible to board stress since the component itself is mounted directly on the board. They are also sensitive to mechanical and thermal stress when solder, which may cause chip cracked.

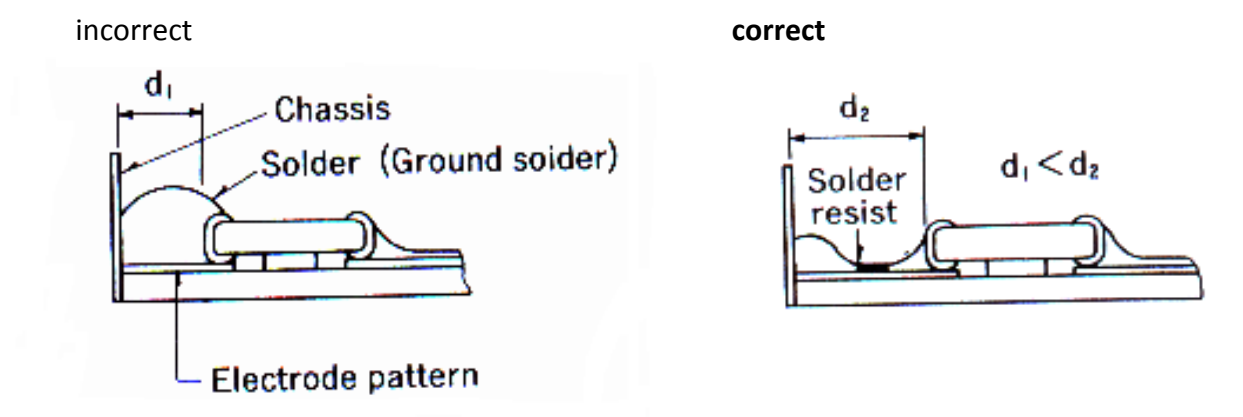
Please take solder form and component layout into consideration to eliminate stress.

Pattern form

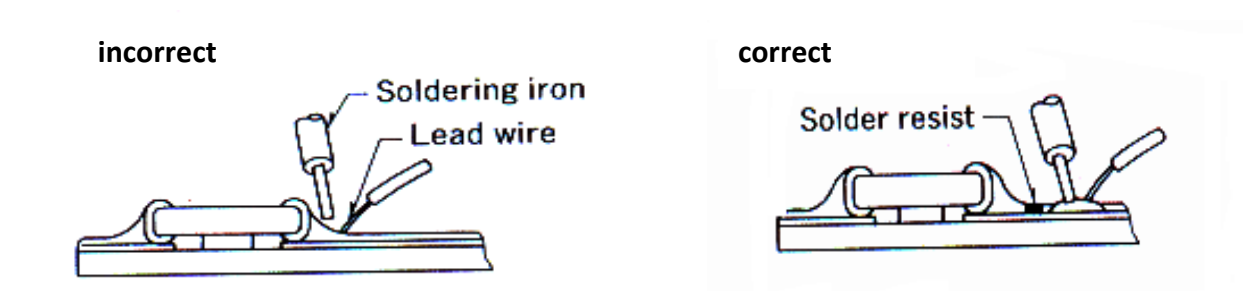
(1) Placing of chip components and component.



(2) Placing close to chassis.

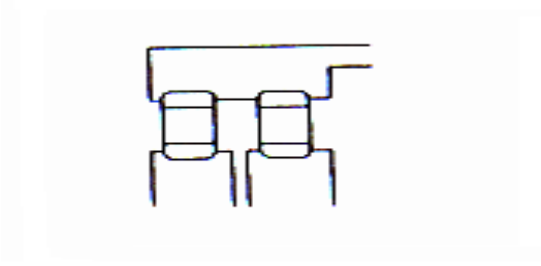


(3) Placing leaded components after chip component.

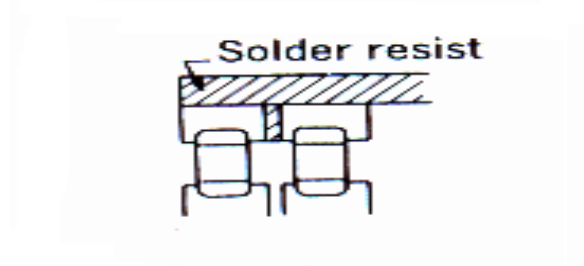


(4) Lateral mounting

incorrect



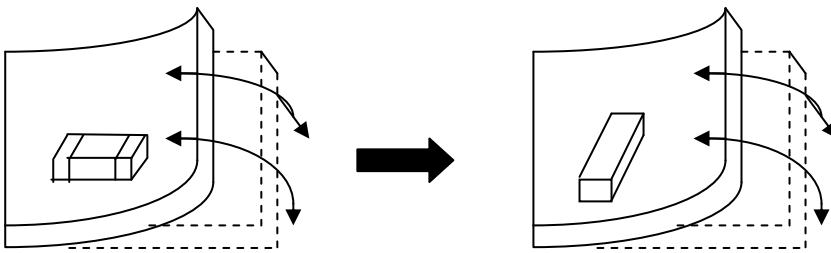
correct



Component direction

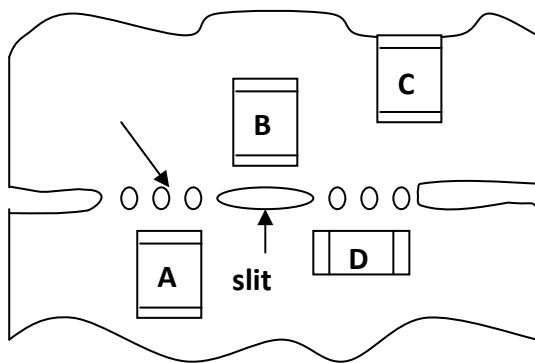
To design a mounting position that minimizes the stress imposed on the chip during flexing or bending of the board.

(1) put the component lateral to the direction in which stress acts.



(2) Component layout close to board separation point.

Susceptibility to stress in the order: $A > C > B = D$



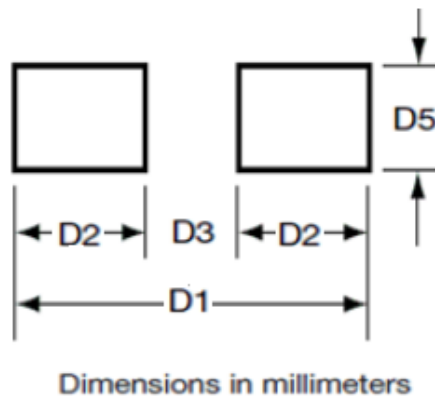
12.3. Land Pattern

When capacitors are mounted on P.C. board, the amount of solder directly affect the performance of capacitors. Therefore, the following items should be carefully considered in the design of solder land pattern.

(1) The greater the amount of solder, the higher the stress on the chip capacitors, and lead to cracking and breaking likely. It is necessary the appropriate size and configuration of the solder pads should be designed to have proper amount of solder on the termination.

(2) When two or more capacitors are soldered together onto the same land or pad, the pad must be designed so that each capacitor's soldering point is separated by solder-resist.

The following diagram and table for recommended pad dimensions.



Type	0201	0402	0603	0805	1206	1210	1808	1812	1825	2220	2225
D1	0.65	1.50	2.30	2.80	4.00	4.00	5.40	5.30	5.30	7.00	7.00
D2	0.21	0.50	0.80	0.90	0.90	0.90	1.05	0.90	0.90	1.35	1.35
D3	0.23	0.50	0.70	1.00	2.20	2.20	3.30	3.50	3.50	4.30	4.30
D5	0.30	0.50	0.80	1.30	1.60	2.50	2.30	3.80	6.50	5.00	6.50

Unit: mm