# ISO776x High-speed, robust EMC, reinforced six-channel digital isolators

## 1 Features

- 100 Mbps data rate
- Robust isolation barrier:
  - >100-Year projected lifetime
  - Up to 5000 $V_{RMS}$ isolation rating
  - Up to 12.8 kV surge capability
  - ±100 kV/µs Typical CMTI
- Wide supply range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level translation
- Default output *high* (ISO776x) and *low* (ISO776xF) Options
- Wide temperature range: –55°C to +125°C
- Low power consumption, typical 1.4 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical at 5 V
- Robust Electromagnetic Compatibility (EMC):
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 Contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16) and SSOP (DBQ-16) package options
- Automotive version available: *ISO776x-Q1*
- Safety-related certifications:
  - Reinforced insulation per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - CSA Certification per IEC 62368-1 and IEC 60601-1
  - CQC Certification per GB4943.1
  - TUV Certification according to EN 62368-1 and EN 61010-1

## 2 Applications

- Industrial automation
- Motor control
- Power supplies
- Solar inverters
- Medical equipment

## 3 Description

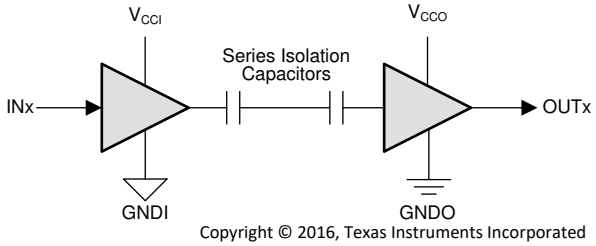
The ISO776x devices are high-performance, six-channel digital isolators with 5000-$V_{RMS}$ (DW package) and 3000-$V_{RMS}$ (DBQ package) isolation ratings per UL 1577. This family of devices is also certified according to VDE, CSA, TUV and CQC.

The ISO776x family of devices provides high-electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a double capacitive silicon dioxide ($SiO_2$) insulation barrier. The ISO776x family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. If the input power or signal is lost, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See the *Device Functional Modes* section for further details.

Used in conjunction with isolated power supplies, this family of devices helps prevent noise currents on data buses, such as RS-485, RS-232, and CAN , or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO776x family of devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO776x family of devices is available in 16-pin SOIC and SSOP packages.

**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ISO7760<br>ISO7761<br>ISO7762<br>ISO7763 | SOIC (16) | 10.30 mm × 7.50 mm |
| | SSOP (16) | 4.90 mm × 3.90 mm |





$V_{CCI}$=Input $V_{CC}$, $V_{CCO}$=Output $V_{CC}$
GNDI=Input ground, GNDO=Output ground

**Simplified Schematic**

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## 4 Revision History

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| Changes from Revision F (November 2022) to Revision G (June 2023) | Page |
|---|---|
| • Changed standard name From: "DIN V VDE V 0884-11:2017-01" To: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document | 1 |
| • Removed references to standard IEC/EN/CSA 60950-1 throughout the document | 1 |
| • Removed standard revision and year references from all standard names throughout the document | 1 |
| • Added Maximum impulse voltage ($V_{IMP}$) per DIN EN IEC 60747-17 (VDE 0884-17) | 10 |
| • Changed test conditions and values of Maximum surge isolation voltage ($V_{IOSM}$) specification per DIN EN IEC 60747-17 (VDE 0884-17) | 10 |
| • Clarified method b test conditions of Apparent charge ($q_{PD}$) | 10 |
| • Changed maximum working voltage value From: 250 $V_{RMS}$ To: 400 $V_{RMS}$ for DBQ-16 devices per GB 4943.1 | 12 |
| • Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDB from: 135 years to: 169 years per DIN EN IEC 60747-17 (VDE 0884-17) | 33 |
| • Changed Figure 9-7 per DIN EN IEC 60747-17 (VDE 0884-17) | 33 |

| Changes from Revision E (February 2019) to Revision F (November 2022) | Page |
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| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |

| Changes from Revision D (November 2018) to Revision E (February 2019) | Page |
|---|---|
| • Changed CPG parameter description from "External clearance" to "External creepage" | 10 |

| Changes from Revision C (January 2018) to Revision D (November 2018) | Page |
|---|---|
| • Made editorial and cosmetic changes throughout the document | 1 |
| • Changed From: "Isolation Barrier Life: >40 Years" To:">100-Year Projected Lifetime" in Section 1 | 1 |
| • Added "Up to 5000 $V_{RMS}$ Isolation Rating" in Section 1 | 1 |

- Added "Up to 12.8 kV Surge Capability" in Section 1 ..... 1
- Added "±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier" in Section 1 .....1
- Added "Automotive Version Available: ISO776x-Q1" in Section 1 ..... 1
- Deleted "Certification Planned" statement throughout the document .....1
- Updated Section 2 list.....1
- Changed Figure 3-1 to show series isolation capacitors.....1
- Added table note to Data rate specification.....8
- Changed $V_{IORM}$ value for DW-16 package from "1414 $V_{PK}$" to "2121 $V_{PK}$ ..... 10
- Changed $V_{IOWM}$ values for DW-16 package from "1000 $V_{RMS}$" and "1414 $V_{DC}$" to "1500 $V_{RMS}$" and "2121 $V_{DC}$".....10
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- Changed From: "*Table 2*" To: "*Safety Related Certifications*" in Table 8-1 table note.....28
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- Changed the $C_{IO}$ value for the DBQ package from 1.1 to 0.9 pF.....10

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- Changed the CSA certification wording in the *Features* and *Safety-Related Certifications* table..... 1
- Changed the isolation voltage for the DBQ-16 package from 2500 to 3000 $V_{RMS}$ .....1
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- Deleted EN from the *Common-Mode Transient Immunity Test Circuit* figure.....26
- Changed the $V_{CC1}$ and $V_{CC2}$ signals in the *Typical ISO7761 Circuit Hook-up* figure.....31

## 5 Pin Configuration and Functions

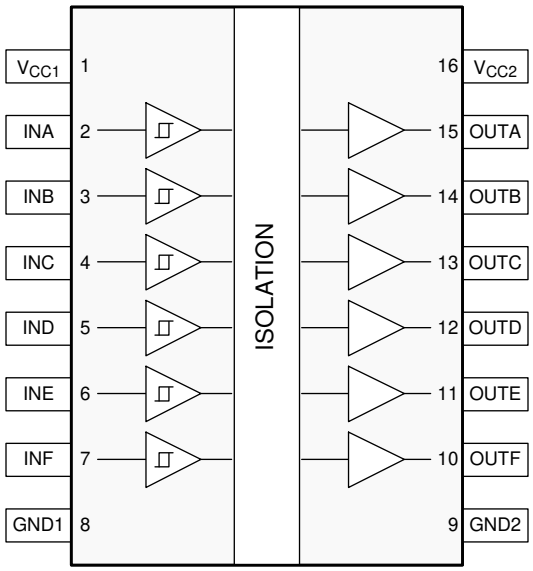



**Figure 5-1. ISO7760 DW and DBQ Packages 16-Pin SOIC and SSOP Top View**

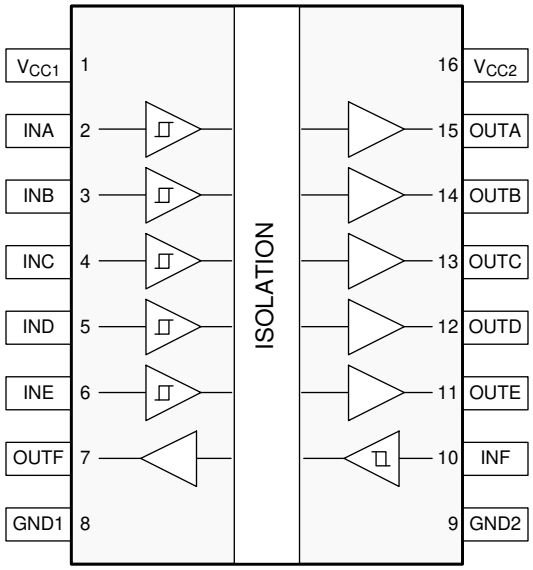



**Figure 5-2. ISO7761 DW and DBQ Packages 16-Pin SOIC and SSOP Top View**

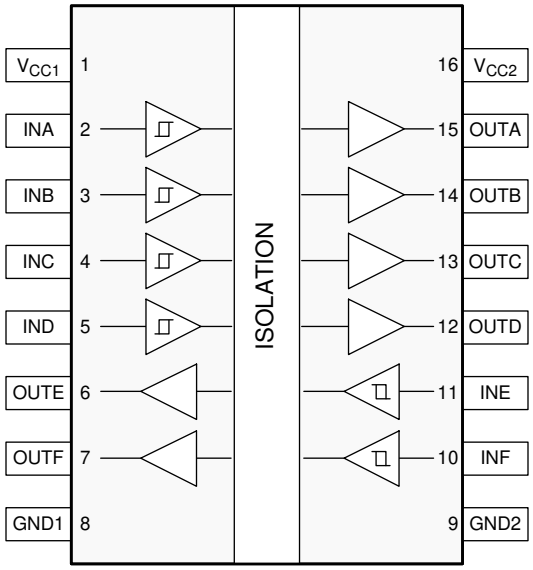



**Figure 5-3. ISO7762 DW and DBQ Packages 16-Pin SOIC and SSOP Top View**

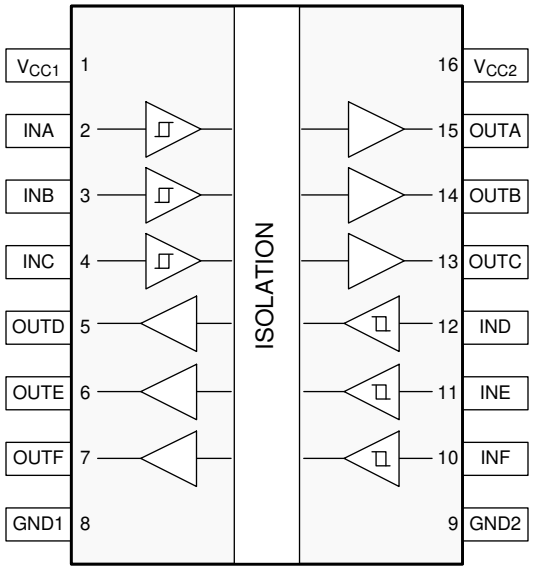



**Figure 5-4. ISO7763 DW and DBQ Packages 16-Pin SOIC and SSOP Top View**

**Table 5-1. Pin Functions**

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | NO. | | | | | |
| | ISO7760 | ISO7761 | ISO7762 | ISO7763 | | |
| GND1 | 8 | 8 | 8 | 8 | — | Ground connection for $V_{CC1}$ |
| GND2 | 9 | 9 | 9 | 9 | — | Ground connection for $V_{CC2}$ |
| INA | 2 | 2 | 2 | 2 | I | Input, channel A |
| INB | 3 | 3 | 3 | 3 | I | Input, channel B |
| INC | 4 | 4 | 4 | 4 | I | Input, channel C |
| IND | 5 | 5 | 5 | 12 | I | Input, channel D |
| INE | 6 | 6 | 11 | 11 | I | Input, channel E |
| INF | 7 | 10 | 10 | 10 | I | Input, channel F |
| OUTA | 15 | 15 | 15 | 15 | O | Output, channel A |
| OUTB | 14 | 14 | 14 | 14 | O | Output, channel B |
| OUTC | 13 | 13 | 13 | 13 | O | Output, channel C |
| OUTD | 12 | 12 | 12 | 5 | O | Output, channel D |
| OUTE | 11 | 11 | 6 | 6 | O | Output, channel E |
| OUTF | 10 | 7 | 7 | 7 | O | Output, channel F |
| $V_{CC1}$ | 1 | 1 | 1 | 1 | — | Power supply, side 1 |
| $V_{CC2}$ | 16 | 16 | 16 | 16 | — | Power supply, side 2 |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

See(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage (2) | -0.5 | 6 | V |
| V | Voltage at INx, OUTx | -0.5 | $V_{CCX}$ + 0.5 (3) | V |
| $I_o$ | Output current | -15 | 15 | mA |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

## 6.2 ESD Ratings

(1) (2)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±6000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |
| | | Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4) | ±8000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage | | 2.25 | | 5.5 | V |
| $V_{cc\ (UVLO+)}$ | UVLO threshold when supply voltage is rising | | | 2 | 2.25 | V |
| $V_{cc\ (UVLO-)}$ | UVLO threshold when supply voltage is falling | | 1.7 | 1.8 | | V |
| $V_{HYS\ (UVLO)}$ | Supply voltage UVLO hysteresis | | 100 | 200 | | mV |
| $I_{OH}$ | High level output current | $V_{CCO}$ (1) = 5 V | -4 | | | mA |
| | | $V_{CCO}$ = 3.3 V | -2 | | | |
| | | $V_{CCO}$ = 2.5 V | -1 | | | |
| $I_{OL}$ | Low level output current | $V_{CCO}$ = 5 V | | | 4 | mA |
| | | $V_{CCO}$ = 3.3 V | | | 2 | |
| | | $V_{CCO}$ = 2.5 V | | | 1 | |
| $V_{IH}$ | High level Input voltage | | 0.7 x $V_{CCI}$ (1) | | $V_{CCI}$ | V |
| $V_{IL}$ | Low level Input voltage | | 0 | | 0.3 x $V_{CCI}$ | V |
| DR(2) | Data Rate | | 0 | | 100 | Mbps |
| $T_A$ | Ambient temperature | | -55 | 25 | 125 | °C |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

## 6.4 Thermal Information

| THERMAL METRIC (1) | | ISO776x | | UNIT |
|---|---|---|---|---|
| | | DW (SOIC) | DBQ (SSOP) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.3 | 86.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 24.0 | 26.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 29.3 | 36.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.3 | 1.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 28.7 | 36.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7760** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 292 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 50 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 242 | mW |
| **ISO7761** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 292 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 83 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 209 | mW |
| **ISO7762** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 292 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 116 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 176 | mW |
| **ISO7763** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 292 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 146 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 146 | mW |

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | | VALUE | | UNIT |
|---|---|---|---|---|---|---|
| | | | | DW-16 | DBQ-16 | |
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | | >8 | >3.7 | mm |
| CPG | External creepage(1) | Shortest terminal-to-terminal distance across the package surface | | >8 | >3.7 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | | >21 | >21 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A | | >600 | >600 | V |
| | Material group | According to IEC 60664-1 | | I | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 150 $V_{RMS}$ | | I-IV | I-IV | |
| | | Rated mains voltage ≤ 300 $V_{RMS}$ | | I-IV | I-III | |
| | | Rated mains voltage ≤ 600 $V_{RMS}$ | | I-IV | n/a | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | | I-III | n/a | |
| **DIN EN IEC 60747-17 (VDE 0884-17)(2)** | | | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | | 2121 | 566 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum working isolation voltage | AC voltage; Time dependent dielectric breakdown (TDDB) test; See Figure 9-7 | | 1500 | 400 | $V_{RMS}$ |
| | | DC voltage | | 2121 | 566 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production) | ISO7760 | 8000 | 4242 | $V_{PK}$ |
| | | | ISO7761, ISO7762, ISO7763 | 7071 | | |
| $V_{IMP}$ | Maximum impulse voltage(3) | Tested in air, 1.2/50-µs waveform per IEC 62368-1 | | 8000 | 4000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(4) | $V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1 | | 12800 | 10000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(5) | Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m$ = 10 s | | ≤5 | ≤5 | pC |
| | | Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m$ = 10 s | | ≤5 | ≤5 | |
| | | Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m$ = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2) | | ≤5 | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output(6) | $V_{IO}$ = 0.4 x sin (2πft), f = 1 MHz | | ~1.1 | ~0.9 | pF |
| $R_{IO}$ | Isolation resistance(6) | $V_{IO}$ = 500 V, $T_A$ = 25°C | | $>10^{12}$ | $>10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | | $>10^{11}$ | $>10^{11}$ | |
| | | $V_{IO}$ = 500 V, $T_S$ = 150°C | | $>10^{9}$ | $>10^{9}$ | |
| | Pollution degree | | | 2 | 2 | |
| | Climatic category | | | 55/125/21 | 55/125/21 | |
| **UL 1577** | | | | | | |
| $V_{ISO}$ | Maximum withstanding isolation voltage | $V_{TEST} = V_{ISO}$ , t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1 s (100% production) | | 5000 | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to IEC 62368-1 and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB 4943.1 | Certified according to EN 61010-1 and EN 62368-1 |
| Reinforced Insulation; Maximum transient isolation voltage, 8000 $V_{PK}$ (ISO7760 in DW-16), 7071 $V_{PK}$ (ISO7761, ISO7762, ISO7763 in DW-16) and 4242 $V_{PK}$ (DBQ-16); Maximum repetitive peak isolation voltage, 2121 $V_{PK}$ (DW-16) and 566 $V_{PK}$ (DBQ-16); Maximum surge isolation voltage, 12800 $V_{PK}$ (DW-16) and 10000 $V_{PK}$ (DBQ-16) | Reinforced insulation per CSA 62368-1 and IEC 62368-1 800 $V_{RMS}$ (DW-16) and 370 $V_{RMS}$ (DBQ-16) maximum working voltage (pollution degree 2, material group I); DW-16: 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 $V_{RMS}$ maximum working voltage | DW-16: Single protection, 5000 $V_{RMS}$ ; DBQ-16: Single protection, 3000 $V_{RMS}$ | DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 $V_{RMS}$ maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 $V_{RMS}$ maximum working voltage | 5000 $V_{RMS}$ Reinforced insulation per EN 61010-1 up to working voltage of 600 $V_{RMS}$ (DW-16) and 300 $V_{RMS}$ (DBQ-16) 5000 $V_{RMS}$ Reinforced insulation per EN 62368-1 up to working voltage of 800 $V_{RMS}$ (DW-16) and 370 $V_{RMS}$ (DBQ-16) |
| Certificate number: 40040142 | Master contract number: 220991 | File number: E181974 | Certificate numbers: CQC15001121716 (DW) CQC18001199097 (DBQ) | Client ID number: 77311 |

## 6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DW-16 PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 60.3°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 377 | mA |
| | | $R_{\theta JA}$ = 60.3°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 576 | |
| | | $R_{\theta JA}$ = 60.3°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 754 | |
| $P_S$ | Safety input, output, or total power (1) | $R_{\theta JA}$ = 60.3°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-3 | | | 2073 | mW |
| $T_S$ | Maximum safety temperature (1) | | | | 150 | °C |
| **DBQ-16 PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 86.5°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 263 | mA |
| | | $R_{\theta JA}$ = 86.5°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 401 | |
| | | $R_{\theta JA}$ = 86.5°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 525 | |
| $P_S$ | Safety input, output, or total power (1) | $R_{\theta JA}$ = 86.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-4 | | | 1445 | mW |
| $T_S$ | Maximum safety temperature (1) | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

## 6.9 Electrical Characteristics—5-V Supply

VCC1 = VCC2 = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -4 mA; See Figure 7-1 | $V_{CCO}$ (1) - 0.4 | 4.8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; See Figure 7-1 | | 0.2 | 0.4 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CCI}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-3 | 85 | 100 | | kV/µs |
| $C_I$ | Input Capacitance (2) | $V_I$ = $V_{CC}$/ 2 + 0.4 × sin(2πft), f = 1 MHz, $V_{CC}$ = 5 V | | 2 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 6.10 Supply Current Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7760** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CC1}$ (ISO7760); $V_I$ = 0 V (ISO7760 with F suffix) | | $I_{CC1}$ | | 1.6 | 2.3 | mA |
| | | | $I_{CC2}$ | | 3 | 4.9 | |
| | $V_I$ = 0 V (ISO7760); $V_I$ = $V_{CC1}$ (ISO7760 with F suffix) | | $I_{CC1}$ | | 8 | 11.3 | |
| | | | $I_{CC2}$ | | 3.3 | 5.3 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 5 | 6.4 | |
| | | | $I_{CC2}$ | | 3.5 | 5.6 | |
| | | 10 Mbps | $I_{CC1}$ | | 5.2 | 6.7 | |
| | | | $I_{CC2}$ | | 6.4 | 9 | |
| | | 100 Mbps | $I_{CC1}$ | | 7 | 9 | |
| | | | $I_{CC2}$ | | 35 | 44 | |
| **ISO7761** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO7761); $V_I$ = 0 V (ISO7761 with F suffix) | | $I_{CC1}$ | | 1.9 | 2.7 | mA |
| | | | $I_{CC2}$ | | 2.9 | 4.7 | |
| | $V_I$ = 0 V (ISO7761); $V_I$ = $V_{CCI}$ (ISO7761 with F suffix) | | $I_{CC1}$ | | 7.3 | 10.6 | |
| | | | $I_{CC2}$ | | 4.2 | 6.6 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.7 | 6.4 | |
| | | | $I_{CC2}$ | | 3.8 | 5.9 | |
| | | 10 Mbps | $I_{CC1}$ | | 5.3 | 7.2 | |
| | | | $I_{CC2}$ | | 6.3 | 8.8 | |
| | | 100 Mbps | $I_{CC1}$ | | 11.5 | 15 | |
| | | | $I_{CC2}$ | | 30.5 | 38 | |
| **ISO7762** | | | | | | | |

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7762); $V_I$ = 0 V (ISO7762 with F suffix) | | $I_{CC1}$ | | 2.1 | 3.2 | mA |
| | | | $I_{CC2}$ | | 2.6 | 4.2 | |
| | $V_I$ = 0 V (ISO7762); $V_I$ = $V_{CCI}$ (ISO7762 with F suffix) | | $I_{CC1}$ | | 6.5 | 9.3 | |
| | | | $I_{CC2}$ | | 5 | 7.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.5 | 6.3 | |
| | | | $I_{CC2}$ | | 4 | 6.1 | |
| | | 10 Mbps | $I_{CC1}$ | | 5.6 | 7.6 | |
| | | | $I_{CC2}$ | | 6 | 8.4 | |
| | | 100 Mbps | $I_{CC1}$ | | 16.5 | 21 | |
| | | | $I_{CC2}$ | | 25.7 | 32 | |
| **ISO7763** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7763); $V_I$ = 0 V (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.4 | 3.7 | mA |
| | $V_I$ = 0 V (ISO7763); $V_I$ = $V_{CCI}$ (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 5.7 | 8.6 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.2 | 6.1 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 5.8 | 8 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 21 | 26.5 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -2mA ; See Figure 7-1 | $V_{CCO}$ (1) - 0.3 | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2mA ; See Figure 7-1 | | 0.1 | 0.3 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-3 | 85 | 100 | | kV/us |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$

## 6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7760** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CC1}$ (ISO7760); $V_I$ = 0 V (ISO7760 with F suffix) | | $I_{CC1}$ | | 1.6 | 2.2 | mA |
| | | | $I_{CC2}$ | | 3 | 4.8 | |
| | $V_I$ = 0 V (ISO7760); $V_I$ = $V_{CC1}$ (ISO7760 with F suffix) | | $I_{CC1}$ | | 8 | 11.4 | |
| | | | $I_{CC2}$ | | 3.3 | 5.3 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.9 | 6.6 | |
| | | | $I_{CC2}$ | | 3.4 | 5.3 | |
| | | 10 Mbps | $I_{CC1}$ | | 5 | 6.7 | |
| | | | $I_{CC2}$ | | 5.5 | 7.8 | |
| | | 100 Mbps | $I_{CC1}$ | | 6.3 | 8.2 | |
| | | | $I_{CC2}$ | | 26 | 33 | |
| **ISO7761** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO7761); $V_I$ = 0 V (ISO7761 with F suffix) | | $I_{CC1}$ | | 1.8 | 2.7 | mA |
| | | | $I_{CC2}$ | | 2.9 | 4.7 | |
| | $V_I$ = 0 V (ISO7761); $V_I$ = $V_{CCI}$ (ISO7761 with F suffix) | | $I_{CC1}$ | | 7.2 | 10.3 | |
| | | | $I_{CC2}$ | | 4.2 | 6.6 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.6 | 6.5 | |
| | | | $I_{CC2}$ | | 3.7 | 5.7 | |
| | | 10 Mbps | $I_{CC1}$ | | 5.1 | 7 | |
| | | | $I_{CC2}$ | | 5.5 | 7.8 | |
| | | 100 Mbps | $I_{CC1}$ | | 9.4 | 12 | |
| | | | $I_{CC2}$ | | 22.8 | 29 | |
| **ISO7762** | | | | | | | |

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7762); $V_I$ = 0 V (ISO7762 with F suffix) | | $I_{CC1}$ | | 2.1 | 3.2 | mA |
| | | | $I_{CC2}$ | | 2.5 | 4.2 | |
| | $V_I$ = 0 V (ISO7762); $V_I$ = $V_{CCI}$ (ISO7762 with F suffix) | | $I_{CC1}$ | | 6.5 | 9.4 | |
| | | | $I_{CC2}$ | | 5 | 7.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.4 | 6.2 | |
| | | | $I_{CC2}$ | | 3.9 | 5.8 | |
| | | 10 Mbps | $I_{CC1}$ | | 5.2 | 7.1 | |
| | | | $I_{CC2}$ | | 5.4 | 7.5 | |
| | | 100 Mbps | $I_{CC1}$ | | 12.9 | 16.5 | |
| | | | $I_{CC2}$ | | 19.5 | 25 | |
| **ISO7763** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7763); $V_I$ = 0 V (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.4 | 3.7 | mA |
| | $V_I$ = 0 V (ISO7763); $V_I$ = $V_{CCI}$ (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 5.7 | 8.4 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.2 | 6.2 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 5.2 | 7.5 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 16 | 20.5 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -1mA ; See Figure 7-1 | $V_{CCO}$ (1) - 0.2 | 2.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1mA ; See Figure 7-1 | | 0.05 | 0.2 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-3 | 85 | 100 | | kV/us |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$

## 6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7760** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CC1}$ (ISO7760); $V_I$ = 0 V (ISO7760 with F suffix) | | $I_{CC1}$ | | 1.6 | 2.2 | mA |
| | | | $I_{CC2}$ | | 3 | 4.8 | |
| | $V_I$ = 0 V (ISO7760); $V_I$ = $V_{CC1}$ (ISO7760 with F suffix) | | $I_{CC1}$ | | 8 | 11.6 | |
| | | | $I_{CC2}$ | | 3.3 | 5.3 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.9 | 6.8 | |
| | | | $I_{CC2}$ | | 3.4 | 5.3 | |
| | | 10 Mbps | $I_{CC1}$ | | 5 | 7 | |
| | | | $I_{CC2}$ | | 4.9 | 7.2 | |
| | | 100 Mbps | $I_{CC1}$ | | 6 | 8 | |
| | | | $I_{CC2}$ | | 20.3 | 26 | |
| **ISO7761** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1) (ISO7761); $V_I$ = 0 V (ISO7761 with F suffix) | | $I_{CC1}$ | | 1.8 | 2.7 | mA |
| | | | $I_{CC2}$ | | 2.9 | 4.6 | |
| | $V_I$ = 0 V (ISO7761); $V_I$ = $V_{CCI}$ (ISO7761 with F suffix) | | $I_{CC1}$ | | 7.2 | 10.3 | |
| | | | $I_{CC2}$ | | 4.2 | 6.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.6 | 6.7 | |
| | | | $I_{CC2}$ | | 3.7 | 5.8 | |
| | | 10 Mbps | $I_{CC1}$ | | 4.9 | 7.1 | |
| | | | $I_{CC2}$ | | 5 | 7.3 | |
| | | 100 Mbps | $I_{CC1}$ | | 8.3 | 10.7 | |
| | | | $I_{CC2}$ | | 18.1 | 24 | |
| **ISO7762** | | | | | | | |

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7762); $V_I$ = 0 V (ISO7762 with F suffix) | | $I_{CC1}$ | | 2.1 | 3.2 | mA |
| | | | $I_{CC2}$ | | 2.6 | 4.1 | |
| | $V_I$ = 0 V (ISO7762); $V_I$ = $V_{CCI}$ (ISO7762 with F suffix) | | $I_{CC1}$ | | 6.5 | 9.6 | |
| | | | $I_{CC2}$ | | 4.9 | 7.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 4.4 | 6.4 | |
| | | | $I_{CC2}$ | | 3.9 | 5.8 | |
| | | 10 Mbps | $I_{CC1}$ | | 5 | 7.1 | |
| | | | $I_{CC2}$ | | 5 | 7.1 | |
| | | 100 Mbps | $I_{CC1}$ | | 10.9 | 14.1 | |
| | | | $I_{CC2}$ | | 15.6 | 20.1 | |
| **ISO7763** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (ISO7763); $V_I$ = 0 V (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.3 | 3.7 | mA |
| | $V_I$ = 0 V (ISO7763); $V_I$ = $V_{CCI}$ (ISO7763 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 5.7 | 8.4 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.1 | 6.1 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.9 | 7.1 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 13 | 17 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 6.15 Switching Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO776x** | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 6 | 11 | 16 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 7-1 | | 0.4 | 4.9 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 4.5 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 1.1 | 3.9 | ns |
| $t_f$ | Output signal fall time | See Figure 7-1 | | 1.4 | 3.9 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-2 | | 0.2 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 1.3 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.16 Switching Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO776x** | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 6 | 12 | 16 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 7-1 | | 0.5 | 5 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4.1 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 4.5 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 1 | 3 | ns |
| $t_f$ | Output signal fall time | See Figure 7-1 | | 1 | 3 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-2 | | 0.2 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 1.3 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.17 Switching Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO776x** | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 7.5 | 13 | 18.5 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | 0.6 | 5.1 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4.1 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 4.6 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 1 | 3.5 | ns |
| $t_f$ | Output signal fall time | | | 1 | 3.5 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-2 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 1.3 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.18 Insulation Characteristics Curves

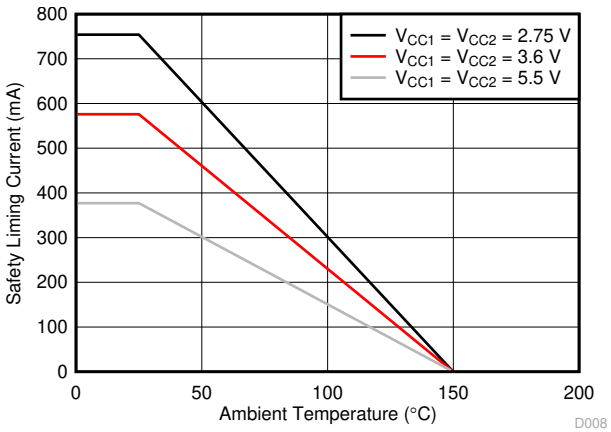



**Figure 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package**

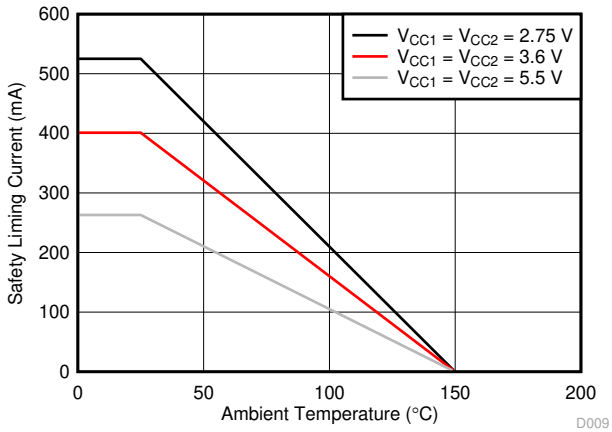



**Figure 6-2. Thermal Derating Curve for Limiting Current per VDE for DBQ-16 Package**

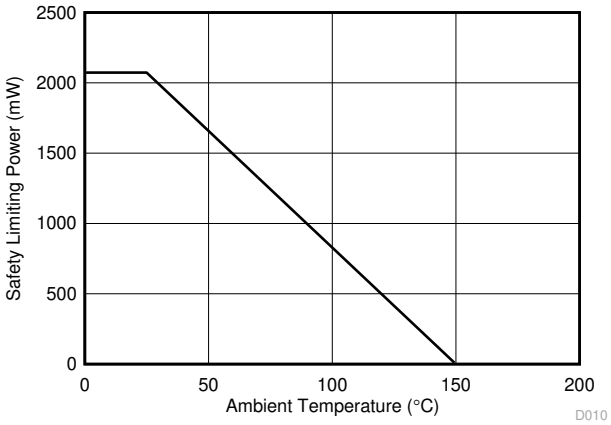



**Figure 6-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package**

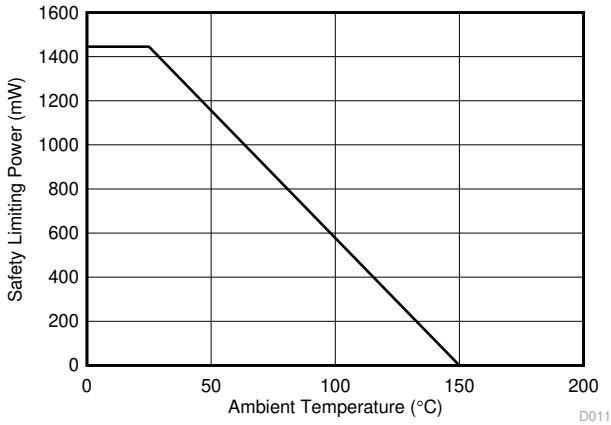
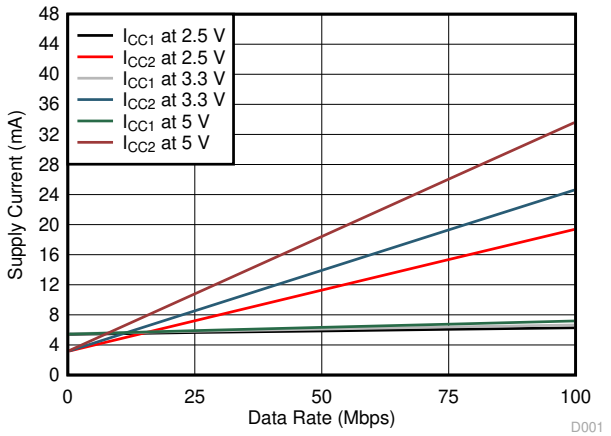


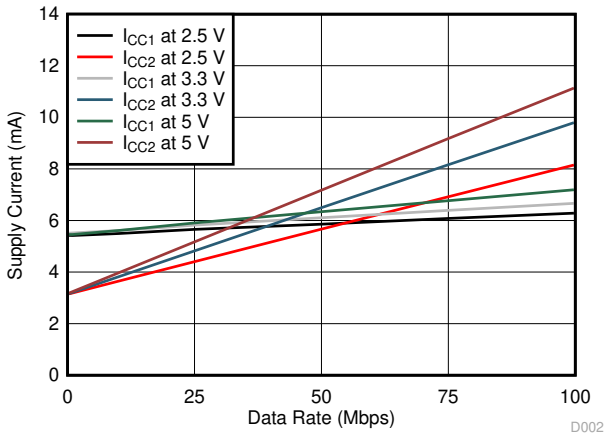

**Figure 6-4. Thermal Derating Curve for Limiting Power per VDE for DBQ-16 Package**

## 6.19 Typical Characteristics



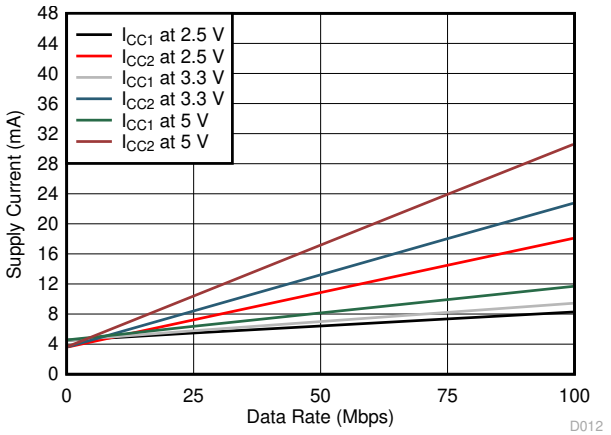

$T_A$ = 25°C $C_L$ = 15 pF

**Figure 6-5. ISO7760 Supply Current vs Data Rate (With 15-pF Load)**



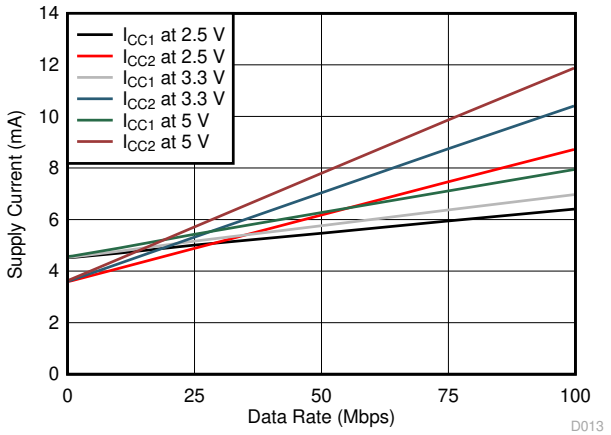

$T_A$ = 25°C $C_L$ = No Load

**Figure 6-6. ISO7760 Supply Current vs Data Rate (With No Load)**



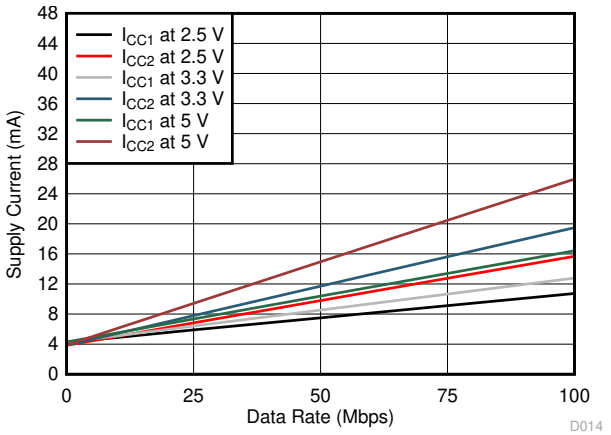

$T_A$ = 25°C $C_L$ = 15 pF

**Figure 6-7. ISO7761 Supply Current vs Data Rate (With 15-pF Load)**



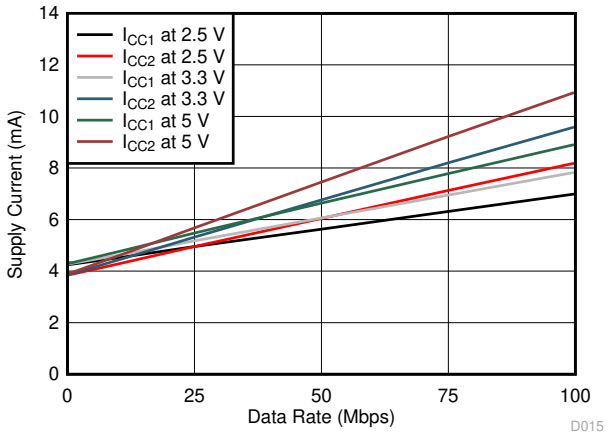

$T_A$ = 25°C $C_L$ = No Load

**Figure 6-8. ISO7761 Supply Current vs Data Rate (With No Load)**



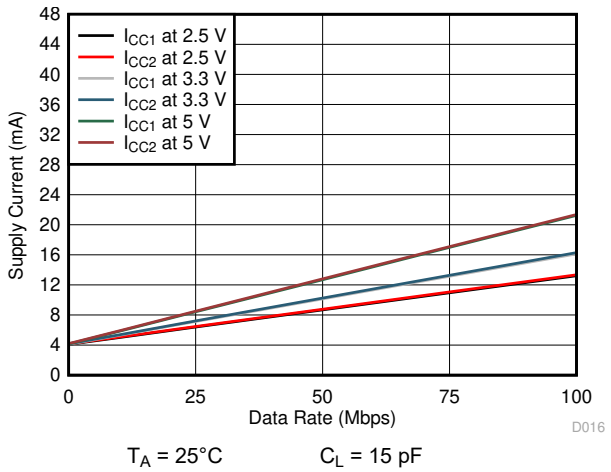

$T_A$ = 25°C $C_L$ = 15 pF

**Figure 6-9. ISO7762 Supply Current vs Data Rate (With 15-pF Load)**



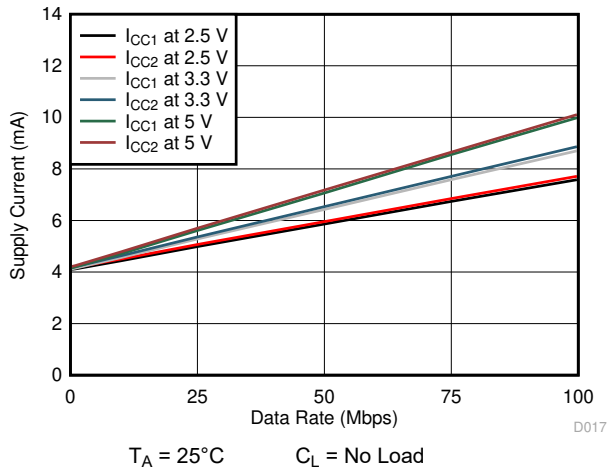

$T_A$ = 25°C $C_L$ = No Load

**Figure 6-10. ISO7762 Supply Current vs Data Rate (With No Load)**



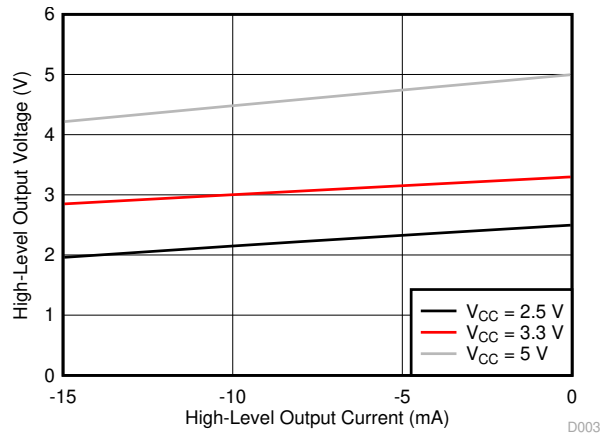

$T_A$ = 25°C $C_L$ = 15 pF

**Figure 6-11. ISO7763 Supply Current vs Data Rate (With 15-pF Load)**



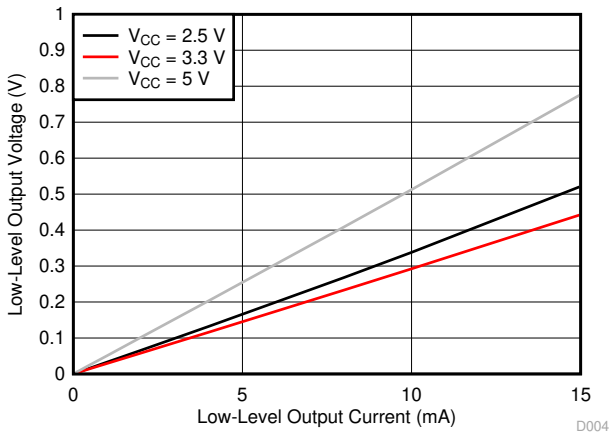

$T_A$ = 25°C $C_L$ = No Load

**Figure 6-12. ISO7763 Supply Current vs Data Rate (With No Load)**




$T_A$ = 25°C

**Figure 6-13. High-Level Output Voltage vs High-Level Output Current**




$T_A$ = 25°C

**Figure 6-14. Low-Level Output Voltage vs Low-Level Output Current**

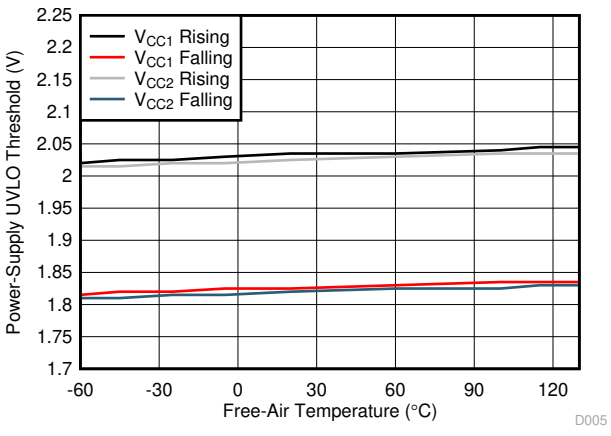



**Figure 6-15. Power Supply Undervoltage Threshold vs Free-Air Temperature**

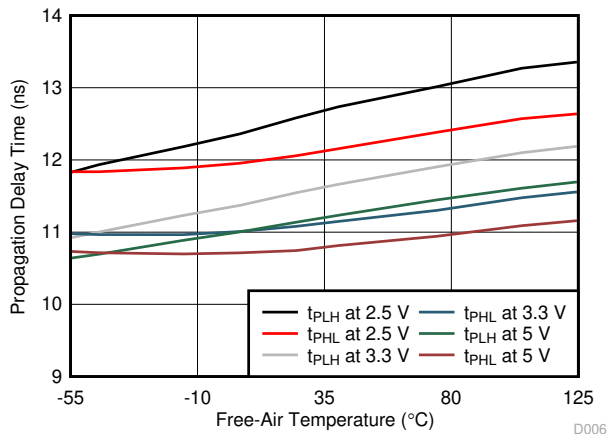
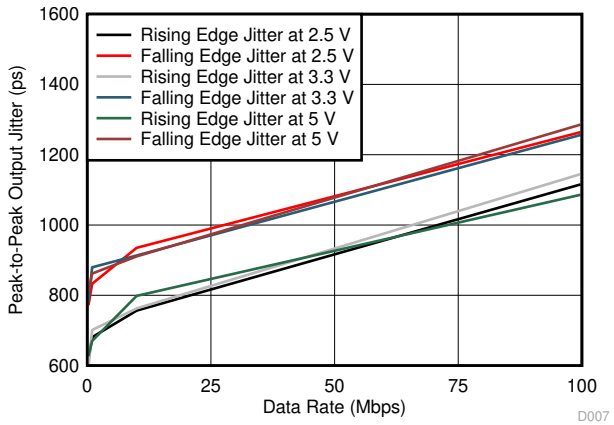


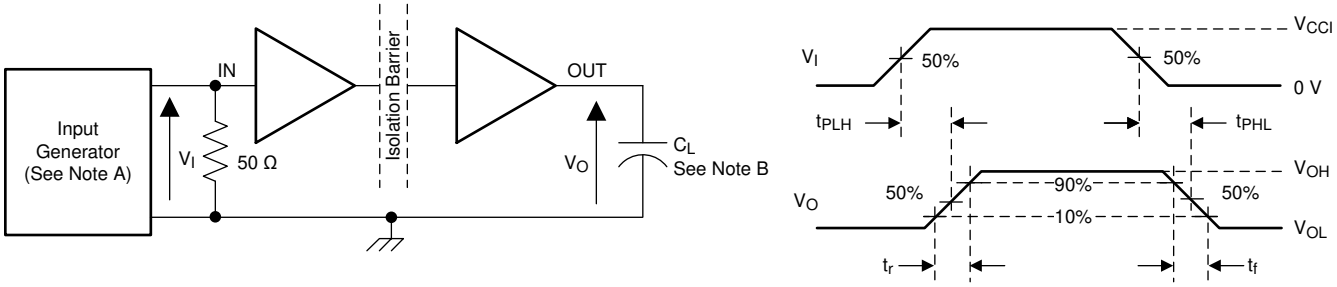

**Figure 6-16. Propagation Delay Time vs Free-Air Temperature**




$T_A$ = 25°C

**Figure 6-17. Peak-to-Peak Output Jitter vs Data Rate**

# 7 Parameter Measurement Information

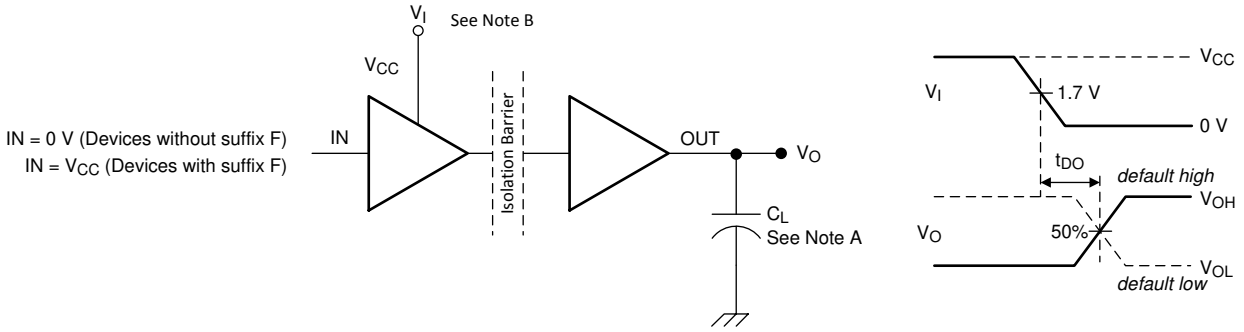





A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω. At the input, a 50-Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

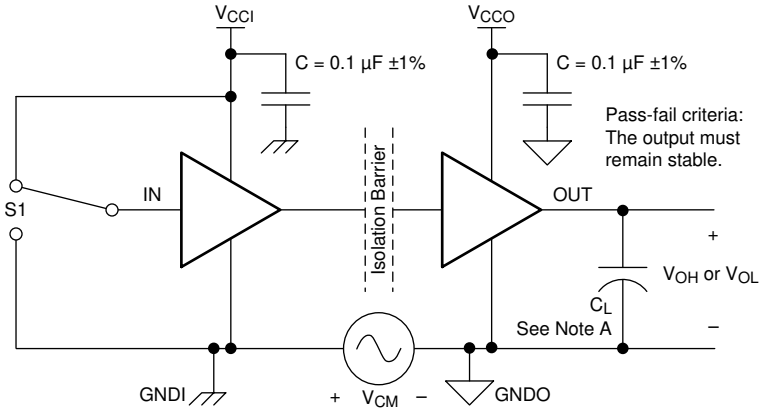
**Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power-supply ramp rate = 10 mV/ns

**Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 7-3. Common-Mode Transient Immunity Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The ISO776x family of devices uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO776x family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 8-1, shows a functional block diagram of a typical channel. Figure 8-2 shows a conceptual detail of how the ON-OFF keying scheme works.

## 8.2 Functional Block Diagram

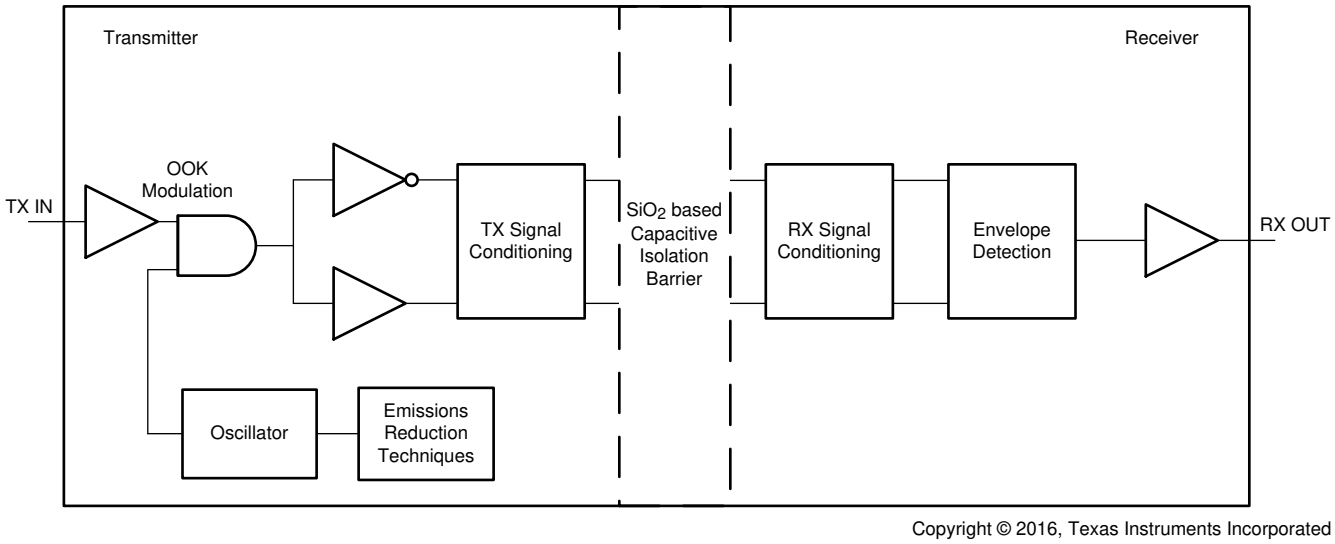





**Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

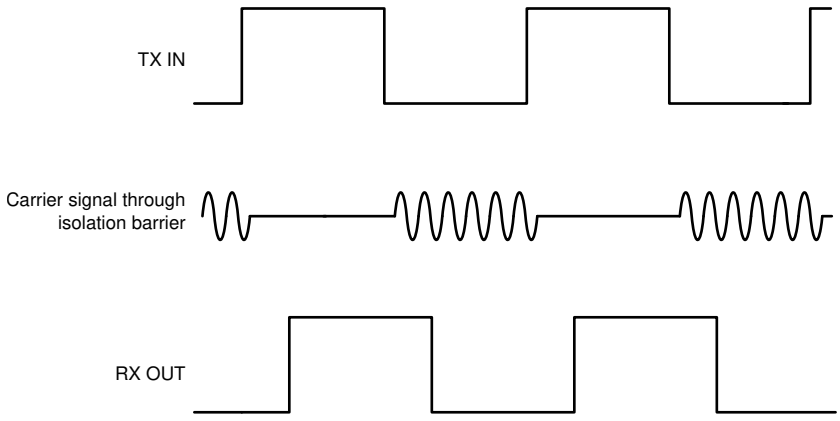



**Figure 8-2. ON-OFF Keying (OOK) Based Modulation Scheme**

## 8.3 Feature Description

Table 8-1 lists the device features.

**Table 8-1. Device Features**

| PART NUMBER | CHANNEL DIRECTION | MAXIMUM DATA RATE | DEFAULT OUTPUT | PACKAGE | RATED ISOLATION(1) |
|---|---|---|---|---|---|
| ISO7760 | 6 Forward, 0 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7760 with F suffix | 6 Forward, 0 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7761 | 5 Forward, 1 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7761 with F suffix | 5 Forward, 1 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7762 | 4 Forward, 2 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7762 with F suffix | 4 Forward, 2 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7763 | 3 Forward, 3 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7763 with F suffix | 3 Forward, 3 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 7071 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |

(1) See Section 6.7 for detailed isolation ratings.

### 8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO776x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

## 8.4 Device Functional Modes

Table 8-2 lists the functional modes for the ISO776x.

**Table 8-2. Function Table**

| $V_{CCI}$ | $V_{CCO}$ | INPUT (INx)(2) | OUTPUT (OUTx) | COMMENTS |
|---|---|---|---|---|
| PU | PU | H | H | Normal Operation:<br>A channel output assumes the logic state of the input. |
| | | L | L | |
| | | Open | Default | Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO776x and *Low* for ISO776x with F suffix. |
| PD | PU | X | Default | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO776x and *Low* for ISO776x with F suffix.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of its input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| X | PD | X | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined (1).<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input |

(1) The outputs are in undetermined state when 1.7 V < $V_{CCI}$, $V_{CCO}$ < 2.25 V.
(2) A strongly driven input signal can weakly power the floating $V_{CC}$ via an internal protection diode and cause undetermined output.

### 8.4.1 Device I/O Schematics

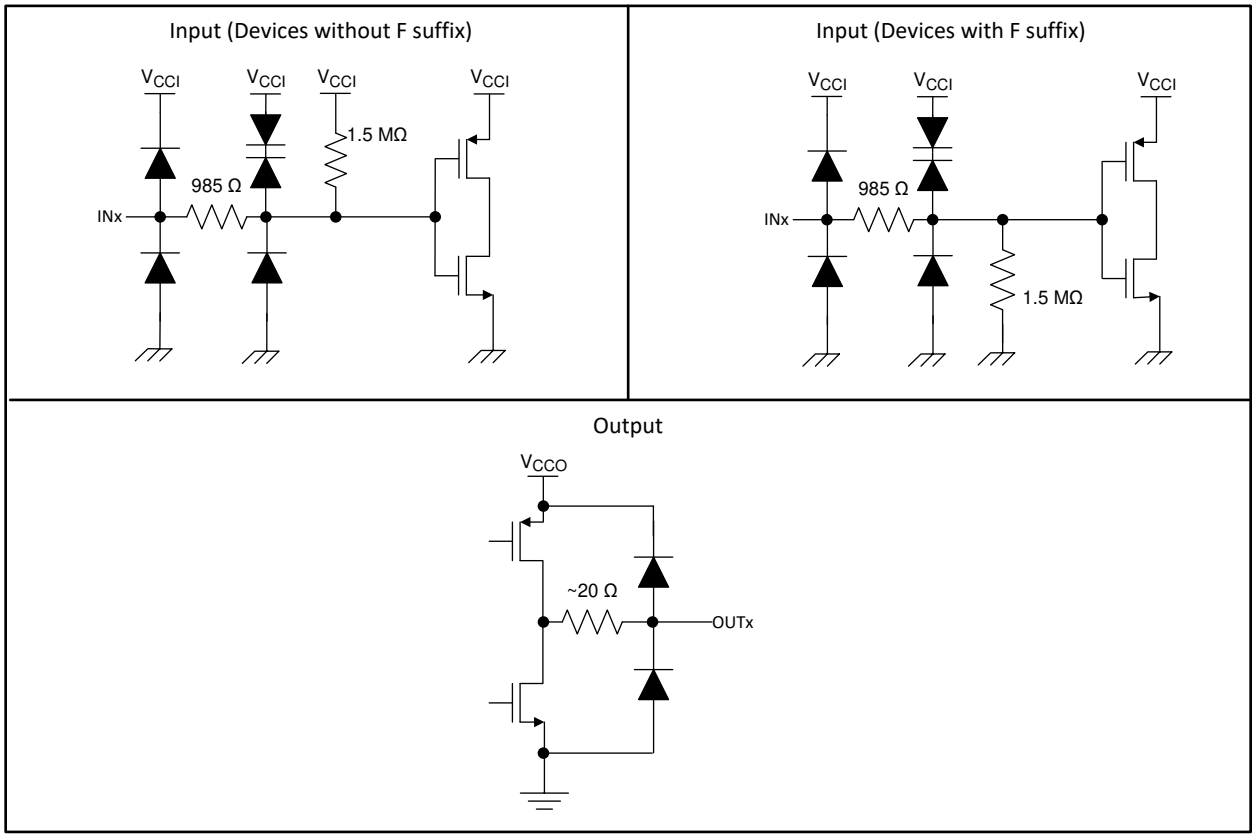





**Figure 8-3. Device I/O Schematics**

# 9 Application and Implementation

**Note**

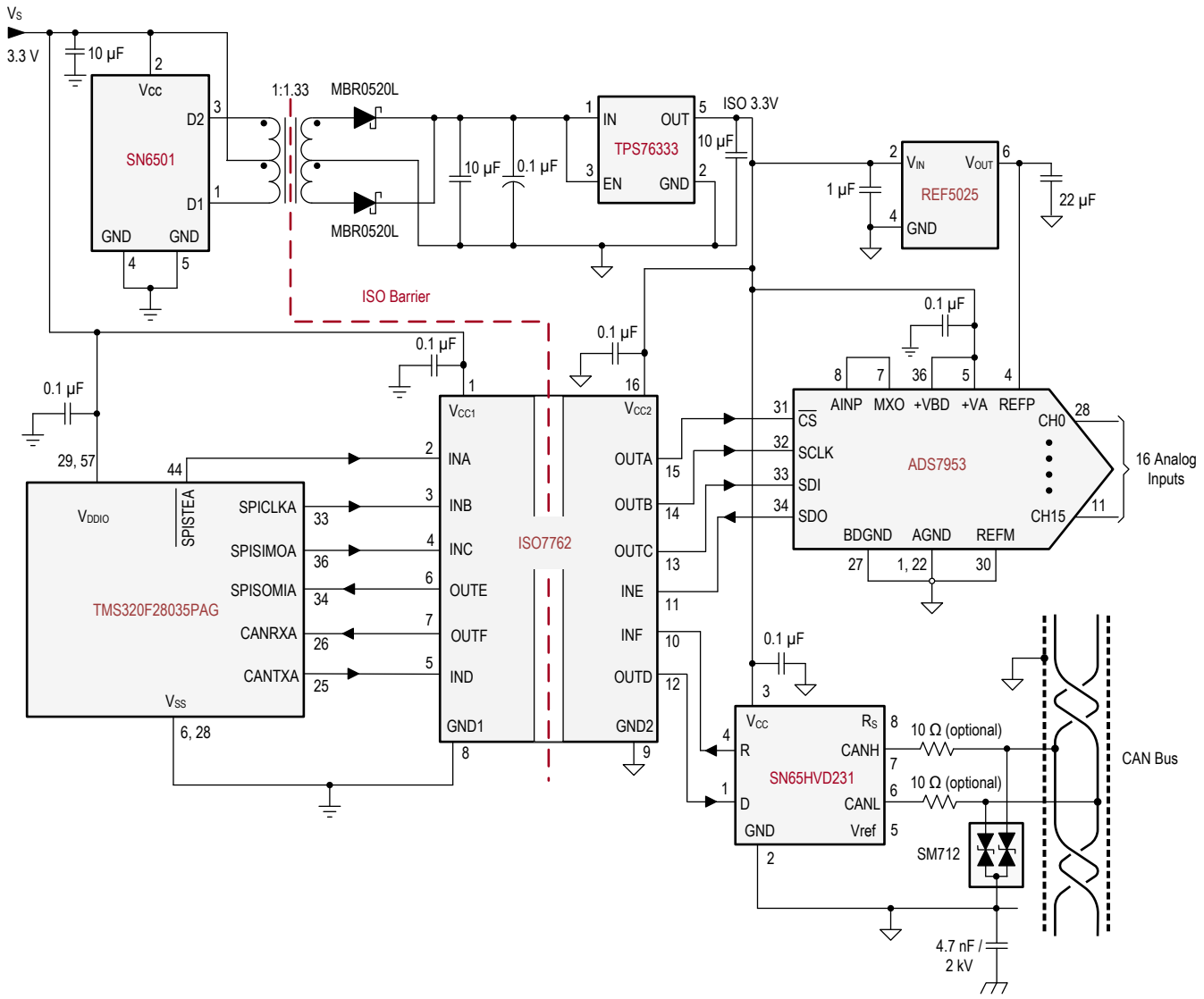
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO776x family of devices is a high-performance, six-channel digital isolators. The ISO776x family of devices uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, $V_{CC1}$ and $V_{CC2}$. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

## 9.2 Typical Application

Figure 9-1 shows the isolated serial-peripheral interface (SPI) and controller-area network (CAN) interface implementation.




Multiple pins and discrete components omitted for clarity purpose.

**Figure 9-1. Isolated SPI and CAN Interface**

### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

**Table 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$ | 2.25 to 5.5 V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1 µF |

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO776x family of devices only requires two external bypass capacitors to operate.

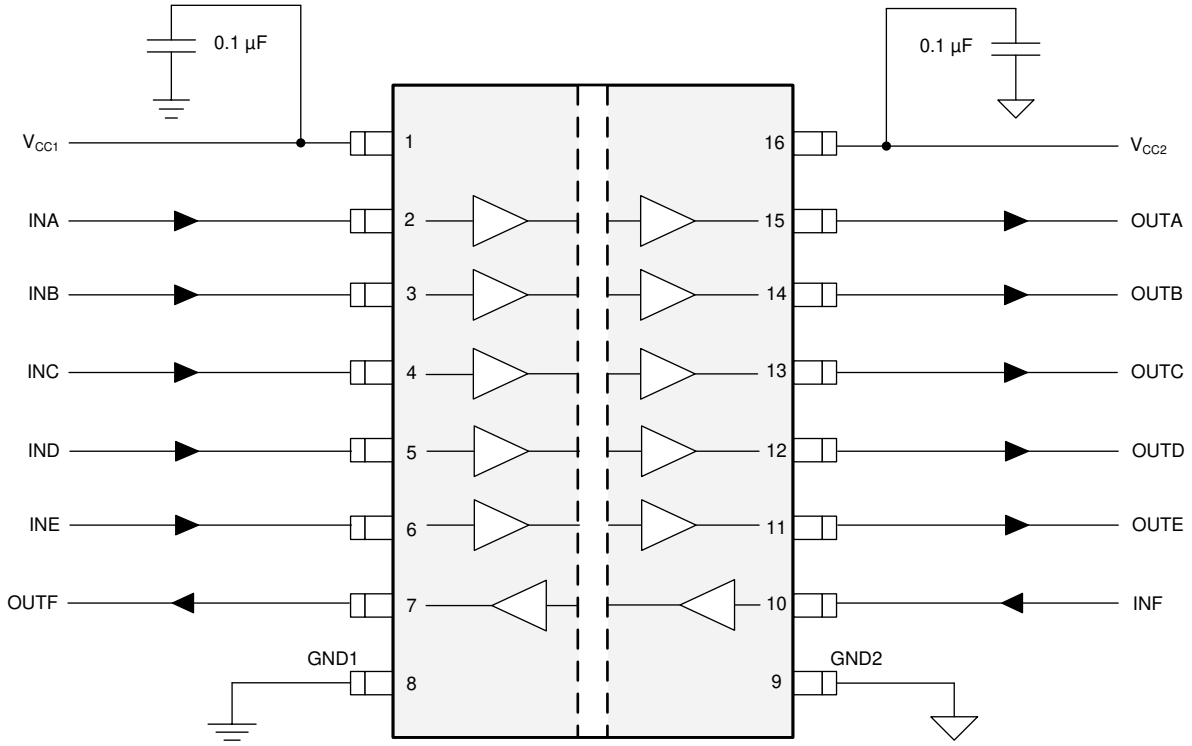



**Figure 9-2. Typical ISO7761 Circuit Hook-up**

### 9.2.3 Application Curves

The typical eye diagram of the ISO776x family of devices indicates low jitter and a wide open eye at the maximum data rate of 100 Mbps.

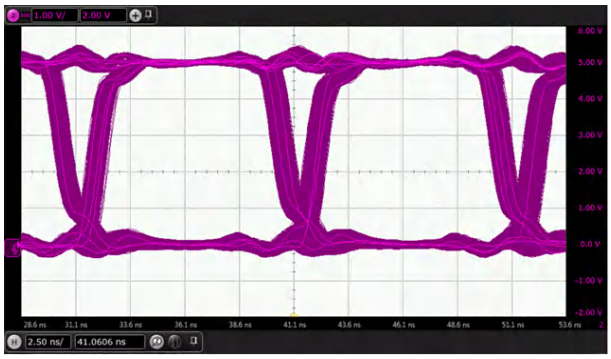


**Figure 9-3. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1 Data, 5 V and 25°C**

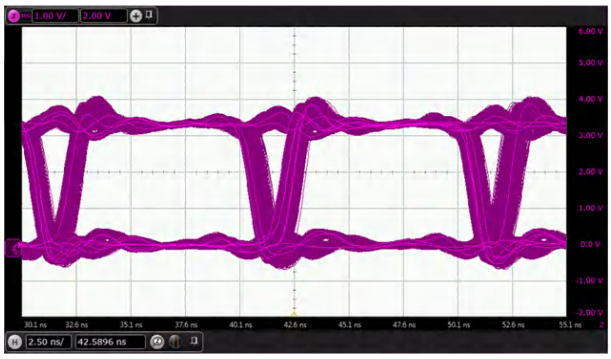


**Figure 9-4. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1 Data, 3.3 V and 25°C**

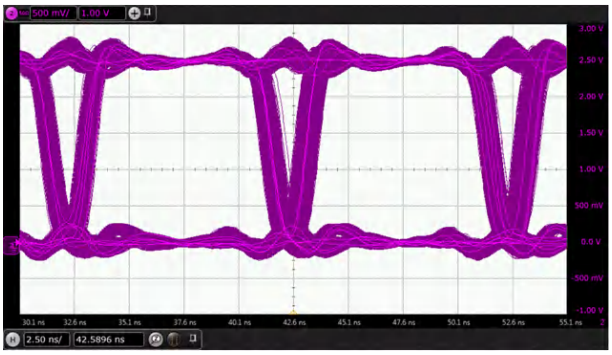


**Figure 9-5. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1 Data, 2.5 V and 25°C**

#### *9.2.3.1 Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-6 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 9-7 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 $V_{RMS}$ with a lifetime of 169 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 $V_{RMS}$ and DBQ-16 package up to 400 $V_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 169 years.

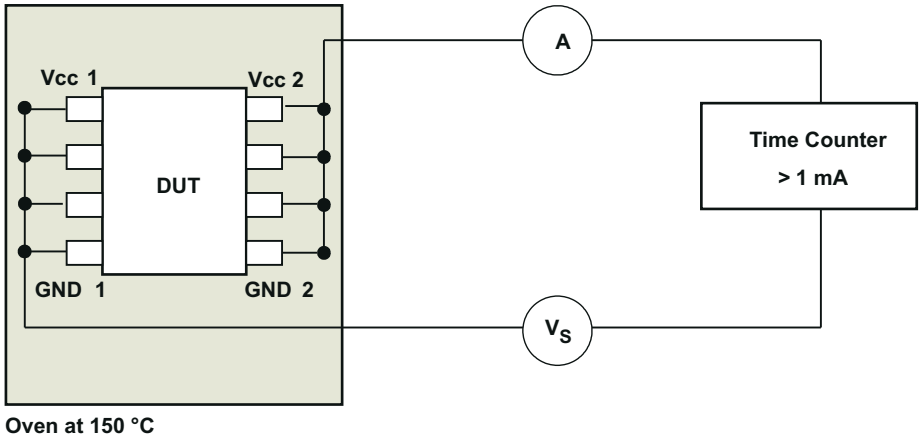



**Figure 9-6. Test Setup for Insulation Lifetime Measurement**

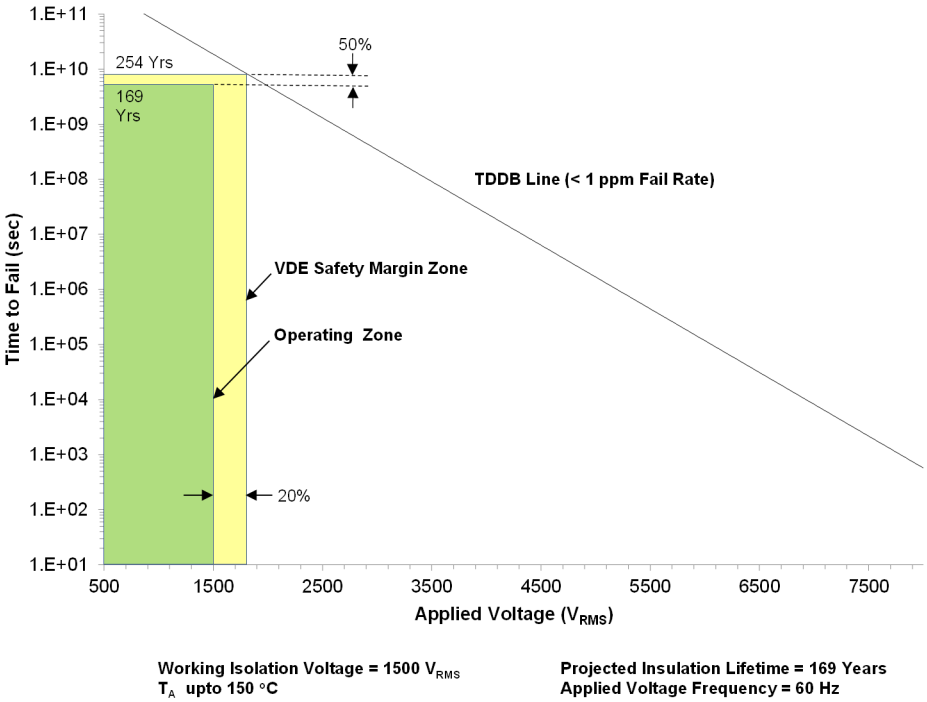



**Figure 9-7. Insulation Lifetime Projection Data**

## 10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins ($V_{CC1}$ and $V_{CC2}$). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

# 11 Layout

## 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* application report.

### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 11.2 Layout Example

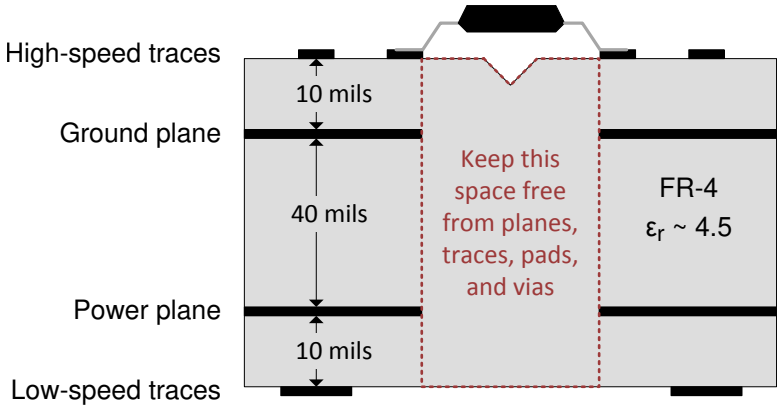



**Figure 11-1. Layout Example Schematic**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide* application report
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application report
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *TMS320F2803xPiccolo™ Microcontrollers* data sheet
- Texas Instruments, *ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs* data sheet
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN65HVD23x 3.3-V CAN Bus Transceivers* data sheet
- Texas Instruments, *TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators* data sheet

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 12-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| ISO7760 | Click here | Click here | Click here | Click here | Click here |
| ISO7761 | Click here | Click here | Click here | Click here | Click here |
| ISO7762 | Click here | Click here | Click here | Click here | Click here |
| ISO7763 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

## 12.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7760DBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7760 | Samples |
| ISO7760DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7760 | Samples |
| ISO7760DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7760 | Samples |
| ISO7760DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7760 | Samples |
| ISO7760FDBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7760F | Samples |
| ISO7760FDBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7760F | Samples |
| ISO7760FDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7760F | Samples |
| ISO7760FDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7760F | Samples |
| ISO7761DBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7761 | Samples |
| ISO7761DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7761 | Samples |
| ISO7761DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7761 | Samples |
| ISO7761DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7761 | Samples |
| ISO7761FDBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7761F | Samples |
| ISO7761FDBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7761F | Samples |
| ISO7761FDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7761F | Samples |
| ISO7761FDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7761F | Samples |
| ISO7762DBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7762 | Samples |
| ISO7762DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7762 | Samples |
| ISO7762DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7762 | Samples |
| ISO7762DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7762 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7762FDBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7762F | Samples |
| ISO7762FDBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7762F | Samples |
| ISO7762FDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7762F | Samples |
| ISO7762FDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7762F | Samples |
| ISO7763DBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7763 | Samples |
| ISO7763DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7763 | Samples |
| ISO7763DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7763 | Samples |
| ISO7763DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7763 | Samples |
| ISO7763FDBQ | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7763F | Samples |
| ISO7763FDBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 7763F | Samples |
| ISO7763FDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7763F | Samples |
| ISO7763FDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | ISO7763F | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF ISO7760, ISO7761, ISO7762, ISO7763 :**

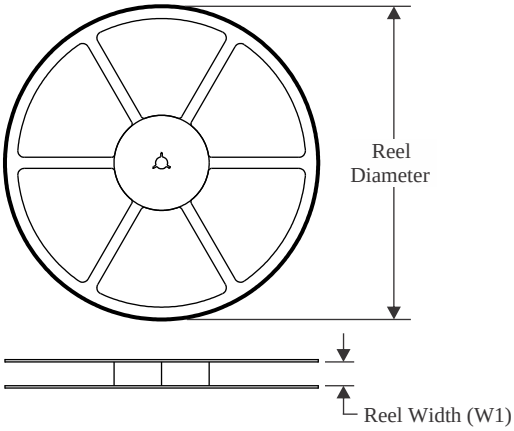
- Automotive : ISO7760-Q1, ISO7761-Q1, ISO7762-Q1, ISO7763-Q1

NOTE: Qualified Version Definitions:

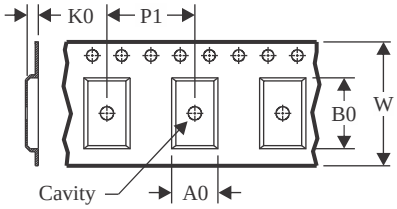
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

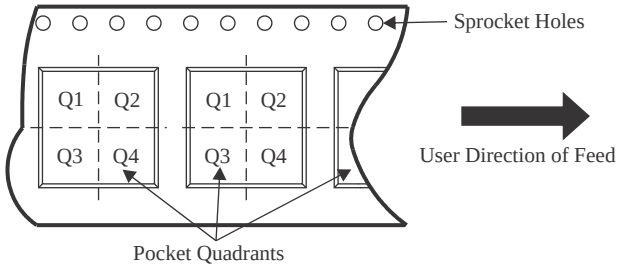



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

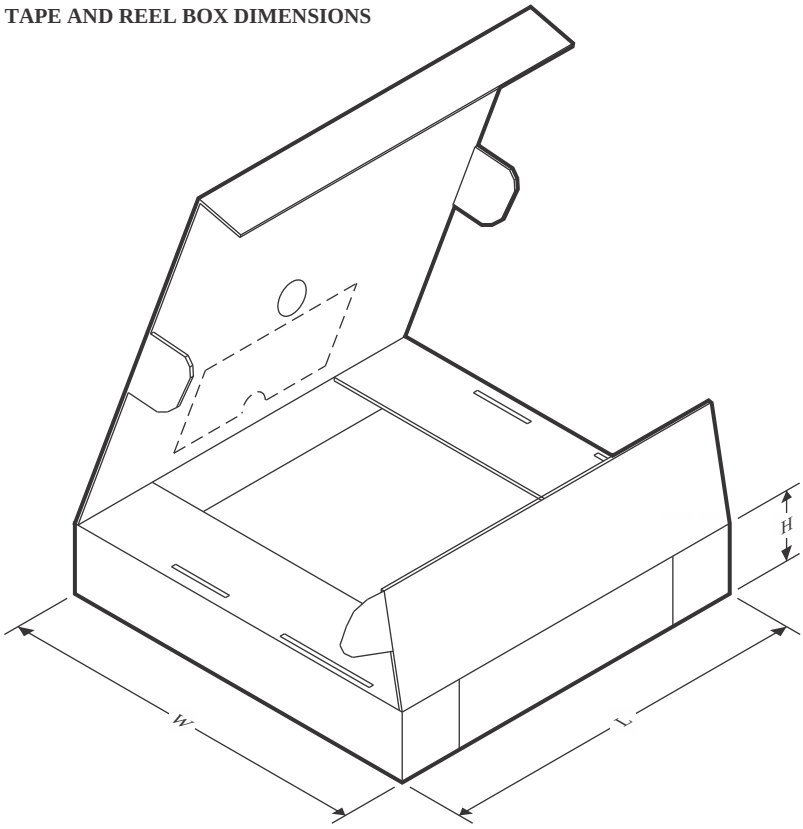



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7760DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7760FDBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761FDBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7762DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7762DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7762DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7762DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7762FDBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763FDBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

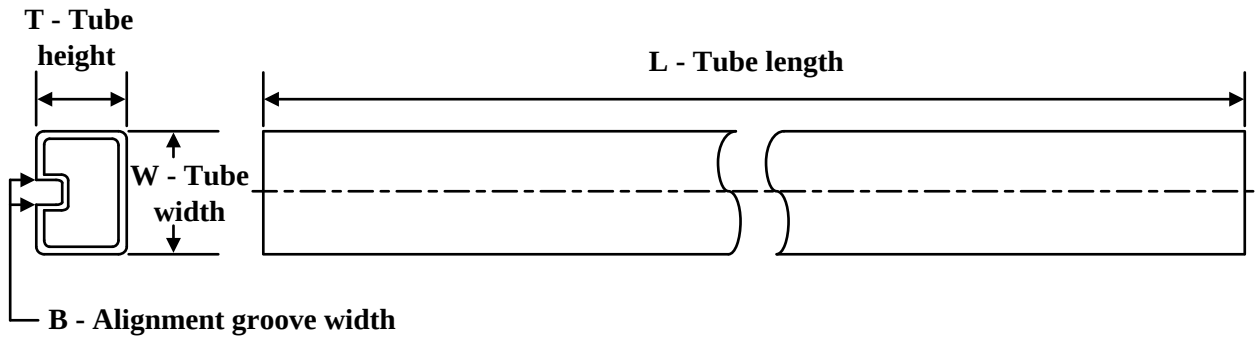



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7760DBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7760DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7760FDBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7760FDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7761DBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7761DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7761FDBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7761FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7762DBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7762DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7762DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7762DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7762FDBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7762FDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7763DBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7763DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7763FDBQR | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 535.4 | 167.6 | 48.3 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7763FDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| ISO7760DBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7760DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7760DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7760FDBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7760FDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7760FDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7761DBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7761DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7761DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7761FDBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7761FDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7761FDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7762DBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7762DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7762DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7762FDBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7762FDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7762FDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7763DBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7763DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7763DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7763FDBQ | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7763FDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7763FDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

# GENERIC PACKAGE VIEW

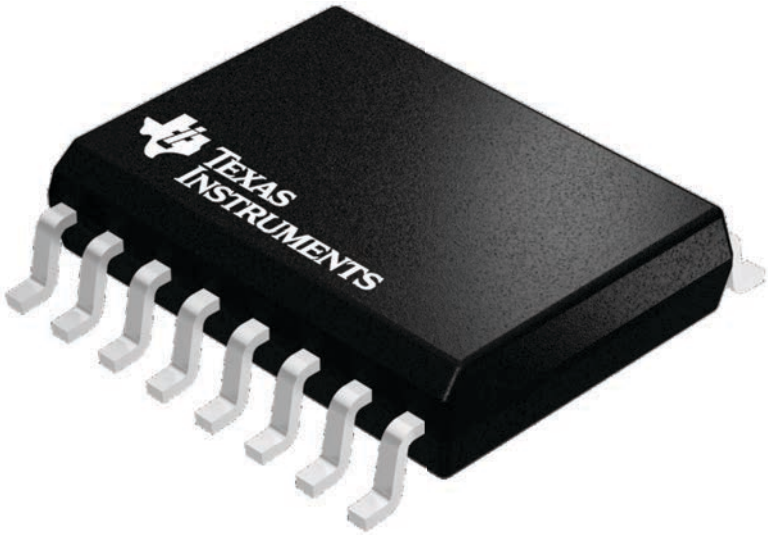
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

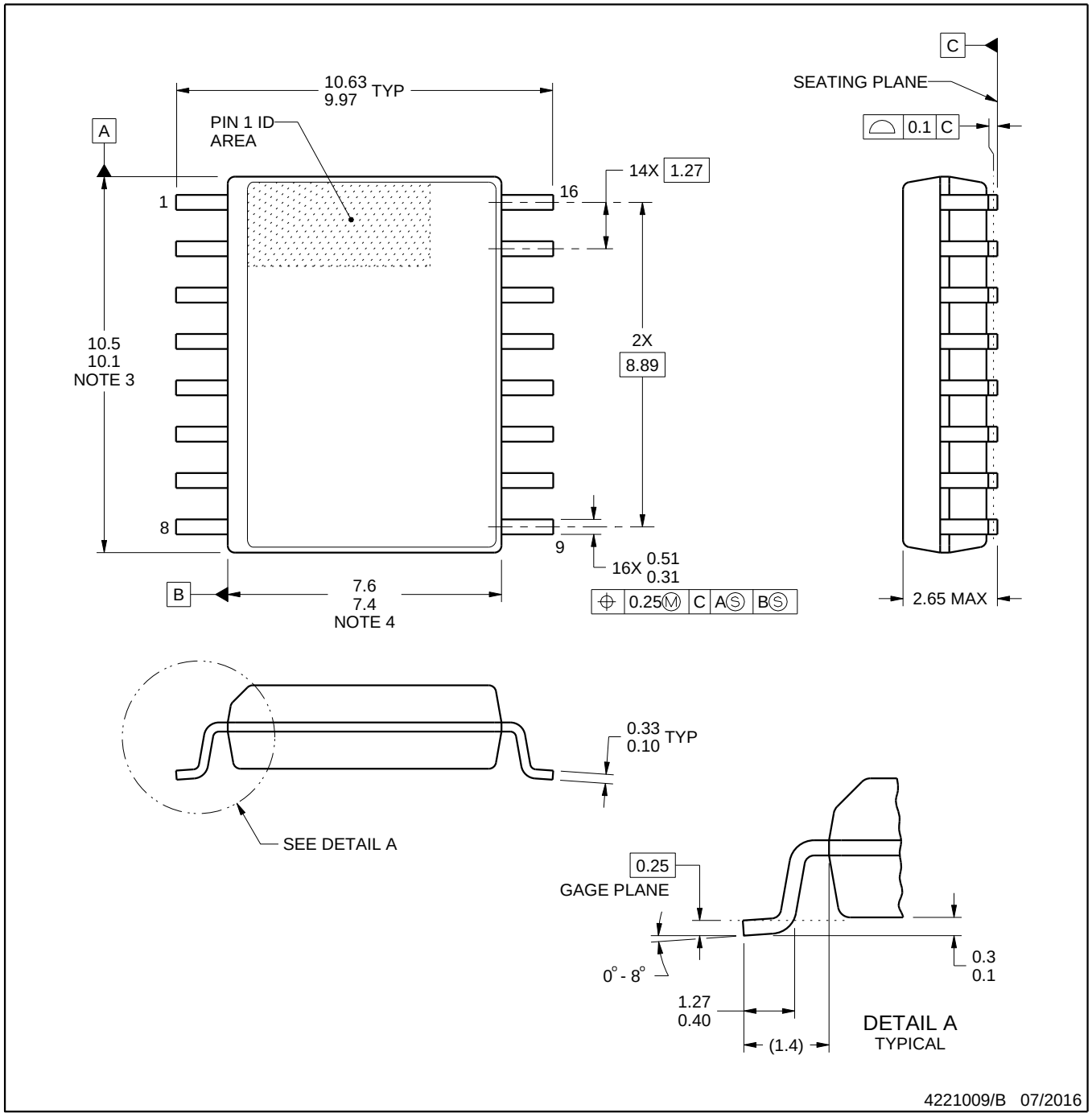
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



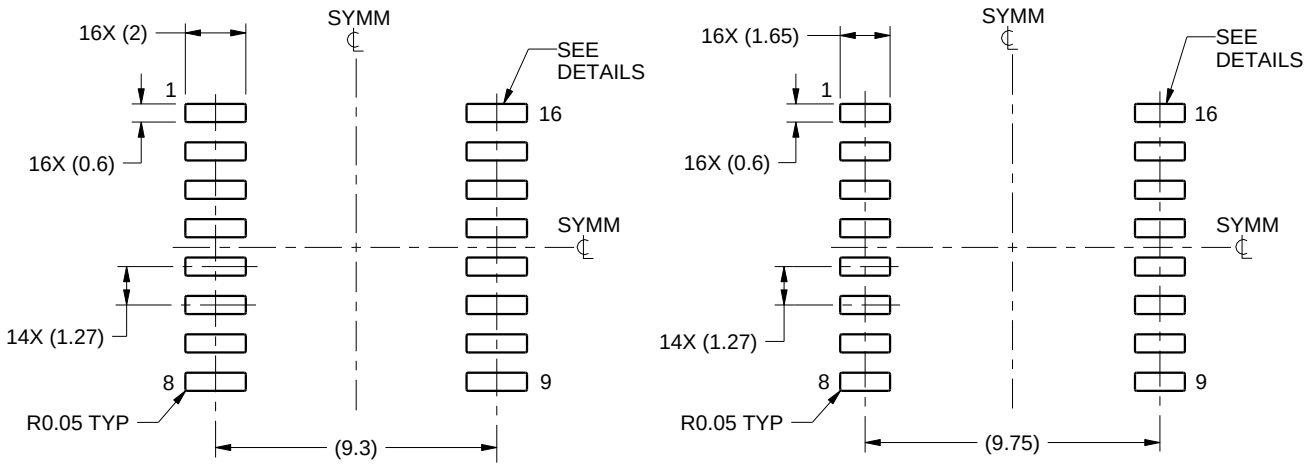

4224780/A

SOIC




NOTES:

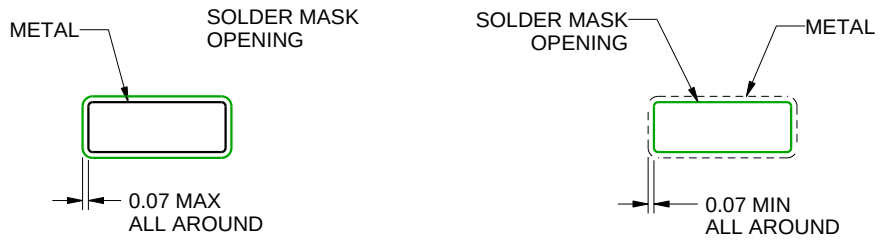
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

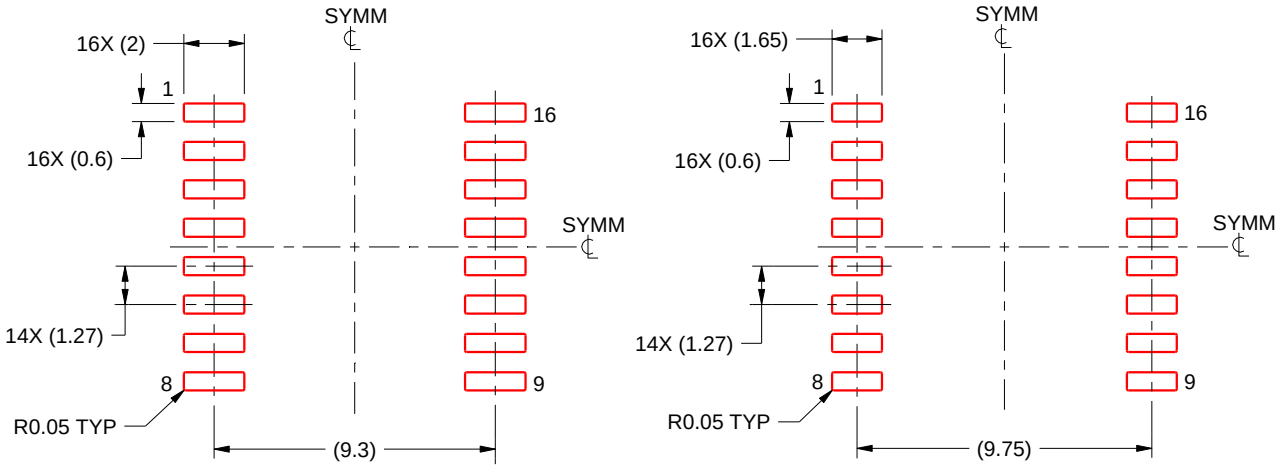
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

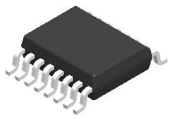
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

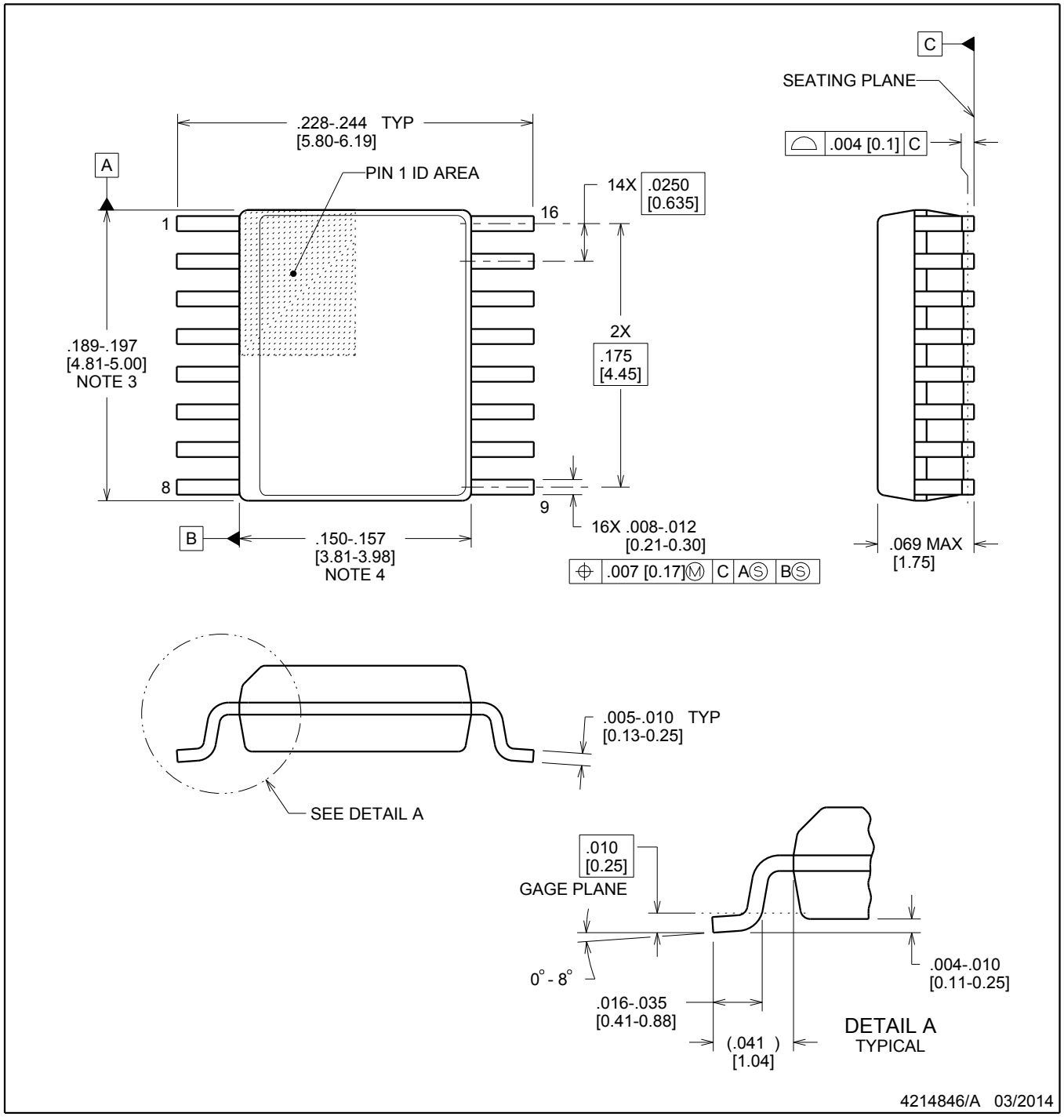


# PACKAGE OUTLINE

## DBQ0016A

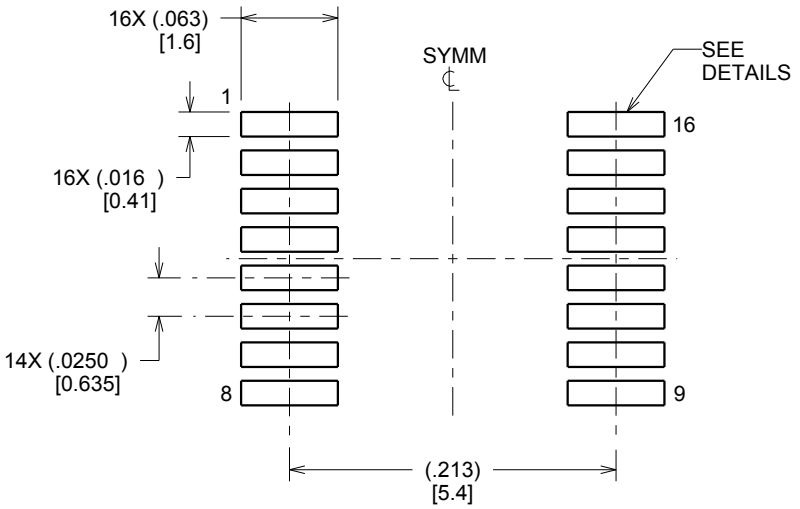
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

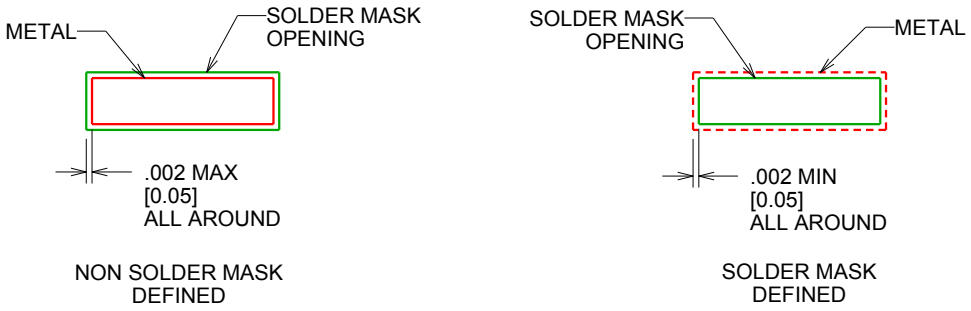



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

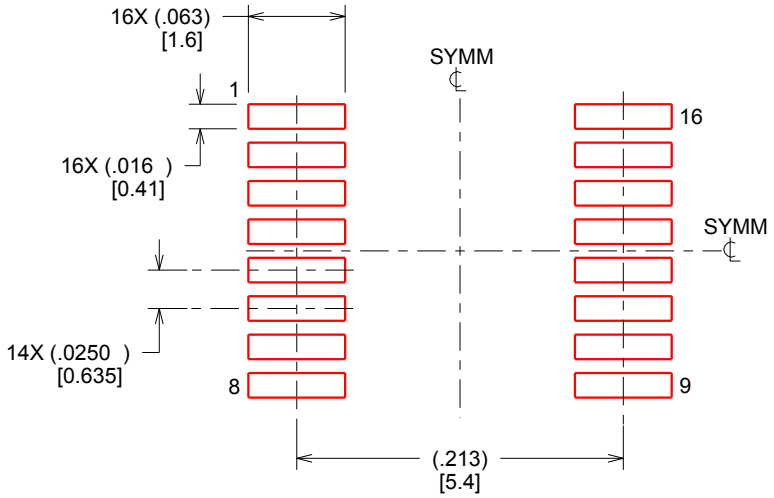
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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