ACPL-P456 and ACPL-W456

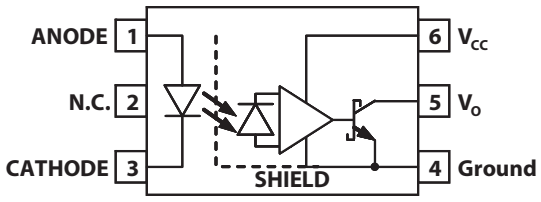
High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

Data Sheet

Description

The ACPL-P456 and ACPL-W456 contain a GaAsP LED optically coupled to an integrated high-gain photo detector. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. Specifications and performance plots are given for typical IPM applications.

Functional Diagram



Note: A 0.1 µF bypass capacitor must be connected between pins 4 and 6.

Truth Table (Positive Logic)

LED	V0
ON	LOW
OFF	HIGH

Applications

- IPM Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters

Features

- Performance Specified for Common IPM Applications Over Industrial Temperature Range
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- High CTR
- Available in Stretched SO-6 Package with 8 mm creepage and clearance
- Safety Approval:
  - UL Recognized with 3750V_{RMS} for 1 minute (5000V_{RMS} for 1 minute for all ACPL-W456 devices and Option 020 device for ACPL-P456) per UL1577
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5 approved with V_{IORM} = 1140V_{peak} (ACPL-W456) and V_{IORM} = 891V_{peak} (ACPL-P456) for Option 060

Specifications

- Wide Operating Temperature Range: –40°C to 100°C
- Maximum Propagation Delay t_{PHL} = 400 ns, t_{PLH} = 490 ns
- Maximum Pulse Width Distortion (PWD) = 450 ns
- 15 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
- CTR > 44% at I_F = 10 mA

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

ACPL-P456 and ACPL-W456 are UL Recognized with 3750V_{RMS} (5000V_{RMS} for ACPL-W456) for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-P456 ACPL-W456	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per tube
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per tube

To order, choose a part number from the part number column and combine with the desired option from the option column to form an ordering part number.

Example 1:

ACPL-P456-560E to order product of Stretched SO-6 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACPL-P456-000E to order product of Stretched SO-6 package in tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Solder Reflow Profile

The recommended reflow profile is per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

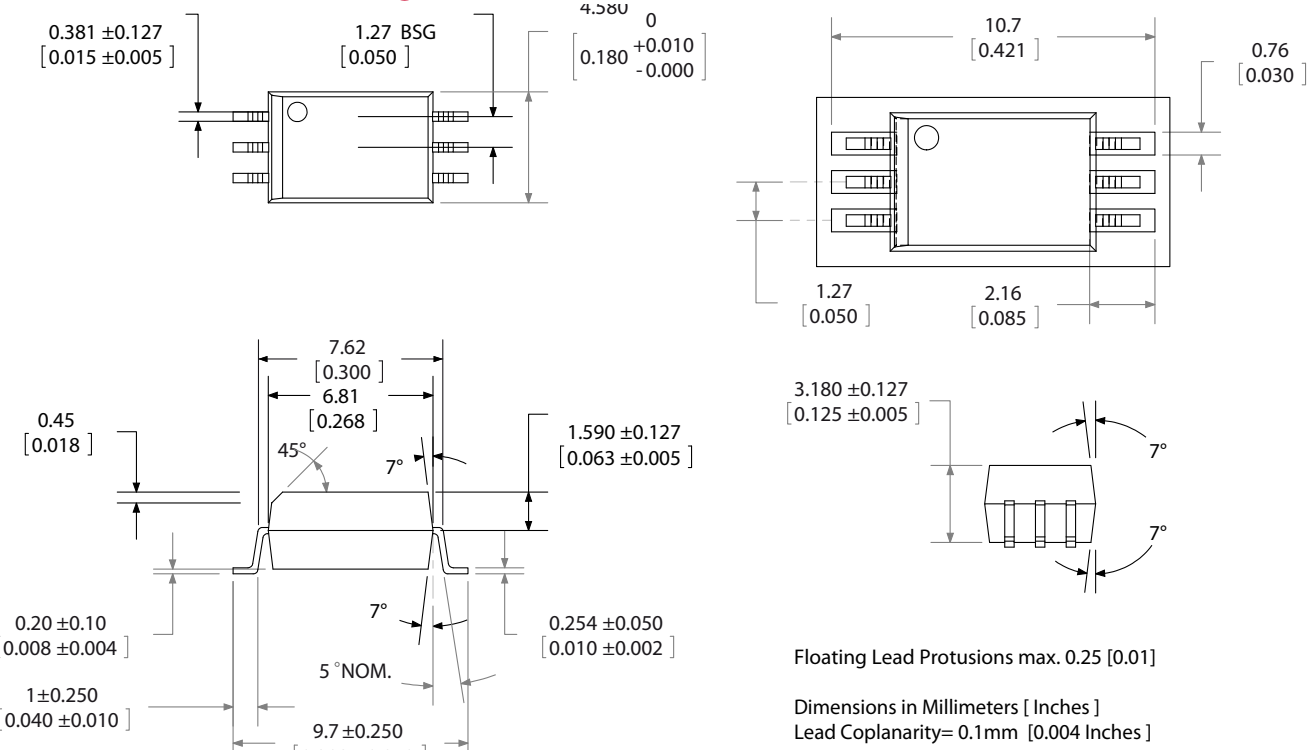
Regulatory Information

The ACPL-P456 and ACPL-W456 are approved by the following organizations:

- IEC/EN/DIN EN 60747-5-5 (Option 060 only): Approved with Maximum Working Insulation Voltage V_{IORM} = 1140V_{peak} (ACPL-W456) and V_{IORM} = 891V_{peak} (ACPL-P456).
- UL: Approval under UL 1577, component recognition program up to V_{ISO} = 3750V_{RMS} (or 5000V_{RMS} for ACPLW456). File E55361.
- CSA: Approval under CSA Component Acceptance Notice #5, File CA 88324.

Package Outline Drawings

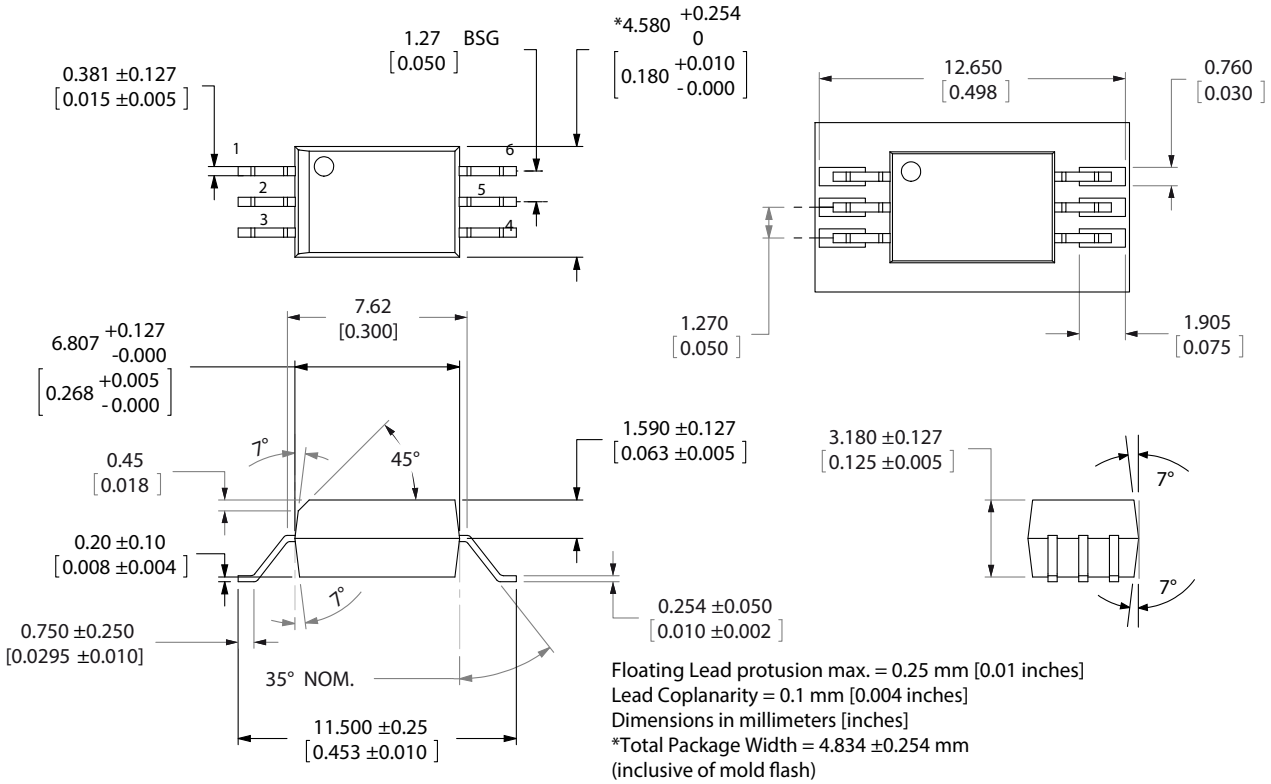
ACPL-P456 Stretched SO-6 Package (7 mm Clearance)



Floating Lead Protusions max. 0.25 [0.01]

Dimensions in Millimeters [Inches]
Lead Coplanarity= 0.1mm [0.004 Inches]

ACPL-W456 Stretched SO-6 Package (8 mm Clearance)



Floating Lead protusion max. = 0.25 mm [0.01 inches]
Lead Coplanarity = 0.1 mm [0.004 inches]
Dimensions in millimeters [inches]
*Total Package Width = 4.834 ±0.254 mm
(inclusive of mold flash)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

Description	Symbol	ACPL-W456	ACPL-P456	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150V_{RMS} for rated mains voltage ≤ 300V_{RMS} for rated mains voltage ≤ 450V_{RMS} for rated mains voltage ≤ 600V_{RMS} for rated mains voltage ≤ 1000V_{RMS}		 I– IV I – IV I – IV I – IV I – III	 I – IV I – IV I – III I – III	
Climatic Classification	55/100/21			
Pollution Degree (DIN VDE 0110/39)	2			
Maximum Working Insulation Voltage	V_{IORM}	1140	891	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2138	1671	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1824	1425	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175		°C
Input Current	$I_{S, INPUT}$	230		mA
Output Power	$P_{S, OUTPUT}$	600		mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$		Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5), for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P456	ACPL-W456	Unit	Condition
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08		mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		N/A		mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175		V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa			Material Group (DIN VDE 0110, 1/89, Table 1).

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	+125	°C	
Operating Temperature	T_A	–40	+100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Input Current (50% duty cycle, <1 ms pulse width)	$I_{F(PEAK)}$		50	mA	2
Peak Transient Input Current ((<1 ìs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage (Pins 3-1)	V_R		5	V	
Average Output Current (Pin 5)	$I_{O(AVG)}$		25	mA	
Output Voltage (Pins 5-4)	V_O	–0.5	+30	V	
Supply Voltage (Pins 6-4)	V_{CC}	–0.5	+30	V	
Output Power Dissipation	P_O			mW	3
Total Power Dissipation	P_T		210	mW	4
Infrared and Vapor Phase Reflow Temperature	See Reflow Thermal Profile				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	4.5	30	V	
Output Voltage	V_O	0	30	V	
Input Current (ON)	$I_{F(OFF)}$	10	20	mA	
Input Voltage (OFF)	$V_{F(ON)}$	–5	0.8	V	
Operating Temperature	T_A	–40	+100	°C	

Electrical Specifications

Over recommended operating conditions unless otherwise specifi ed: T_A = –40°C to +100°C, V_{CC} = 4.5V to 30V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = –5V to +0.8V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	44	90		%	I_F = 10 mA, V_O = 0.6V		5
Low Level Output Current	IOL	4.4	9.0		mA	I_F = 10 mA, V_O = 0.6V	1, 2	
Low Level Output Voltage	VOL		0.3	0.6	V	I_O = 2.4 mA		
Input Threshold Current	ITH		1.5	5.0	mA	V_O = 0.8V, I_O = 0.75 mA	1	9
High Level Output Current	IOH		5	50	µA	V_F = 0.8V	3	
High Level Supply Current	ICCH		0.6	1.3	mA	V_F = 0.8V, V_O = Open		9
Low Level Supply Current	ICCL		0.6	1.3	mA	I_F = 10 mA, V_O = Open		9
Input Forward Voltage	VF		1.5	1.8	V	I_F = 10 mA	4	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	ΔVF/ΔTA		−1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BVR	5			V	I_R = 10 µA		
Input Capacitance	CIN		60		pF	f = 1 MHz, V_F = 0V		

Switching Specifications (R_L = 20 kΩ)

Over recommended operating conditions unless otherwise specified. T_A = −40°C to +100°C, V_{CC} = +4.5V to 30V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = −5V to 0.8V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	30	200	400	ns	C_L = 100 pF	$I_{F(ON)}$ = 10 mA, $V_{F(OFF)}$ = 0.8V, V_{CC} = 15.0V, V_{THLH} = 2.0V, V_{THHL} = 1.5V	5, 7, 8, 9, 10, 11	8, 9
			100			C_L = 10 pF			
Propagation Delay Time to Logic High Output Level	t_{PLH}	270	400	550	ns	C_L = 100 pF			
			130			C_L = 10 pF			
Pulse Width Distortion	PWD		200	450	ns	C_L = 100 pF			13
Propagation Delay Difference Between Any 2 Parts	$t_{PLH} - t_{PHL}$	−150	+200	+450	ns				10
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0V, C_L = 100 pF, V_{CM} = 1500 V_{P-P}, T_A = 25°C	6	11
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	I_F = 10 mA, V_O < 1.0 V			12

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750[b] 5000[c]			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C		6, 7
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V_{DC}		6
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz		6

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

b. For all ACPL-W456 devices.

c. For ACPL-W456 and Option 020 of ACPL-P456)

Notes:
1. Derate linearly above 90°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 90°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 90°C free-air temperature at a rate of 3.0 mA/°C.
4. Derate linearly above 90°C free-air temperature at a rate of 4.2 mA/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (IF) times 100.
6. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5, and 6 shorted together.
7. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage. 4500V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA); each optocoupler under ACPL-W456 is proof tested by applying an insulation test voltage. 6000V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
8. Pulse: f = 20 kHz, Duty Cycle = 10%.
9. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 can improve performance by filtering power supply line noise.
10. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
11. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0V$).
12. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0V$).
13. Pulse Width Distortion (PWD) is defi ned as $|t_{PHL} - t_{PLH}|$ for any given device.

Figure 1 Typical Transfer Characteristics

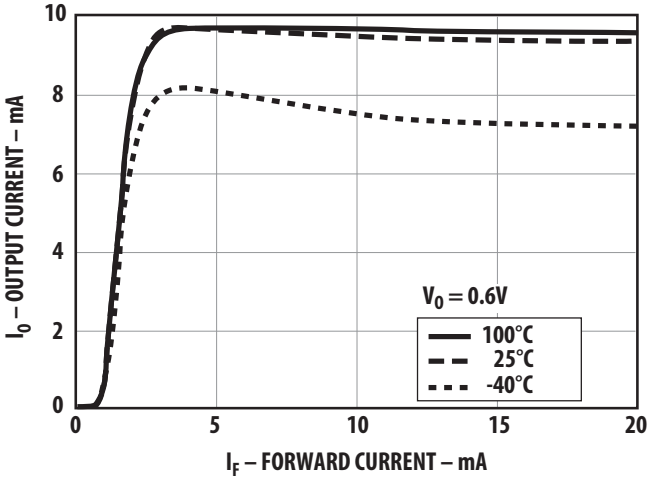


Figure 2 Normalized Output Current vs. Temperature

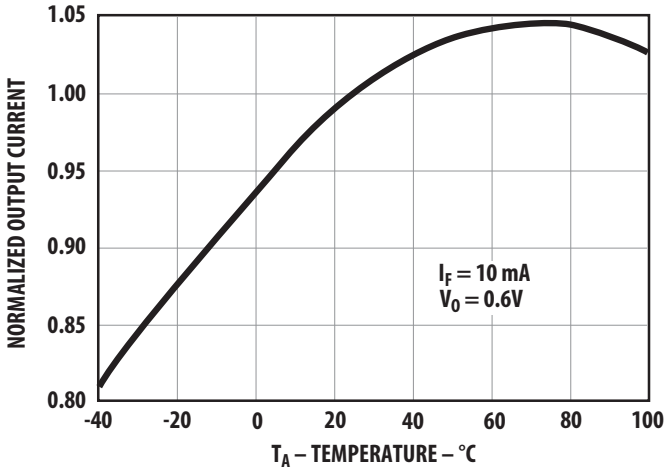


Figure 3 High Level Output Current vs. Temperature

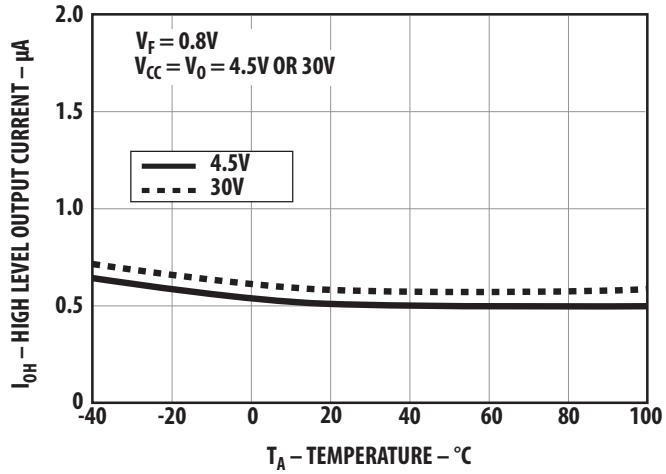


Figure 4 Input Current vs. Forward Voltage

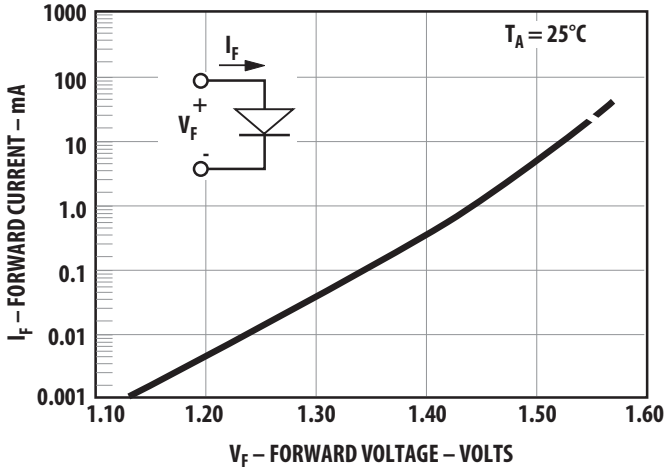
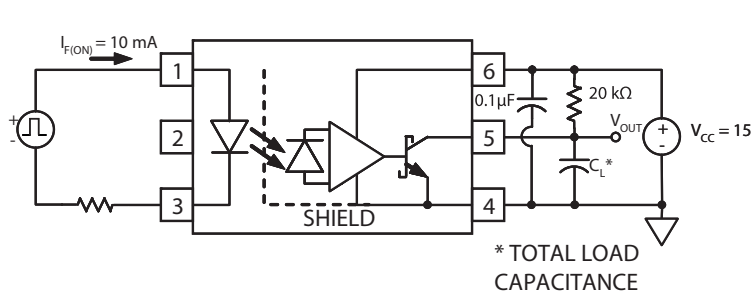


Figure 5 Propagation Delay Test Circuit



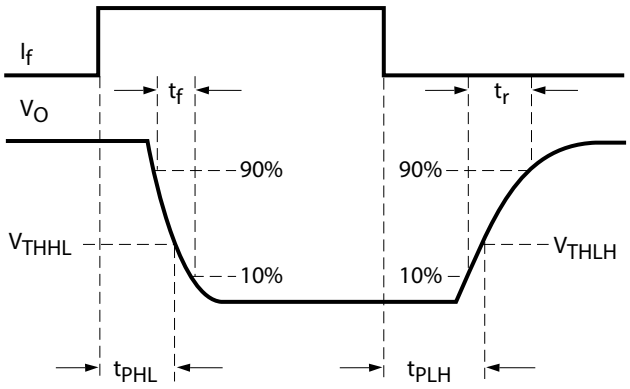
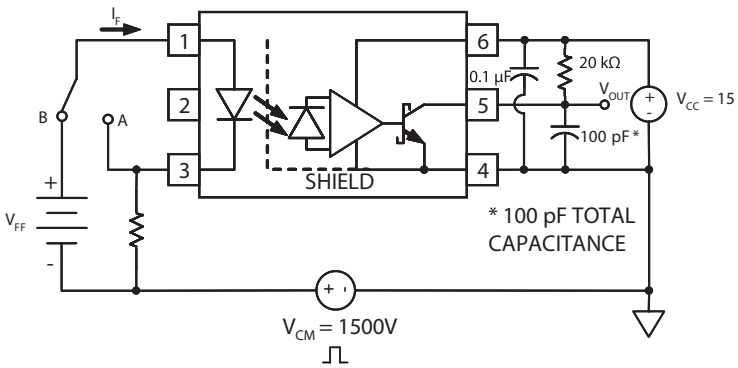


Figure 6 CMR Test Circuit and Waveforms



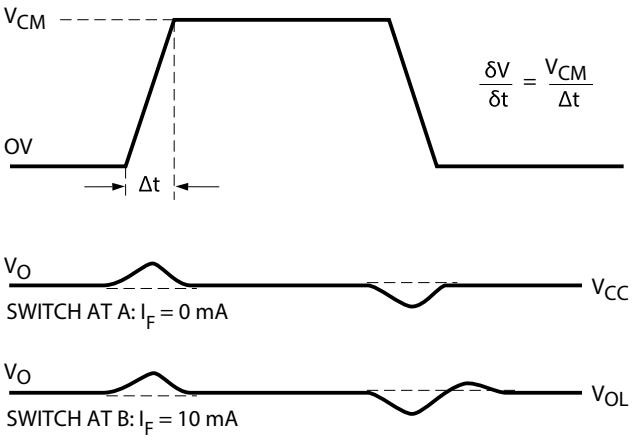


Figure 7 Propagation Delay with External 20 kΩ RL vs. Temp.

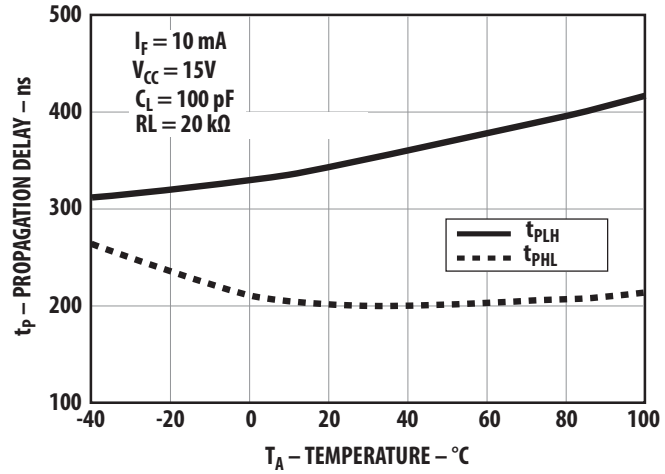


Figure 8 Propagation Delay vs. Load Resistance

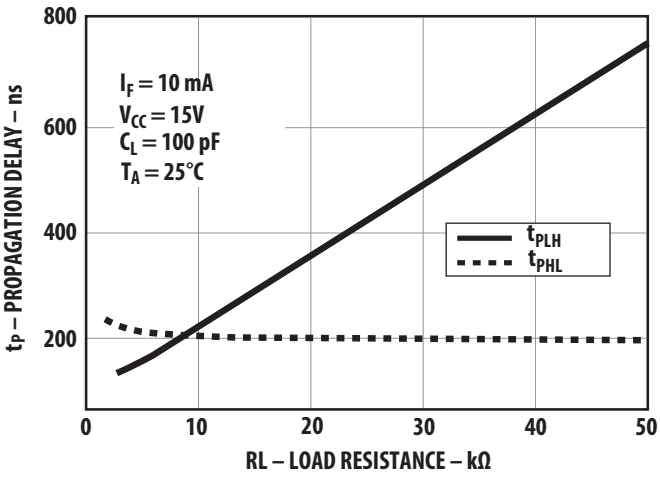


Figure 9 Propagation Delay vs. Load Capacitance

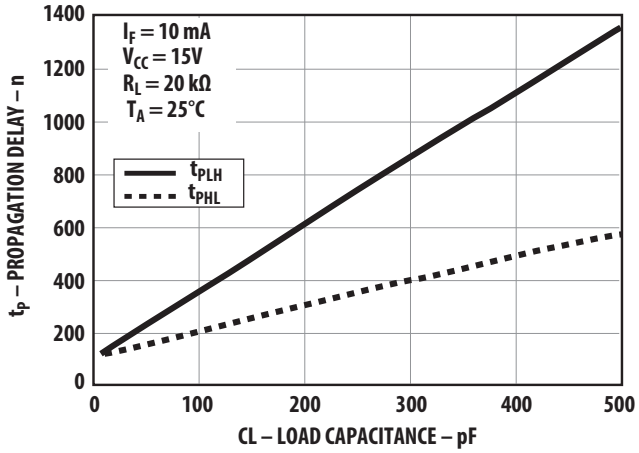


Figure 10 Propagation Delay vs. Supply Voltage

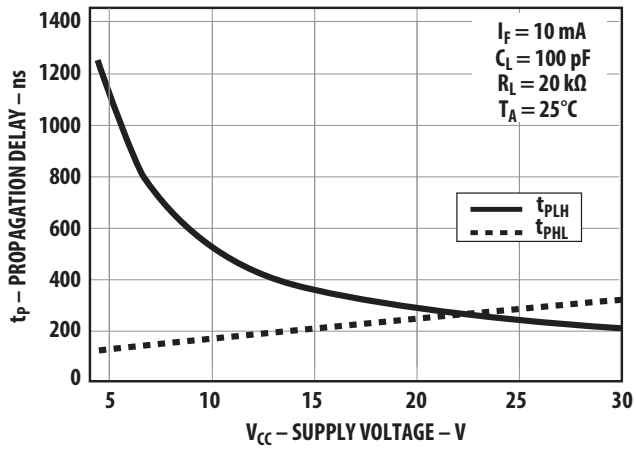
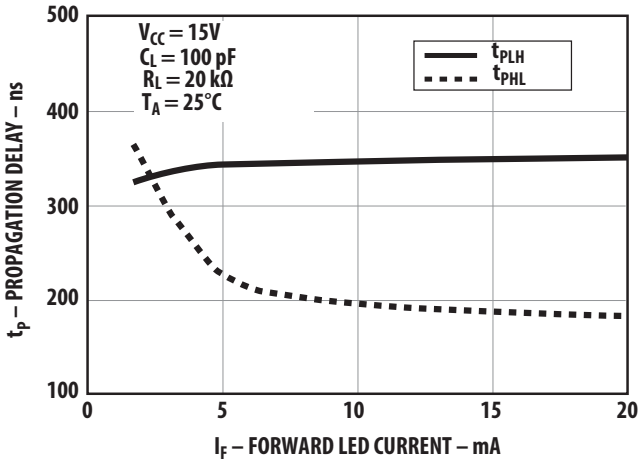


Figure 11 Propagation Delay vs. Input Current



Applications Information

LED Drive Circuit Considerations For Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 13. The ACPL-P456/W456 improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pin and output ground as shown in Figure 14. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 12), can achieve 15 kV/µs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 12 to keep the LED off when the gate is in the high state.

Figure 12 Recommended LED Drive Circuit

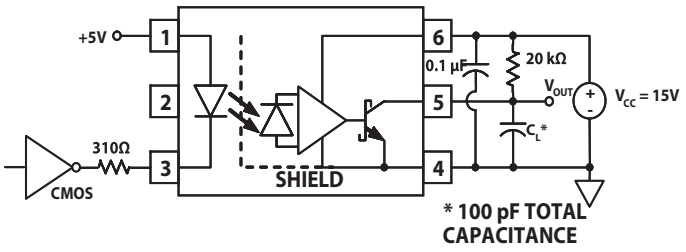
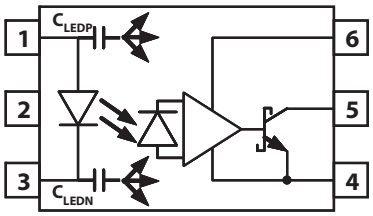
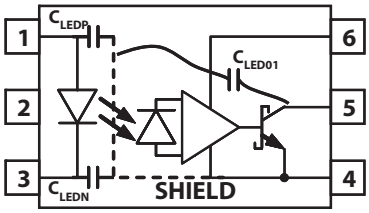


Figure 13 Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers



Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through CLEDO1 in Figure 14. Many factors influence the effect and magnitude of the direct coupling including: the position of the LED current setting resistor and the value of the capacitor at the optocoupler output (CL).

Figure 14 Optocoupler Input to Output Capacitance Model for Shielded Optocouplers



CMR With The LED On (CMRL)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 4.0 mA (see Figure 1) to achieve 15 kV/µs CMR.

The placement of the LED current setting resistor effects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 15 is connected to the anode. Figure 16 shows the AC equivalent circuit for Figure 15 during common mode transients. During a $+dV_{CM}/dt$ in Figure 16, the current available at the LED anode (I_{total}) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 12) places the current setting resistor in series with the LED cathode. Figure 17 is the AC equivalent circuit for Figure 12 during common mode

transients. In this case, the LED current is not reduced during a $+dV_{CM}/dt$ transient because the current fl owing through the package capacitance is supplied by the power supply. During a $-dV_{CM}/dt$ transient, however, the LED current is reduced by the amount of current flowing through C_{LEDN}. But, better CMR performance is achieved since the current fl owing in C_{LEDO1} during a negative transient acts to keep the output low.

Figure 15 LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended)

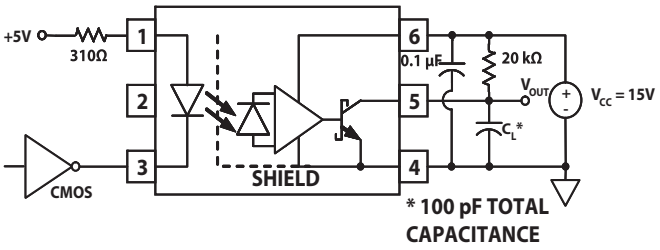


Figure 16 AC Equivalent Circuit for Figure 15 During Common Mode Transients

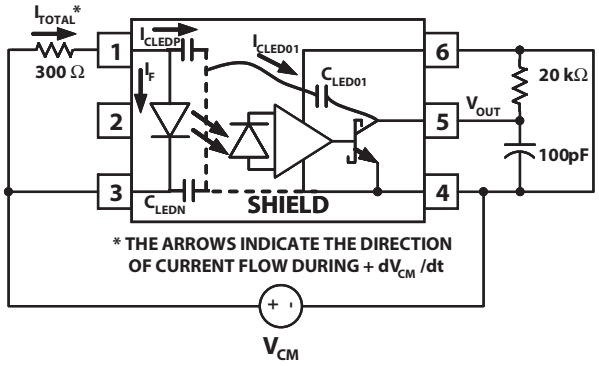
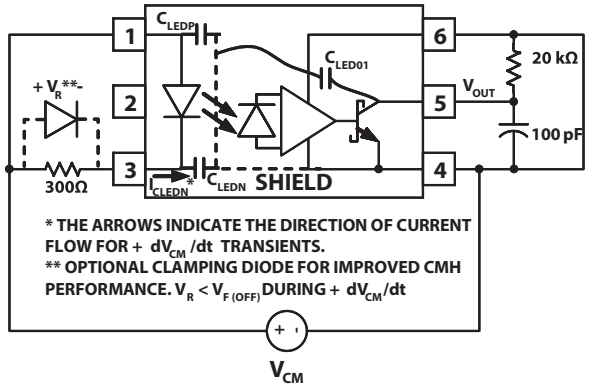


Figure 17 AC Equivalent Circuit for Figure 12 During Common Mode Transients



CMR With The LED Off (CMRH)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $+dV_{CM}/dt$ transient in Figure 17, the current flowing through CLEDN is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 5-4 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 12) provides about 10V of margin between the lowest optocoupler output voltage and a 3V IPM threshold during a 15 kV/µs transient with V_{CM} = 1500V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 17, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 18, cannot keep the LED off during a $+dV_{CM}/dt$ transient, it is not desirable for applications requiring ultra high CMR_H performance. Figure 19 is the AC equivalent circuit for Figure 18 during common mode transients. Essentially all the current flowing through C_{LEDN} during a $+dV_{CM}/dt$ transient must be supplied by the LED. CMRH failures can occur at dv/dt rates where the current through the LED and C_{LEDN} exceeds the input threshold. Figure 20 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

Figure 18 Not Recommended Open Collector LED Drive Circuit

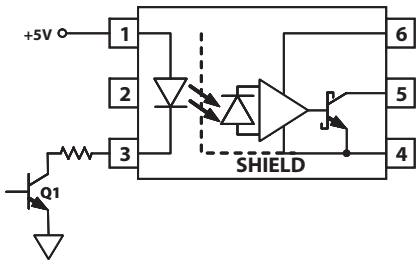


Figure 19 AC Equivalent Circuit for Figure 18 During Common Mode Transients

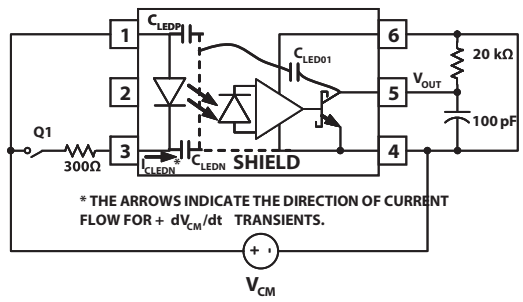
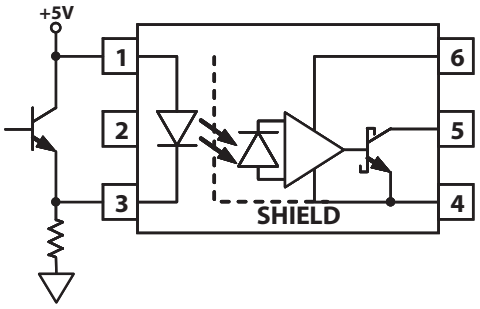


Figure 20 Recommended LED Drive Circuit for Ultra High CMR



IPM Dead Time and Propagation Delay Specifications

The ACPL-P456/W456 includes a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 21) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 22. A minimum dead time of zero is achieved in Figure 22 when the signal to turn on LED2 is delayed by (t_{PLH} max – t_{PHL} min) from the LED1 turn off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, previous equation are not the same as the t_{PLH} max and t_{PHL} min, over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification which is specified at 450 ns for the ACPL-P456/W456 over an operating temperature range of –40°C to +100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 23. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the ACPL-P456/W456 are 600 ns (= 450 ns – (–150 ns)) over an operating temperature range of –40°C to +100°C.

Figure 21 Typical Application Circuit

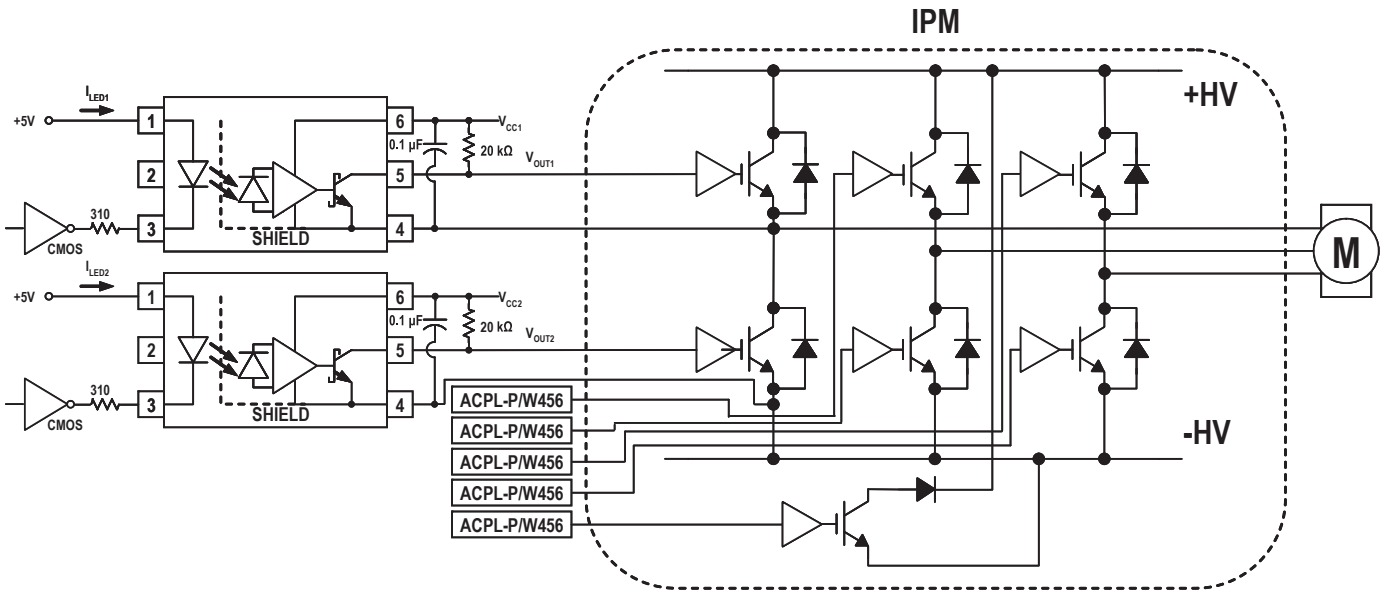
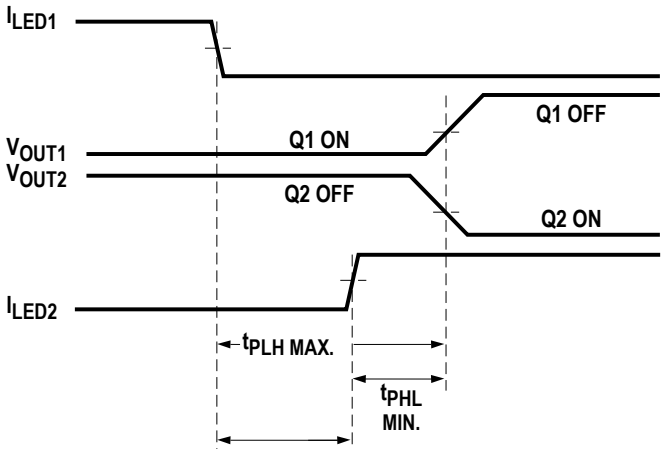


Figure 22 Minimum LED Skew for Zero Dead Time

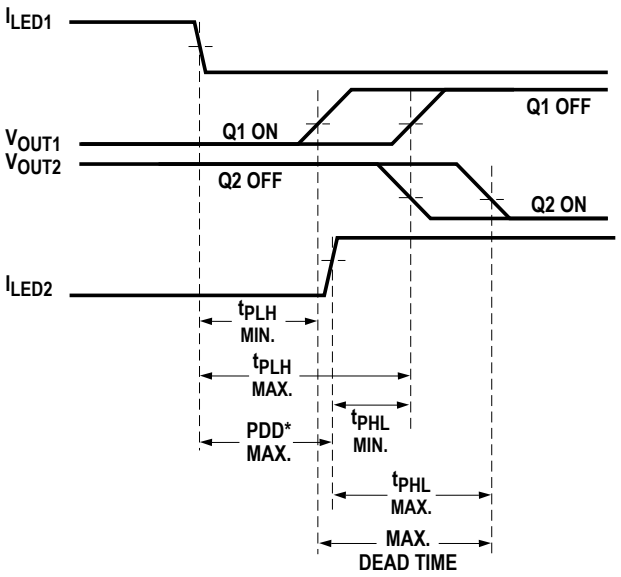


PDD* MAX. =
$(t_{PLH}-t_{PHL})$ MAX. = t_{PLH} MAX. - t_{PHL} MIN.

***PDD = PROPAGATION DELAY DIFFERENCE**

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.

Figure 23 Waveforms for Deadtime Calculation



MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)
= ($t_{PLH\ MAX.}$ - $t_{PLH\ MIN.}$) + ($t_{PHL\ MAX.}$ - $t_{PHL\ MIN.}$)
= ($t_{PLH\ MAX.}$ - $t_{PHL\ MIN.}$) - ($t_{PLH\ MIN.}$ - $t_{PHL\ MAX.}$)
= PDD* MAX. - PDD* MIN.

***PDD = PROPAGATION DELAY DIFFERENCE**

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE THE MAXIMUM DEAD TIME ARE TAKEN AT EQUAL TEMPERATURES.

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