74LVC595A

8-bit serial-in/serial-out or parallel-out shift register; 3-state

Rev. 2 — 20 June 2014 Product data sheet

1. General description

The 74LVC595A is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial Power-down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Data is shifted on the positive-going transitions of the SHCP input. The data in the shift register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial output (Q7S) for cascading purposes. It is also provided with asynchronous reset input $\overline{MR}$ (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM JESD22-A114-D exceeds 2000 V
  - CDM JESD22-C101-C exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC595AD	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC595APW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC595ABQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

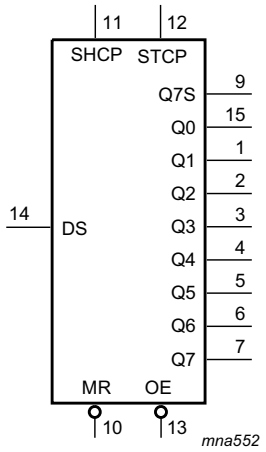


Fig 1. Logic symbol

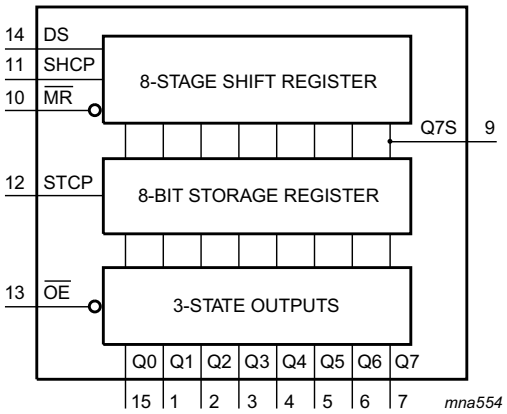


Fig 2. Functional diagram

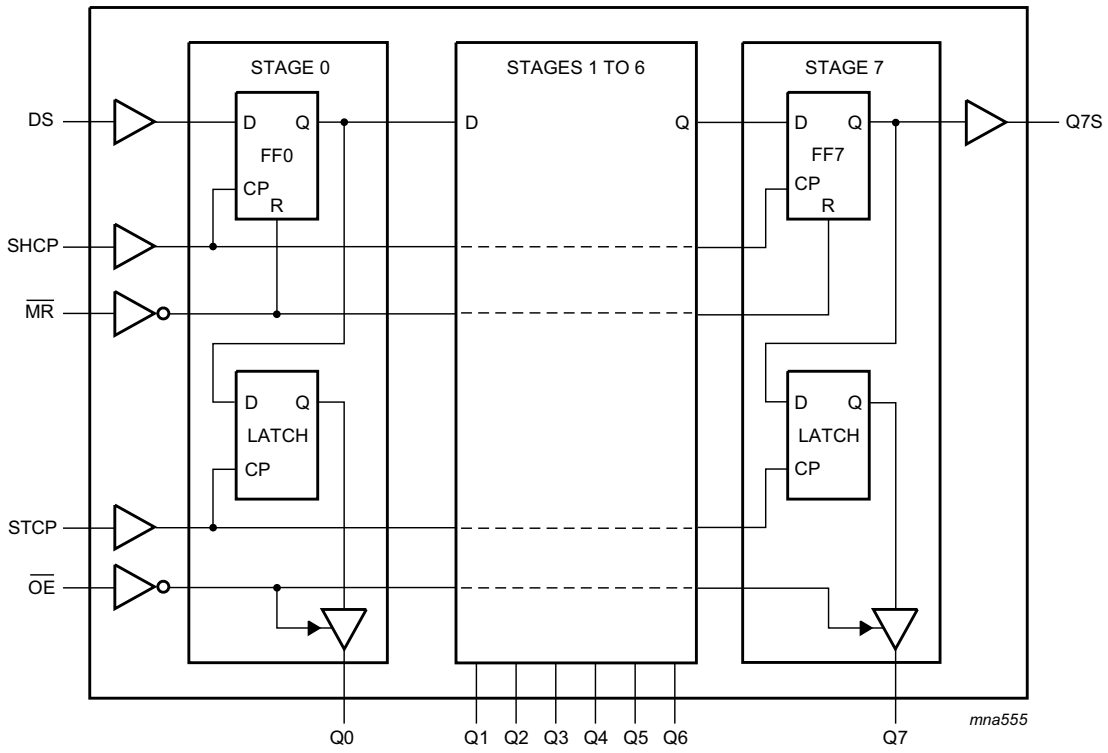


Fig 3. Logic diagram

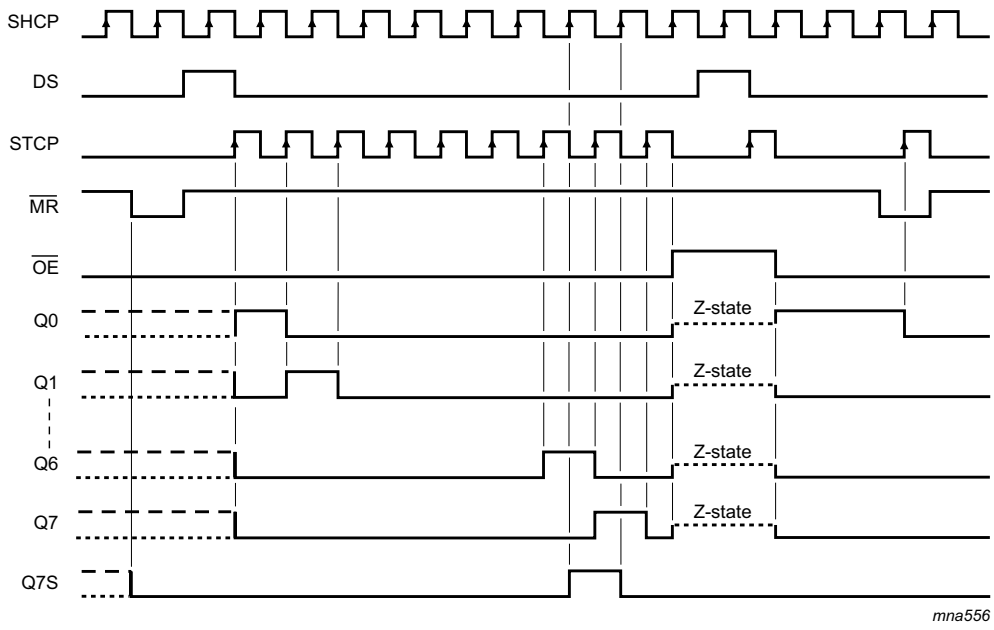


Fig 4. Timing diagram

6. Pinning information

6.1 Pinning

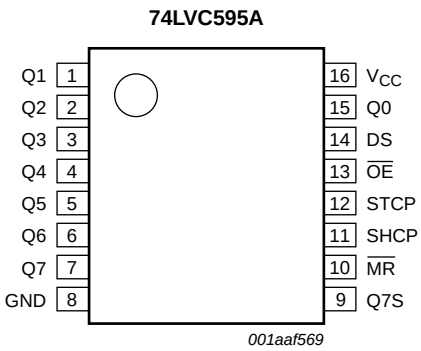
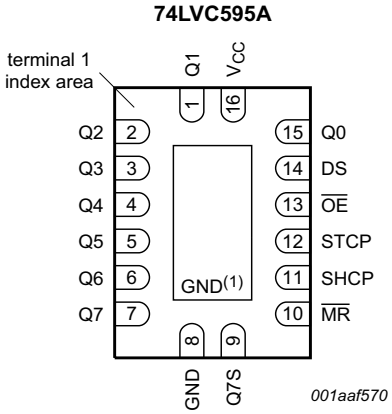


Fig 5. Pin configuration SO16 and TSSOP16



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q[0:7]	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Input					Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-state on $\overline{MR}$ only affects the shift register
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-state shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW-to-HIGH transition;
X = don't care;
NC = no change;
Z = high-impedance OFF-state.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	−50	-	mA
V_I	input voltage	[1]	−0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	3-state [1]	−0.5	6.5	V
		output HIGH or LOW state [1]	−0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		−100	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	3-state	0	-	5.5	V
		output HIGH or LOW state	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.2	-	-	V_{CC} − 0.3	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = −18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics *…continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V [2]	-	0.1	±10	-	±20	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	0.1	10	-	20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 1.65 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] For transceivers, the parameter I_{OZ} includes the input leaking current.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	SHCP to Q7S; see Figure 7 [2]						
		V_{CC} = 1.2 V	-	17.5	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	6.6	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.2	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V	1.5	4.7	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	4.0	6.7	1.5	7.7	ns
		STCP to Qn; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	16.8	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	5.8	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.7	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V	1.5	4.0	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.3	6.7	1.2	7.7	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Figure 11						
		V_{CC} = 1.2 V	-	17.3	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	6.9	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.3	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V	1.5	4.5	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.8	6.7	1.2	7.7	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 12 [3]						
		V_{CC} = 1.2 V	-	17.9	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	6.4	14.1	2.0	16.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.2	8.0	1.5	9.2	ns
		V_{CC} = 2.7 V	1.5	4.5	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.8	6.7	1.2	7.7	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 12 [4]						
		V_{CC} = 1.2 V	-	9.6	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	4.9	9.8	2.0	11.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	2.8	5.8	1.2	6.6	ns
		V_{CC} = 2.7 V	1.5	3.7	6.2	1.5	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.5	5.7	1.2	6.5	ns
t_W	pulse width	SHCP, STCP HIGH or LOW; see Figure 7 and Figure 8						
		V_{CC} = 1.65 V to 1.95 V	6.0	2.5	-	7.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.0	-	5.5	-	ns
		V_{CC} = 2.7 V	4.5	1.5	-	5.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.5	-	4.5	-	ns
		$\overline{MR}$ LOW; see Figure 11						
		V_{CC} = 1.65 V to 1.95 V	5.0	2.0	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	1.5	-	4.5	-	ns
		V_{CC} = 2.7 V	2.5	1.0	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.0	-	3.0	-	ns
t_{su}	set-up time	DS to SHCP; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	5.0	0.4	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	0.1	-	4.5	-	ns
		V_{CC} = 2.7 V	2.0	0	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	–0.1	-	2.5	-	ns
		$\overline{MR}$ to STCP; see Figure 10						
		V_{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V_{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns
		SHCP to STCP; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V_{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_h	hold time	DS to SHCP; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	1.5	0.2	-	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	0.1	-	2.0	-	ns
		V_{CC} = 2.7 V	1.5	–0.1	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	–0.2	-	1.5	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 11						
		V_{CC} = 1.65 V to 1.95 V	5.0	–2.7	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	–1.5	-	4.5	-	ns
		V_{CC} = 2.7 V	2.0	–1.0	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	–1.0	-	2.5	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Figure 7 and Figure 8						
		V_{CC} = 1.65 V to 1.95 V	80	130	-	70	-	MHz
		V_{CC} = 2.3 V to 2.7 V	100	140	-	90	-	MHz
		V_{CC} = 2.7 V	110	150	-	100	-	MHz
		V_{CC} = 3.0 V to 3.6 V	130	180	-	115	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V [5]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [6]						
		V_{CC} = 1.65 V to 1.95 V	-	50	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	45	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	44	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

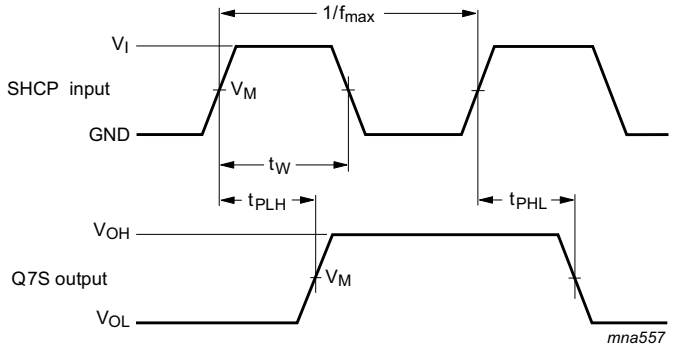
[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

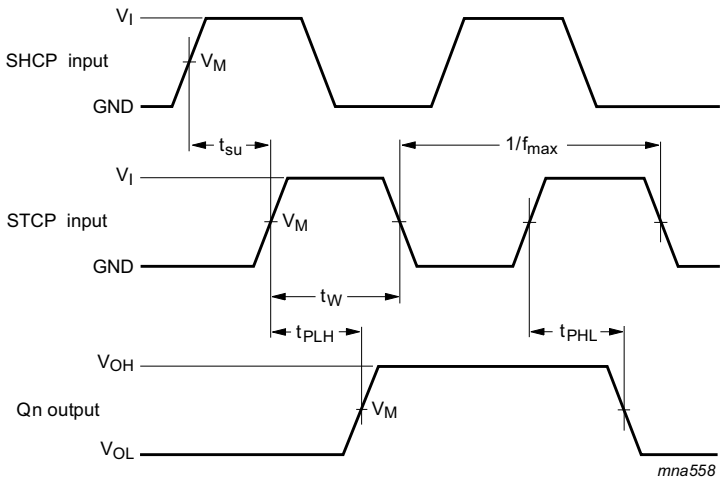
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

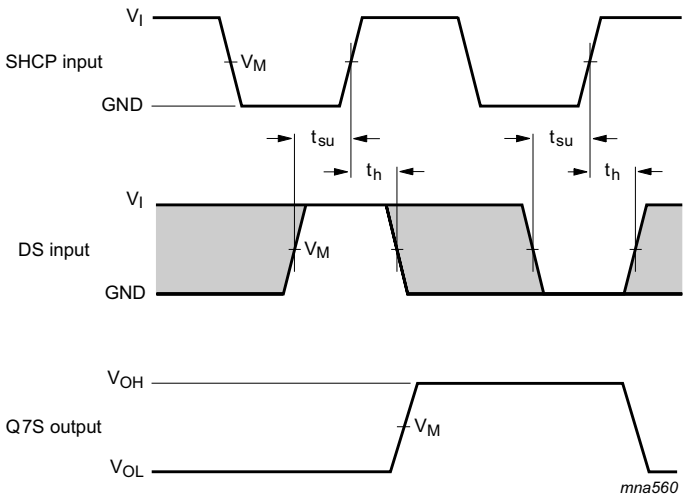
Fig 7. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 8. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time

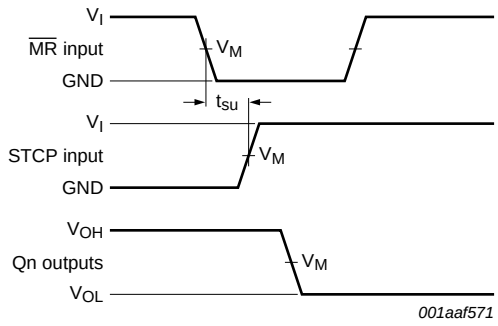


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

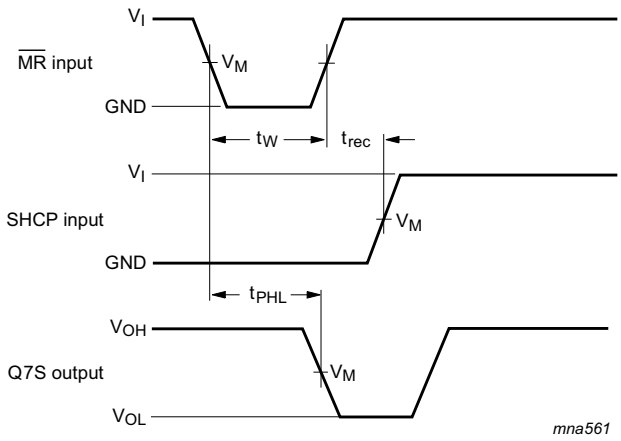
Fig 9. The data set-up and hold times for the serial data input (DS)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

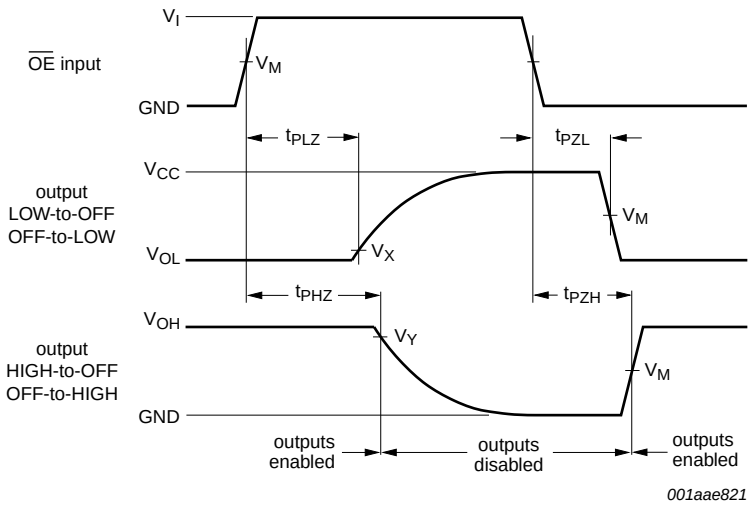
Fig 10. The master reset ($\overline{MR}$) to storage clock (STCP) set-up times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 11. The master reset ($\overline{MR}$) pulse width, the master reset to serial data output (Q7S) propagation delays and the master reset to shift clock (SHCP) recovery time



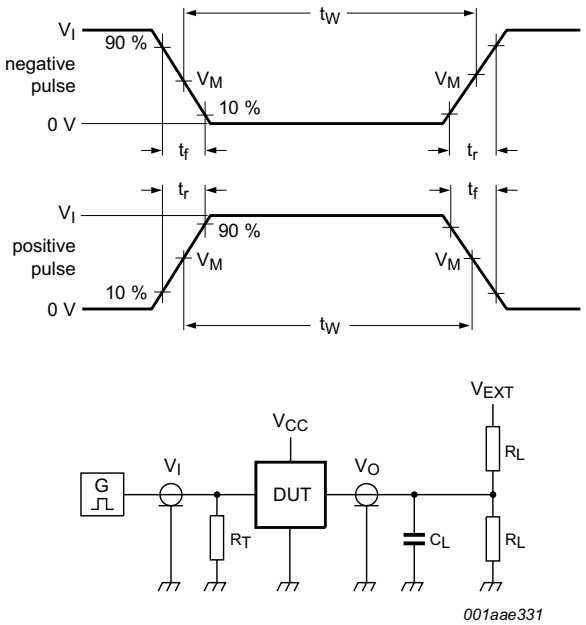
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 12. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
$V_{CC} < 2.7$ V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
$V_{CC} \geq 2.7$ V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Test data is given in Table 9. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

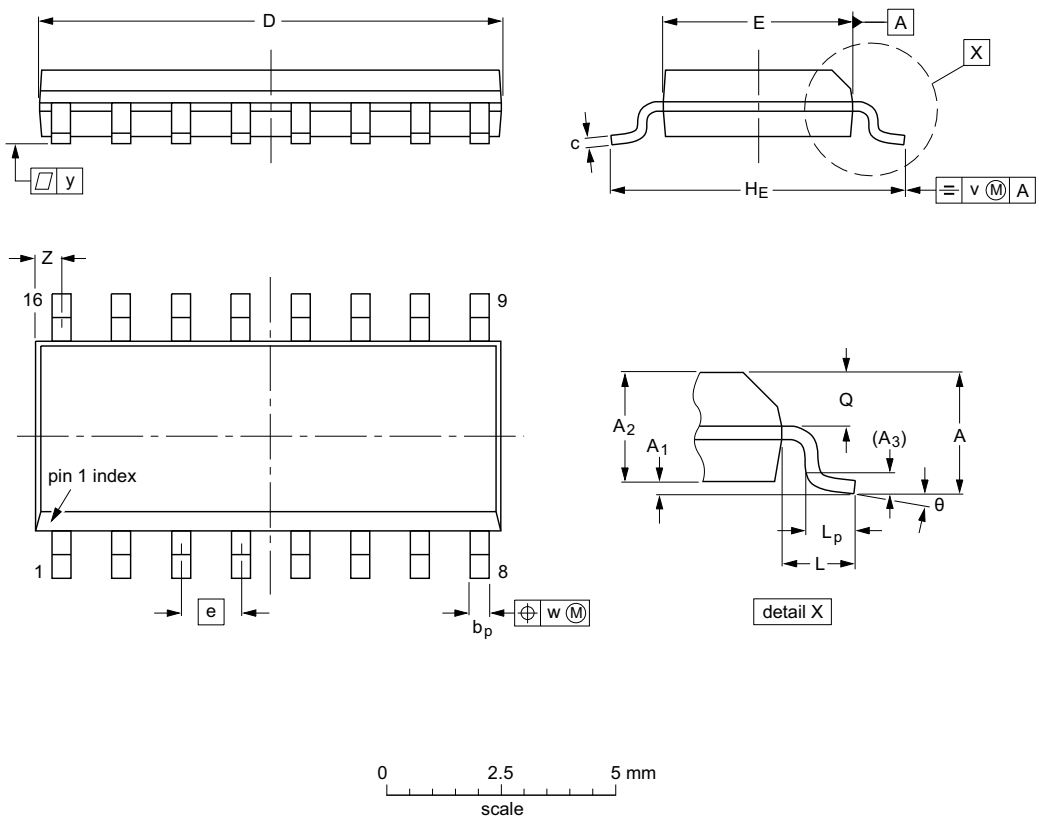
Fig 13. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

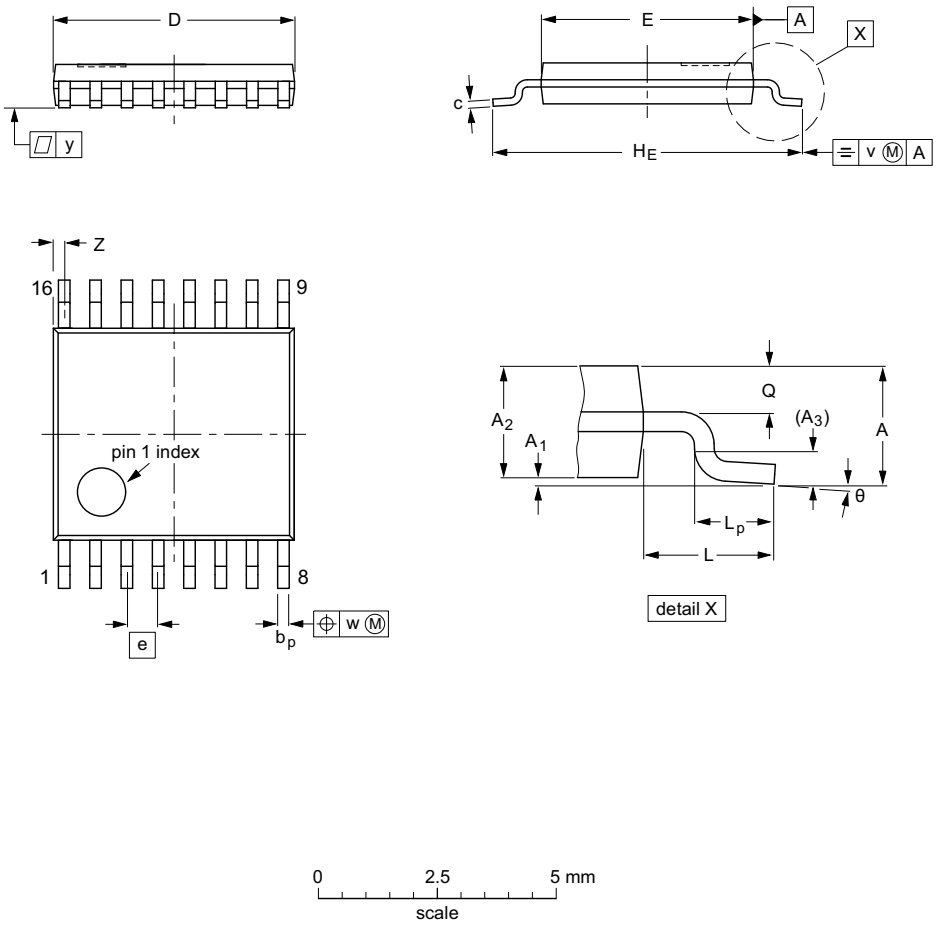
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

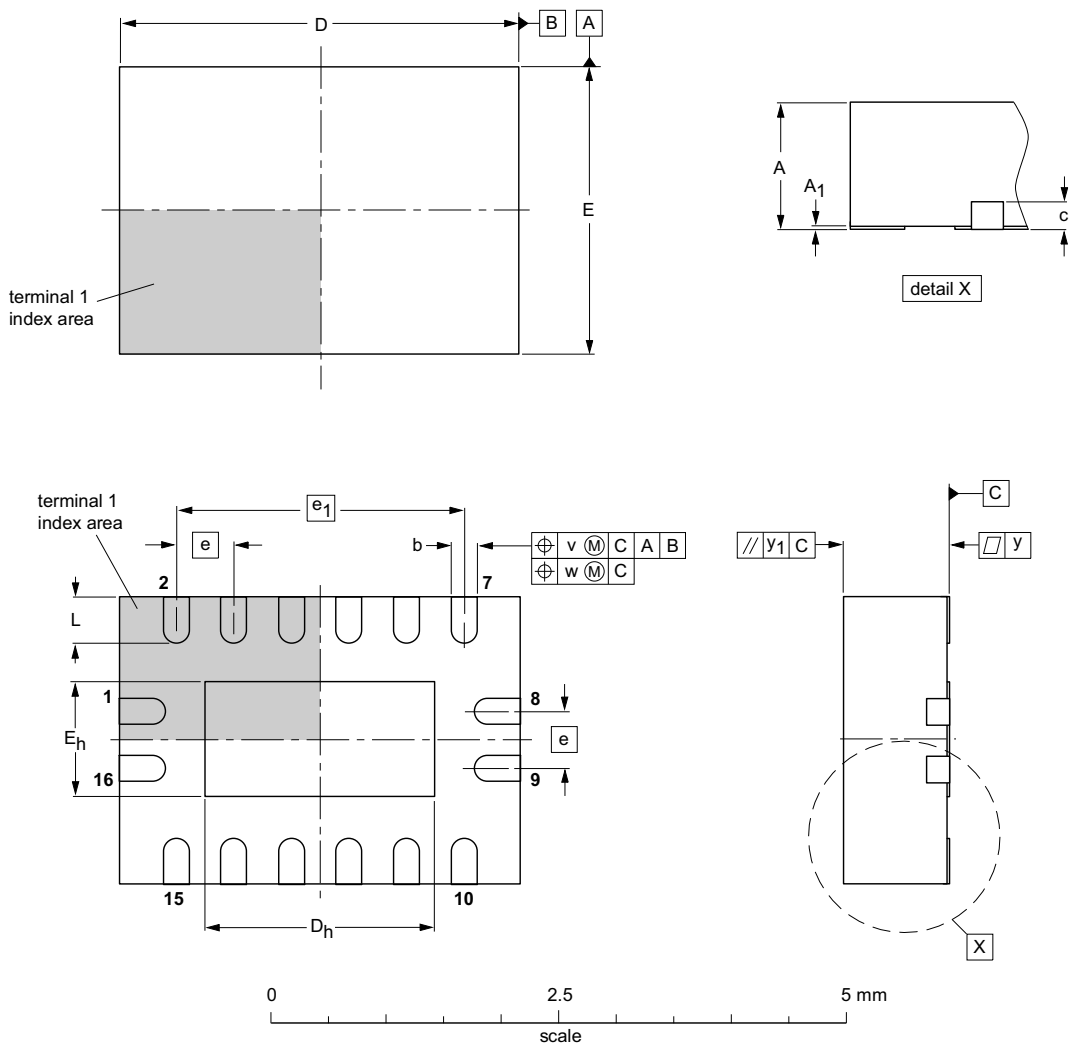
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 16. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC595A v.2	20140620	Product data sheet	-	74LVC595A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Figure note for Figure 6 added.			
74LVC595A v.1	20070529	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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