Secondary-Side Synchronous Forward Controller with PolyPhase Capability

FEATURES

- **Secondary-Side Control for Fast Transient Response**
- **Self-Starting Architecture Eliminates Need for Separate Bias Regulator**
- **Proprietary Gate Drive Encoding Scheme Reduces System Complexity**
- PolyPhase® Operation Reduces C_{IN} Requirements
- Current Mode Control Ensures Current Sharing
- PLL Fixed Frequency: 100kHz to 500kHz
- ±1% Output Voltage Accuracy
- True Remote Sense Differential Amplifier
- Power Good Output Voltage Monitor
- High Voltage Linear Regulator Controller
- Wide Supply Range: 5V to 30V
- Available in a Narrow 24-Lead SSOP Package

APPLICATIONS

- Isolated 48V Telecommunication Systems
- Internet Servers and Routers
- Distributed Power Step-Down Converters
- Automotive and Heavy Equipment

DESCRIPTION

The LTC®3706 is a PolyPhase capable secondary-side controller for synchronous forward converters. When used in conjunction with the LTC3705 gate driver and primary-side controller, the part creates a complete isolated power supply that combines the power of PolyPhase operation with the speed of secondary-side control.

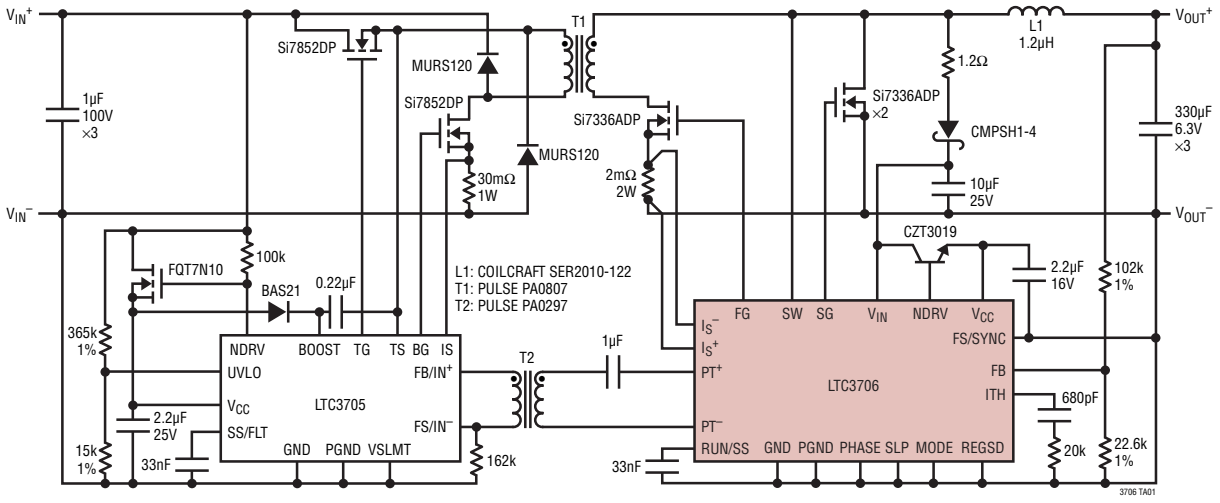
The LTC3706 has been designed to simplify the design of highly efficient, secondary-side forward converters. Working in concert with the LTC3705, the LTC3706 forms a robust, self-starting converter that eliminates the need for the separate bias regulator that is commonly used in secondary-side control applications. In addition, a proprietary scheme is used to multiplex gate drive signals and DC bias power across the isolation barrier through a single, tiny pulse transformer.

The LTC3706 provides remote sensing, accurate power good and overvoltage monitoring circuits to support precision, high current applications. A linear regulator controller with thermal protection is also provided to simplify the generation of secondary-side bias voltage.

The LTC3706 is available in a 24-lead SSOP package.

TYPICAL APPLICATION

36V-72V to 3.3V/20A Isolated Forward Converter

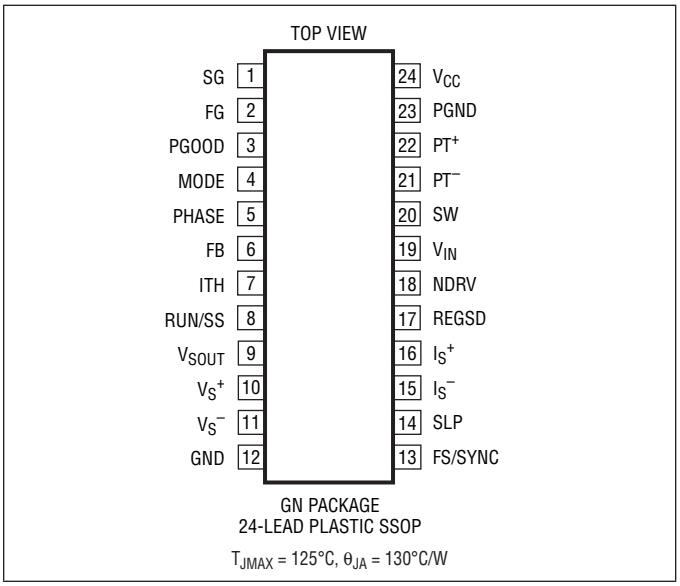


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} ..... –0.3V to 10V
V_{IN} ..... –0.3V to 33V
SW ..... –5V to 50V
NDRV ..... –0.3V to 13V
ITH, RUN/SS, V_{SOUT}, V_S^+, V_S^-, REGSD ..... –0.3V to 7V
All Other Pins ..... –0.3V to 10V
Operating Temperature Range (Note 2)
LTC3706EGN ..... –40°C to 85°C
LTC3706IGN ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3706EGN#PBF	LTC3706EGN#TRPBF	LTC3706EGN	24-Lead Plastic SSOP	–40°C to 85°C
LTC3706IGN#PBF	LTC3706IGN#TRPBF	LTC3706IGN	24-Lead Plastic SSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3706EGN	LTC3706EGN#TR	LTC3706EGN	24-Lead Plastic SSOP	–40°C to 85°C
LTC3706IGN	LTC3706IGN#TR	LTC3706IGN	24-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 7V, V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Regulated Feedback Voltage	(Note 4) ITH = 1.2V	●	0.594	0.600	0.606	V
I_{FB}	Feedback Input Current	(Note 4)			2	100	nA
$\Delta V_{FB(LINREG)}$	Feedback Voltage Line Regulation	V_{IN} = 6V to 30V, ITH = 1.2V			0.001		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	Measured in Servo Loop, ITH = 0.5V to 2V	●		–0.01	–0.1	%
V_{ISMAX}	Maximum Current Sense Threshold	R_{SENSE} Mode, 0V < V_{IS}^- < 5V V_{IS}^- = V_{CC}, 0V < V_{IS}^+ < 2V (CT Mode)		68 1.15	78 1.28	88 1.4	mV V
V_{ISOC}	Over-Current Shutdown Threshold	R_{SENSE} Mode, 0V < V_{IS}^- < 5V V_{IS}^- = V_{CC}, 0V < V_{IS}^+ < 2V (CT Mode)		87 1.45	100 1.65	113 1.85	mV V
g_m	Transconductance Amplifier g_m			2.40	2.75	3.10	mS
$I_{RUN/SS(C)}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 2V		–4	–5	–6	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current				3		µA
$V_{RUN/SS}$	RUN/SS Pin On Threshold	$V_{RUN/SS}$ Rising	●	0.4	0.45	0.5	V
$t_{ON,MIN}$	Minimum On-Time				200		ns
FG, SG R_{UP}	FG, SG Driver Pull-Up On Resistance	FG, SG Low			1.5	2.7	Ω
FG, SG R_{DOWN}	FG, SG Driver Pull-Down On Resistance	FG, SG High			1.5	2.7	Ω
PT^+, PT^- R_{UP}	PT^+, PT^- Driver Pull-Up Resistance	PT^+, PT^- Low			1.5	2.7	Ω
PT^+, PT^- R_{DOWN}	PT^+, PT^- Driver Pull-Down Resistance	PT^+, PT^- High			1.5	2.7	Ω
$\Delta V_{FB(OV)}$	Output Overvoltage Threshold	V_{FB} Rising		15	17	19	%
V_{CC} Supply							
V_{CCOP}	Operating Voltage Range			5		10	V
V_{CCREG}	Regulated Output Voltage			6.6	7.0	7.4	V
I_{CC}	Supply Current Operating Shutdown	 f_{OSC} = 200kHz (Note 5) $V_{RUN/SS}$ = GND			 4.2 240		 mA µA
V_{UVLO}	UV Lockout	V_{CC} Rising	●	4.52	4.60	4.70	V
V_{HYS}	UV Hysteresis				0.4		V
V_{IN} Supply							
V_{INOP}	Operating Voltage Range			5		30	V
I_{IN}	Supply Current Normal Mode Shutdown	 f_{OSC} = 200kHz $V_{RUN/SS}$ = GND			 900 460		 µA µA
V_{INUVLO}	UV Lockout	V_{IN} Rising	●	3.90	4.30	4.51	V
V_{INHYS}					0.2		V
V_{REGSD}	REGSD Shutdown Threshold	V_{REGSD} Rising			4		V
$g_{m,REGSD}$	REGSD Transconductance				5		µS

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 7V, V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
I_{FS}	FS/SYNC Pin Sourcing Current				20		µA
f_{LOW}	Oscillator Low Frequency Set Point	$V_{FS/SYNC}$ = GND		165	200	235	kHz
f_{HIGH}	Oscillator High Frequency Set Point	$V_{FS/SYNC}$ = VCC		247	300	353	kHz
Δf (R_{FS})	Oscillator Resistor Set Accuracy	75kΩ < $R_{FS/SYNC}$ < 175kΩ		–22		20	%
$f_{PLL(MAX)}$	Maximum PLL Sync Frequency				500		kHz
$f_{PLL(MIN)}$	Minimum PLL Sync Frequency				75		kHz
PGOOD Output							
V_{FBH}/0.6	Power Good Upper Threshold	V_{FB} Rising		115	117	119	%
V_{FBL1}/0.6	Power Good Lower Threshold	V_{FB} Rising		91.5	93	94.5	%
V_{FBL2}/0.6	Power Good Lower Threshold	V_{FB} Falling		89.5	91	92.5	%
Differential Amplifier (V_{SENSE} AMP)							
ADA	Gain	V_S^- = GND, 1V ≤ V_S^+ ≤ 5V		0.990	1	1.010	V/V
CMRR DA	Common Mode Rejection Ratio				75		dB
R_{IN}	Input Resistance				80		kΩ
f_{BW}	–3dB Bandwidth				3		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3706E is guaranteed to meet the performance specifications over the 0°C to 85°C operating temperature range. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3706I is guaranteed and tested over the full –40°C to 85°C operating temperature range.

Note 3: Junction temperature T_J (in °C) is calculated from the ambient temperature T_A and the average power dissipation P_D (in Watts) by the formula:

$$T_J = T_A + \theta_{JA} \bullet P_D$$

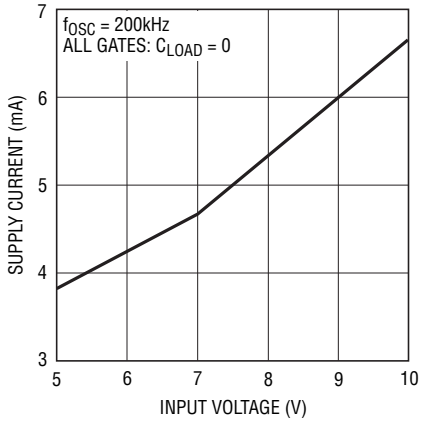
Refer to the Applications Information section for details.

Note 4: The LTC3706 is tested in a feedback loop that servos V_{FB} to a voltage near the internal 0.6V reference voltage to obtain the specified ITH voltage (V_{ITH} = 1.2V).

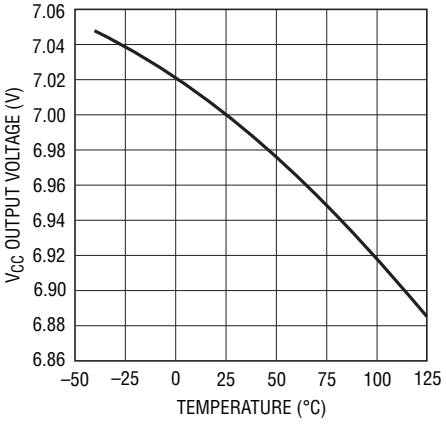
Note 5: Operating supply current is measured in test mode. Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency. See the Typical Performance Characteristics section.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

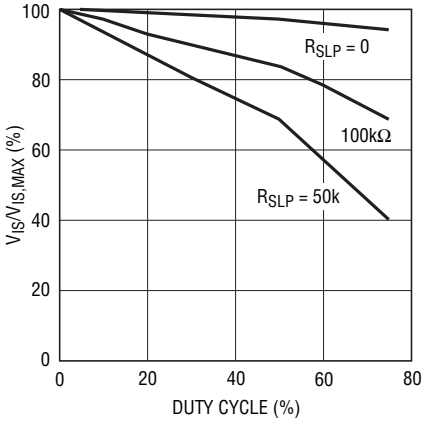
V_{CC} Supply Current vs Input Voltage



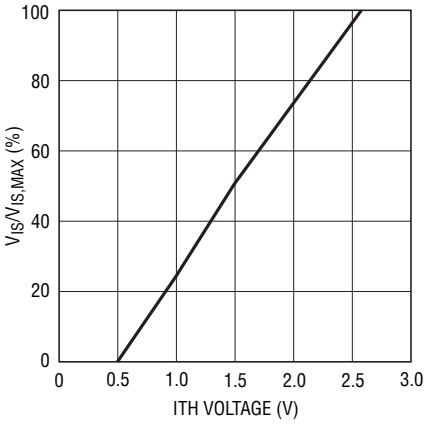
V_{CC} Regulator Output Voltage vs Temperature



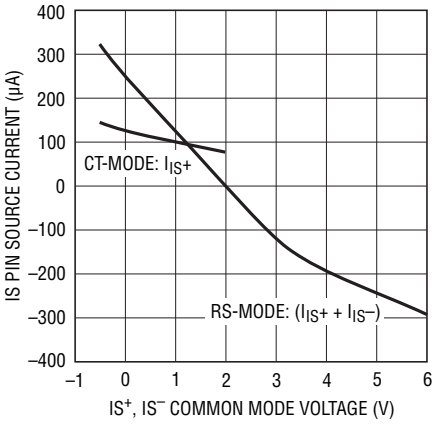
Maximum Current Sense Threshold vs Duty Cycle



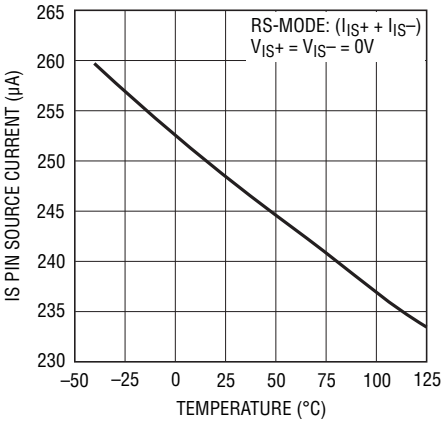
Maximum Current Sense Threshold vs ITH Voltage



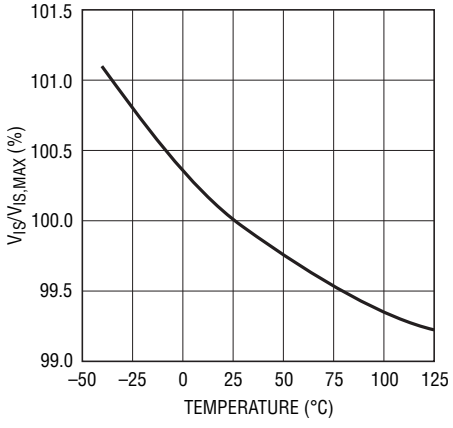
IS Pins Source Current



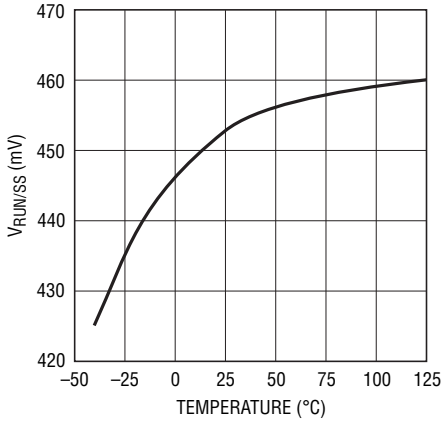
IS Pins Source Current vs Temperature



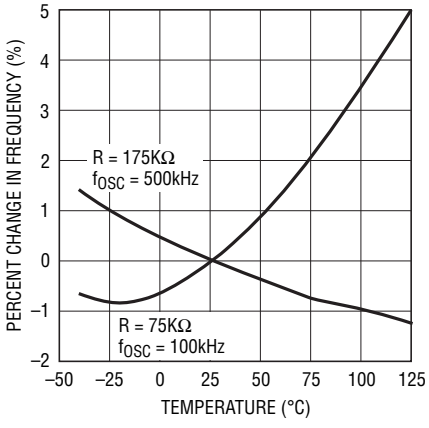
Maximum Current Sense Threshold vs Temperature



RUN/SS ON Threshold vs Temperature

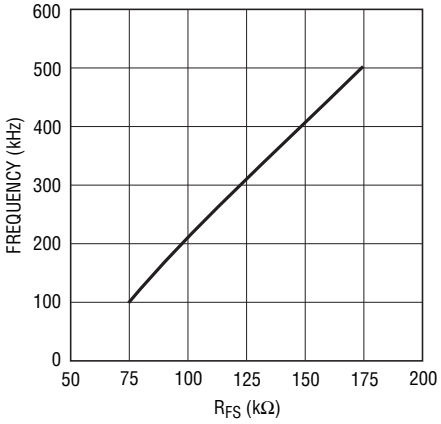


Oscillator Frequency vs Temperature

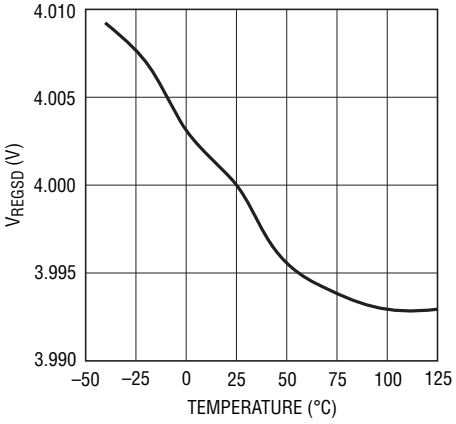


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

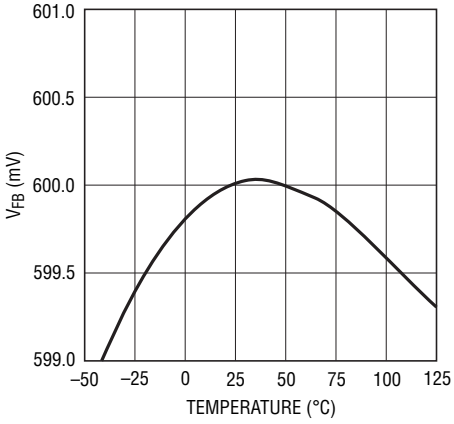
Oscillator Frequency vs R_{FS}



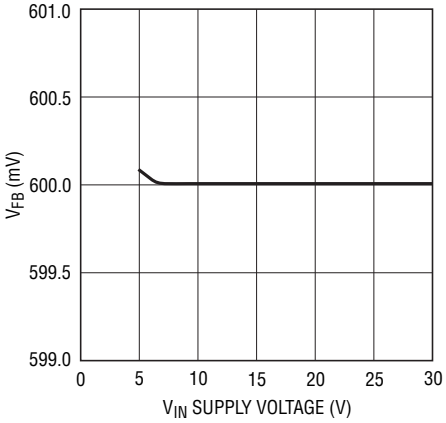
REGSD Shutdown Threshold vs Temperature



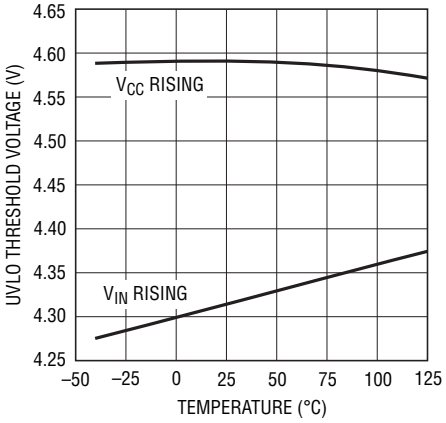
FB Voltage vs Temperature



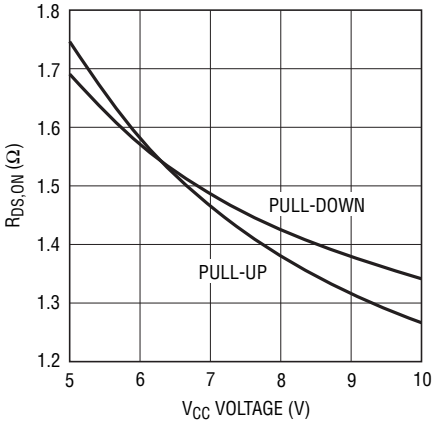
FB Voltage Line Regulation



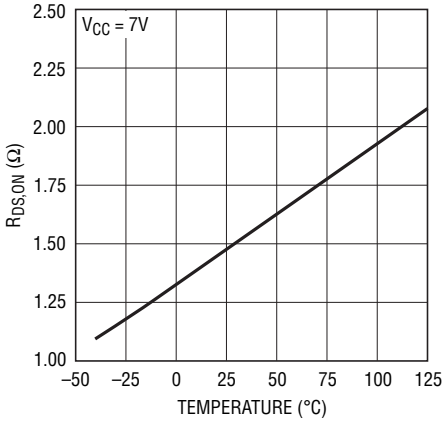
Undervoltage Lockout vs Temperature



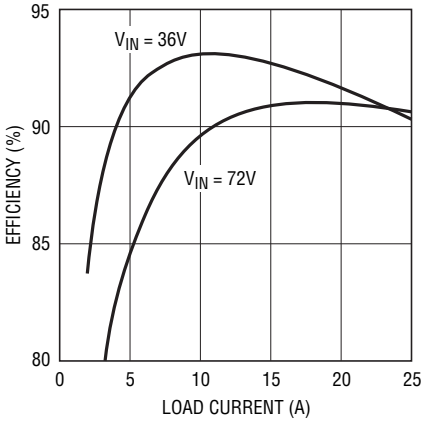
Gate Driver On-Resistance vs V_{CC}



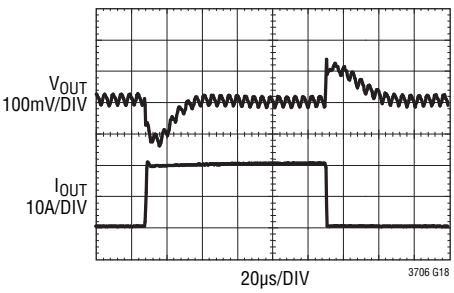
Gate Driver On-Resistance vs Temperature



Efficiency (Figure 5)



Load Step (Figure 5)



V_{IN} = 48V
V_{OUT} = 3.3V
LOAD STEP = 0A TO 20A

PIN FUNCTIONS

SG (Pin 1): Gate Drive for the "Synchronous" MOSFET.

FG (Pin 2): Gate Drive for the "Forward" MOSFET.

PGOOD (Pin 3): Open-Drain Power Good Output. The FB pin is monitored to ensure that the output is in regulation. When the output is not in regulation, the PGOOD pin is pulled low.

MODE (Pin 4): Tie to either GND or V_{CC} to set the maximum duty cycle at either 50% or 75% respectively. Tie to ground through either a 200k or 100k resistor (50% or 75% maximum duty cycle) to disable pulse encoding. In this mode, normal PWM signals will be generated at the PT^+ pin, while a clock signal is generated at the PT^- pin.

PHASE (Pin 5): Control Input to the Phase Selector. This pin determines the phasing of the controller CLK relative to the synchronizing signal at the FS/SYNC pin.

FB (Pin 6): The Inverting Input of the Main Loop Error Amplifier.

ITH (Pin 7): The Output of the Main Loop Error Amplifier. Place compensation components between the ITH pin and GND.

RUN/SS (Pin 8): Combination Run Control and Soft-Start Inputs. A capacitor to ground sets the ramp time of the output voltage. Holding this pin below 0.4V causes the IC to shut down all internal circuitry.

V_{SOUT}, V_S^+, V_S^- (Pins 9, 10, 11): V_{SOUT} is the output of a precision, unity-gain differential amplifier. Tie V_S^+ and V_S^- to the output of the main DC/DC converter to achieve true remote differential sensing. This allows DCR error effects to be minimized.

GND (Pin 12): Signal Ground.

FS/SYNC (Pin 13): Combination Frequency Set and SYNC pin. Tie to GND or V_{CC} to run at 200kHz and 300kHz respectively. Place a single resistor to ground at this pin to set the frequency between 100kHz and 500kHz. To synchronize, drive this pin with a clock signal to achieve PLL synchronization from 75kHz to 500kHz. Sources 20µA of current.

SLP (Pin 14): Slope Compensation Input. Place a single resistor to ground to set the desired amount of slope compensation.

I_S^- (Pin 15): Negative Input to the Current Sense Circuit. When using current sense transformers, this pin may be tied to V_{CC} for single-ended sensing with a 1.28V maximum current trip level.

I_S^+ (Pin 16): Positive Input to the Current Sense Circuit. Connect to the positive end of a current sense resistor or to the output of a current sense transformer.

REGSD (Pin 17): This pin is used to prevent overheating of the external linear regulator pass device that generates the V_{CC} supply voltage from the V_{IN} voltage. A current proportional to the voltage across the external pass device flows out of this pin. The IC shuts down the linear regulator when the voltage on this pin exceeds 4V. Place a resistor (or a resistor and capacitor in parallel) between this pin and GND to limit the temperature rise of the external pass device.

NDRV (Pin 18): Drive Output for the External Pass Device of the V_{CC} Linear Regulator. Connect to the base (NPN) or gate (NMOS) of an external N-type device.

V_{IN} (Pin 19): Connect to a higher voltage bias supply, typically the output of a peak detected bias winding. When not used, tie together with the V_{CC} and NDRV pins.

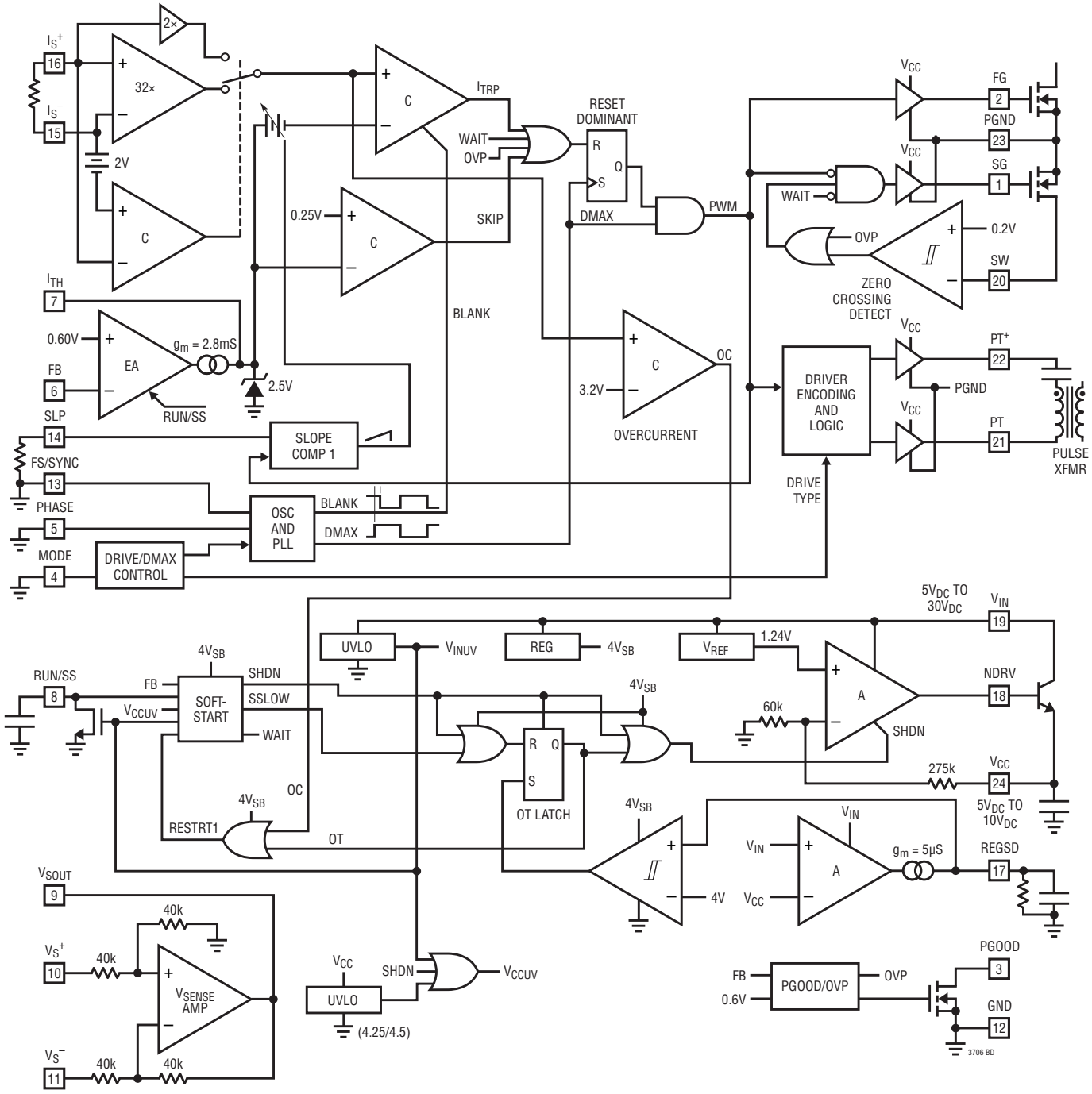
SW (Pin 20): Connect to the drain of the "synchronous" MOSFET. This input is used for adaptive shoot-through prevention and leading edge blanking.

PT^-, PT^+ (Pins 21, 22): Pulse Transformer Driver Outputs. For most applications, these connect to a pulse transformer (with a series DC blocking capacitor). The PWM information is multiplexed together with DC power and sent through a single pulse transformer to the primary side. This information may be decoded by the LTC3705 gate driver and primary-side controller.

PGND (Pin 23): Gate Driver Ground Pin.

V_{CC} (Pin 24): Main V_{CC} Input for all Driver and Control Circuitry.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3706 is designed to work in a constant frequency, current mode 2-transistor forward converter. During normal operation, the primary-side MOSFETs (both top and bottom) are "clocked" on together with the forward MOSFET on the secondary side. This applies the reflected input voltage across the inductor on the secondary side. When the current in the inductor has ramped up to the peak value as commanded by the voltage on the ITH pin, the current sense comparator is tripped, turning off the primary-side and forward MOSFETs. To avoid turning on the synchronous MOSFET prematurely and causing shoot-through, the voltage on the SW pin is monitored. This voltage will usually fall below 0V soon after the primary-side MOSFETs have turned completely off. When this condition is detected, the synchronous MOSFET is quickly turned on, causing the inductor current to ramp back downwards. The error amplifier senses the output voltage, and adjusts the ITH voltage to obtain the peak current needed to maintain the desired main-loop output voltage. The LTC3706 always operates in a continuous current, synchronous switching mode. This ensures a rapid transient response as well as a stable bias supply voltage at light loads. A maximum duty cycle (either 50% or 75%) is internally set via clock dividers to prevent saturation of the main transformer. In the event of an overvoltage on the output, the synchronous MOSFET is quickly turned on to help protect critical loads from damage.

Gate Drive Encoding

Since the LTC3706 controller resides on the secondary side of an isolation barrier, communication to the primary-side power MOSFETs is generally done through a transformer. Moreover, it is often necessary to generate a low voltage bias supply for the primary-side gate drive circuitry. In order to reduce the number of isolated windings present in the system, the LTC3706 uses a proprietary scheme to encode the PWM gate drive information and multiplex it together with bias power for the primary-side drive and control, using a single pulse transformer. Note that, unlike optoisolators and other modulation techniques, this multiplexing scheme does not introduce a significant time delay into the system.

For most forward converter applications, the PT^+ and PT^- outputs will contain a pulse-encoded PWM signal. These outputs are driven in a complementary fashion with an essentially constant 50% duty cycle. This results in a stable volt-second balance as well as an efficient transfer of bias power across the pulse transformer. As shown in Figure 1, the beginning of the positive half-cycle coincides with the turn-on of the primary-side MOSFETs. Likewise, the beginning of the negative half-cycle coincides with the maximum duty cycle (forced turn-off of primary switches). At the appropriate time during the positive half-cycle, the end of the on-time (PWM going LOW) is signaled by briefly applying a zero volt differential across the pulse transformer. Figure 1 illustrates the operation of this multiplexing scheme.

The LTC3705 primary-side controller and gate driver will decode this PWM information as well as extract the power needed for primary-side gate drive.

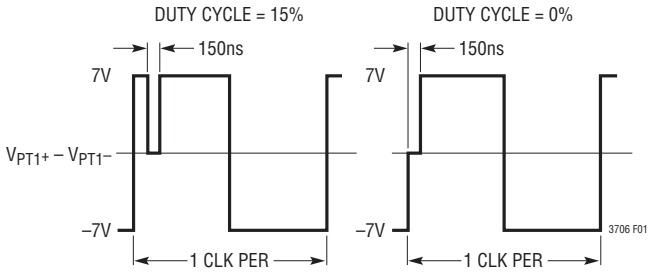


Figure 1. Gate Drive Encoding Scheme (V_{MODE} = GND)

OPERATION

Self-Starting Architecture

When the LTC3706 is used in conjunction with the LTC3705 primary-side controller and gate driver, a complete self-starting isolated supply is formed. When input voltage is first applied in such an application, the LTC3705 will begin switching in an "open-loop" fashion, causing the main output to slowly ramp upwards. This is the primary-side soft-start mode. On the secondary side, the LTC3706 derives its operating bias voltage from a peak-charged capacitor. This peak-charged voltage will rise more rapidly than the main output of the converter, so that the LTC3706 will become operational well before the output voltage has reached its final value.

When the LTC3706 has adequate operating voltage, it will begin the procedure of assuming control from the primary side. To do this, it first measures the voltage on the power supply's main output and then automatically advances its own soft-start voltage to correspond to the main output voltage. This ensures that the output voltage increases monotonically as the soft-start control is transferred from primary to secondary. The LTC3706 then begins sending PWM signals to the LTC3705 on the primary side through a pulse transformer. When the LTC3705 has detected a stable signal from the secondary controller, it transfers control of the primary switches over to the LTC3706, beginning the secondary-side soft-start mode. The LTC3706 continues in this mode until the output voltage has ramped up to its final value. If for any reason, the LTC3706 either stops sending (or initially fails to send) PWM information to the LTC3705, the LTC3705 will detect a FAULT and initiate a soft-start retry. (See the LTC3705 data sheet.)

Slope Compensation

Slope compensation is added at the input of the PWM comparator to improve stability and noise margin of the peak current control loop. The amount of slope compensation can be selected from one of five preprogrammed values using the SLP pin as shown in Table 1. Note that the amount of slope compensation doubles when the duty cycle exceeds 50%.

Table 1

SLP PIN	SLOPE (D < 0.5)	SLOPE (D > 0.5)
GND	$0.05 \bullet I_{SMAX} \bullet f_{OSC}$	$0.1 \bullet I_{SMAX} \bullet f_{OSC}$
V_{CC}	None	None
400kΩ to GND	$0.1 \bullet I_{SMAX} \bullet f_{OSC}$	$0.2 \bullet I_{SMAX} \bullet f_{OSC}$
200kΩ to GND	$0.15 \bullet I_{SMAX} \bullet f_{OSC}$	$0.3 \bullet I_{SMAX} \bullet f_{OSC}$
100kΩ to GND	$0.25 \bullet I_{SMAX} \bullet f_{OSC}$	$0.5 \bullet I_{SMAX} \bullet f_{OSC}$
50kΩ to GND	$0.5 \bullet I_{SMAX} \bullet f_{OSC}$	$1.0 \bullet I_{SMAX} \bullet f_{OSC}$

In Table 1 above, I_{SMAX} is the maximum current limit, and f_{OSC} is the switching frequency.

Current Sensing and Current Limit

For current sensing, the LTC3706 supports either a current sense resistor or a current sense transformer. The current sense resistor may either be placed in series with the inductor (either high side or ground lead sensing), or in the source of the "forward" switch. If a current sense transformer is used, the I_S^- input should be tied to V_{CC} and the I_S^+ pin to the output of the current sense transformer. This causes the gain of the internal current sense amplifier to be reduced by a factor of 16×, so that the maximum current sense voltage (current limit) is increased from 78mV to 1.28V. An internal, adaptive leading edge blanking circuit ensures clean operation for "switch" current sensing applications.

Current limit is achieved in the LTC3706 by limiting the maximum voltage excursion of the error signal (ITH voltage). Note that if slope compensation is used, the precise value at which current limit occurs will be a function of duty cycle (See the Typical Performance Characteristics section). If a short circuit is applied, an independent overcurrent comparator may be tripped. In this case, the LTC3706 will enter a "hiccup" mode using the soft-start circuitry.

OPERATION

Frequency Setting and Synchronization

The LTC3706 uses a single pin to set the operating frequency, or to synchronize the internal oscillator to a reference clock with an on-chip phase-locked loop (PLL). The FS pin may be tied to GND, V_{CC} or have a single resistor to GND to set the switching frequency. If a clock signal (>2V) is detected at the FS pin, the LTC3706 will automatically synchronize to the rising edge of the reference clock. Table 2 summarizes the operation of the FS pin.

For synchronization between multiple LTC3706s, the PT^+ pin of one LTC3706 can be used as a master clock reference and tied to the FS pin of the other LTC3706s.

Table 2

FS PIN	SWITCHING FREQUENCY
GND	200kHz
V_{CC}	300kHz
R_{FS} to GND	f_{OSC} (Hz) = $4R_{FS}$ – 200k
Reference Clock	$f_{OSC} = f_{REF}$ (75kHz to 500kHz)

This will cause all LTC3706's to operate at the same frequency. The phase angle of each LTC3706 that is being synchronized can be set by using the PHASE pin. This pin can be tied to GND, V_{CC} or have a single resistor to V_{CC} to set the phase angle (delay) of the internal oscillator relative to the incoming sync signal on the FS pin. Any one of five preset values can be selected as summarized in Table 3.

Table 3

PHASE PIN	LTC3706 PHASE DELAY
GND	0°
V_{CC}	180°
226kΩ to V_{CC}	60°
113kΩ to V_{CC}	90°
56.2kΩ to V_{CC}	120°

Soft-Start

The soft-start circuitry has five functions: 1) to provide a shutdown, 2) to provide a smooth ramp on the output voltage during start-up, 3) to limit the output current in a short-circuit situation by entering a hiccup mode, 4) to limit the maximum power dissipation in the external linear regulator via the REGSD pin, and 5) to communicate fault and shutdown information between multiple LTC3706s in a PolyPhase application.

When the RUN/SS pin is pulled to GND, the chip is placed into shutdown mode. If this pin is released, the RUN/SS pin is initially charged with a 50µA current source. After the RUN/SS pin gets above 0.5V, the chip is enabled. At the instant that the LTC3706 is first enabled, the RUN/SS voltage is rapidly preset to a voltage that will correspond to the main output voltage of the DC/DC converter. (See the Self-Starting Architecture section.) After this preset interval has completed, the normal soft-start interval begins and the charging current is reduced to 5µA. The external soft-start voltage is used to internally ramp up the 0.6V reference (positive) input to the error amplifier. When fully charged, the RUN/SS voltage remains at 3V.

In the event that the sensed switch or inductor current exceeds the overcurrent trip threshold, an internal fault latch is tripped. This latch is also tripped when the REGSD voltage exceeds 4V (see the Linear Regulator section). When such a fault is detected, the LTC3706 immediately goes to zero duty cycle and initiates a soft-start retry. Prior to discharging the soft-start capacitor, however, the LTC3706 first puts a voltage pulse on the RUN/SS pin, which trips the fault latch in any other LTC3706 that shares the RUN/SS. This ensures an orderly shutdown of all phases in a PolyPhase application. After the soft-start capacitor is fully discharged, the LTC3706 attempts a restart. If the fault is persistent, the system enters a "hiccup" mode.

OPERATION

Note that in self-starting secondary-side control applications (with the LTC3705), the presence of the LT3706 bias voltage is dependent upon the regular switching of the primary-side MOSFETs. Therefore, depending on the details of the application circuit, the LTC3706 may lose its bias voltage after a fault has been detected and before completing a soft-start retry. In this case, the "hiccup-mode" operation is actually governed by the LTC3705 soft-start circuitry. (See the LTC3705 data sheet.)

Drive Mode and Maximum Duty Cycle

Although the LTC3706 is primarily intended to be used with the LTC3705 in 2-transistor forward applications, the MODE pin provides the flexibility to use the LTC3706 in a wide variety of additional applications. This pin can be used to defeat the gate drive encoding scheme, as well as change the maximum duty cycle from its default value of 50%. The use of the MODE pin is summarized in Table 4.

When the gate drive encoding scheme is defeated, a standard PWM-style signal will be present at the PT^+ pin and a reference clock (in phase with the PWM signal) will be present at the PT^- pin. These outputs can be used in "standalone" applications (without the LTC3705) to drive the gates of MOSFETs in a conventional manner.

Table 4

MODE PIN	PT^+/PT^- Mode (MAX DUTY CYCLE)	INTENDED APPLICATION
GND	Encoded PWM (D_{MAX} = 50%)	2-Switch Forward with LTC3705
V_{CC}	Encoded PWM (D_{MAX} = 75%)	1-Switch Forward
200kΩ to GND	Standard PWM (D_{MAX} = 50%)	2-Switch Forward Standalone
100kΩ to GND	Standard PWM (D_{MAX} = 75%)	1-Switch Forward Standalone

Power Good/Overvoltage Protection

This circuit monitors the voltage on the FB input. The open-drain PGOOD output will be logic high if the voltage on the FB pin is within +17%/–7% of 0.6V. If the voltage on the FB pin exceeds 117% of 0.6V (0.7V), an overvoltage (OVP) is detected. For overvoltage protection, the secondary-side synchronous MOSFET is turned on while all other MOSFETs are turned off. This protection mode is not latched, so that the overvoltage detection is cleared if the FB voltage falls below 115% of 0.6V (0.69V).

Linear Regulator Operation

The LTC3706 provides a linear regulator controller that drives an external N-type pass device. This controller is used to create a 7V DC bias from the peak-charged secondary bias voltage (8V to 30V). Internal divider resistors are used to establish a regulation voltage of 7V at the V_{CC} pin. An auxiliary bias supply with a regulated voltage greater than 7V may be applied to the V_{CC} pin to bypass (bootstrap) the linear regulator. This improves efficiency and also helps to avoid overheating the linear regulator pass device.

Thermal protection for the linear regulator pass device is also provided by means of the REGSD pin. A current is sourced from this pin that is proportional to the voltage across the linear regulator pass device ($V_{IN} – V_{CC}$). Since the V_{CC} load current is essentially constant for a given switching frequency and choice of power MOSFETs, the power dissipated in the external pass device will only vary with the voltage across it. Thus, a single resistor may be placed between the REGSD pin and GND to develop a voltage that is proportional to the power in the external pass device. An additional parallel capacitor can also be used to account for the thermal time constant associated with the external pass device itself. When the voltage on the REGSD pin exceeds 4V, an overtemperature fault occurs and the LTC3706 attempts a soft-start retry.

OPERATION

Slave Mode Operation

When two or more LTC3706 devices are used in PolyPhase systems, one device becomes the "master" controller, while the others are used as "slaves." Slave mode is activated by connecting the FB pin to V_{CC}. In this mode, the ITH pin becomes a high impedance input, allowing it to be driven by the master controller. In this way, equal inductor currents are established in each of the individual phases. Also, in slave mode the soft-start charge/discharge currents are disabled, allowing the master device to control the charging and discharging of the soft-start capacitor.

APPLICATIONS INFORMATION

Start-Up Considerations

In self-starting applications, the LTC3705 will initially begin the soft-start of the converter in an open-loop fashion. After bias is obtained on the secondary side, the LTC3706 assumes control and completes the soft-start interval. In order to ensure that control is properly transferred from the LTC3705 (primary-side) to the LTC3706 (secondary-side), it is necessary to limit the rate of rise on the primary-side soft-start ramp so that the LTC3706 has adequate time to wake up and assume control before the output voltage gets too high. This condition is satisfied for many applications if the following relationship is maintained:

$$C_{SS,SEC} \leq C_{SS\ PRI}$$

However, care should be taken to ensure that soft-start transfer from primary-side to secondary-side is completed well before the output voltage reaches its target value. A good design goal is to have the transfer completed when the output voltage is less than one-half of its target value. Note that the fastest output voltage rise time during primary-side soft-start mode occurs with maximum input voltage and minimum load current.

The open-loop start-up frequency on the LTC3705 is set by placing a resistor from the FB/IN$^+$ pin to GND. Although the exact start-up frequency on the primary side is not critical, it is generally good practice to set this approximately equal to the operating frequency on the secondary side. The FS/IN$^-$ start-up resistor for the LTC3705 may be selected using the following:

$$f_{PRI}(Hz) = \frac{3.2 \bullet 10^{10}}{R_{FS/IN^-} + 10k}$$

In the event that the secondary-side circuitry fails to properly start up and assume control of switching, there are several fail-safe mechanisms to help avoid overvoltage conditions. First, the LTC3705 contains a volt-second clamp that will keep the primary-side duty cycle at a level that cannot produce an overvoltage condition. Second, the LTC3705 contains a time-out feature that will detect a FAULT if the LTC3706 fails to start up and deliver PWM signals to the primary side. Finally, the LTC3706 has an independent overvoltage detection circuit that will crowbar the output of the DC/DC converter using the synchronous MOSFET switch.

In the event that a short circuit is applied to the output of the DC/DC converter prior to start-up, the LTC3706 will generally not receive enough bias voltage to operate. In this case, the LTC3705 will detect a FAULT for one of two reasons: 1) the start-up time-out feature will be activated since the LTC3706 never sends signals to the primary side or 2) the primary-side overcurrent circuit will be tripped because of current buildup in the output inductor. In either case, the LTC3705 will initiate a shutdown followed by a soft-start retry. See the LTC3705 data sheet for further details.

APPLICATIONS INFORMATION

Bias Supply Generation

Figure 2 shows a commonly used method of developing a V_{CC} bias supply for the LTC3706. During start-up, bias winding 1 uses a peak detection method to rapidly develop a V_{IN} voltage for the LTC3706, which in turn drives the linear regulator that generates the V_{CC} voltage (7V). When the main output of the converter is in regulation, winding 2 (configured as a forward-style output) is designed to produce a regulated auxiliary voltage of approximately 7.5V to 8.5V. Since the auxiliary voltage is greater than that of the linear regulator, the linear regulator will effectively be shut down. Note that the output inductor L1 must be adequately large so that its ripple current is continuous given the amount of V_{CC} load current, thereby providing a stable output voltage.

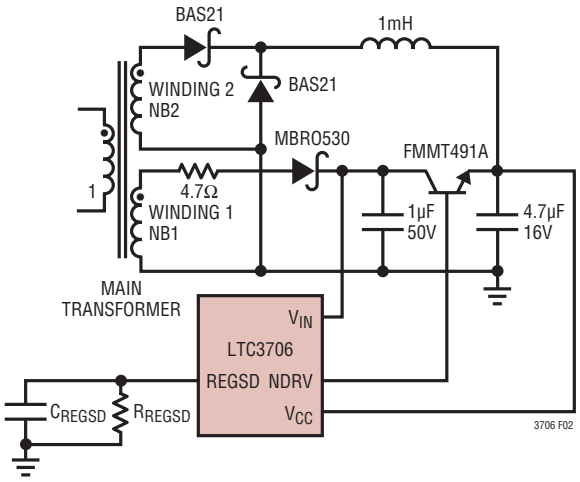


Figure 2. Typical Bias Supply Configuration

The turns ratio (NB1) of the bias winding 1 should be chosen to ensure that there is adequate voltage to operate the LTC3706 over the entire range for the DC/DC converter's input bus voltage (V_{BUS}). This may be calculated using:

$$NB1 = \frac{V_{CC(MIN)} + 1.5V}{V_{BUS(MIN)}}$$

$V_{CC(MIN)}$ can be as low as 5V (if this provides adequate gate drive voltage to maintain acceptable efficiency) or as high as 7V. For $V_{CC(MIN)}$ = 6V and V_{BUS} = 36V to 72V, this would mean a turns ratio of NB1 ≈ 0.21 and a V_{IN} voltage range at the LTC3706 of 7.5V to 15V.

Using the bias circuit of Figure 2, the linear regulator would normally operate only for a brief interval during the initial soft-start ramp of the main output voltage. Under some fault conditions (e.g., output overload), the auxiliary voltage produced by bias winding 2 may decrease below 7V, causing the linear regulator to again supply the V_{CC} bias current. Since the amount of power dissipation in the linear regulator pass device may be quite high, it can take considerable board area when the linear regulator pass device is sized to handle this power continuously. As an alternative, the REGSD pin may be used to effectively detect an overtemperature condition on the linear regulator pass device and generate a shut down (soft-start retry) before overheating occurs. This allows for the use of a small (e.g., SOT-23) package for the linear regulator pass device.

APPLICATIONS INFORMATION

The REGSD resistor should be selected based upon the steady-state (DC) thermal impedance of the linear regulator pass device.

$$R_{REGSD} = 960k \frac{\theta_{JA} \bullet I_{CC(MAX)}}{T_{RISE(MAX)}}$$

where θ_{JA} is the DC thermal impedance of the linear regulator pass device and $T_{RISE(MAX)}$ is the maximum junction temperature rise desired for the pass device. The value for $I_{CC(MAX)}$ depends heavily on the particular switching MOSFETs used, as well as on the details of overall system design. Note that it may include the bias current associated with the primary-side gate driver and controller, if the LTC3705 is being used. The value for I_{CC} is best determined experimentally and then guard banded appropriately to establish $I_{CC(MAX)}$. Using the Typical Application circuit on the first page of this data sheet as an example, if a SOT-23 MOSFET is chosen, we might have θ_{JA} = 150°C/W, $t_{RISE(MAX)}$ = 50°C and $I_{CC(MAX)}$ = 35mA so that $R_{REGSD} \approx 100k\Omega$. In this case, the linear regulator can run continuously for any V_{IN} voltage that is less than:

$$4V = (V_{IN} - V_{CC})(5\mu s)(R_{REGSD})$$

$$V_{IN(MAX)} = \left(\frac{640k}{R_{REGSD}}\right) + 7V$$

or 13.4V. In addition, a capacitor may be added in parallel with the REGSD resistor to delay the thermal shutdown and thereby account for the thermal time constant of the pass device. When using a delay capacitor, care must be taken to ensure that the safe operating area (SOA) of the pass device is not exceeded. The capacitor should be chosen to provide a time constant that is somewhat faster than the thermal time constant of the pass device in the system. This technique will allow for much higher transient power dissipation, which is particularly useful in larger (PolyPhase) systems that have a higher V_{CC} bias current. For the above SOT-23 example, a capacitor C_{REGSD} = 1µF provides a linear regulator shutdown delay given by:

$$t_{SHDN} = (C_{REGSD})(R_{REGSD}) \ln\left(\frac{1}{1 - \frac{640k}{(V_{IN} - 7)R_{REGSD}}}\right)$$

or 33ms at V_{IN} = 30V. This delay provides ample time for linear regulator operation during soft-start, while providing protection for the pass device during fault conditions such as input overvoltage or output overcurrent.

Current Sensing

The LTC3706 provides considerable flexibility in current sensing techniques. It supports two main methods: 1) resistive current sensing and 2) current transformer current sensing. Resistive current sensing is generally simpler, smaller and less expensive, while current transformer sensing is more efficient and generally appropriate for higher (>20A) output currents. For resistive current sensing, the sense resistor may be placed in any one of three different locations: high side inductor, low side inductor or low side switch, as shown in Figure 3. Sensing the inductor

APPLICATIONS INFORMATION

current (high side or low side) is generally less noisy but dissipates more power than sensing the switch current (Figures 3a and 3b). High side inductor current sensing provides a more convenient layout than low side (no split ground plane), but can only be used for output voltages up to 5.5V, due to the common mode limitations of the current sense inputs (I_S^+ and I_S^-). For most applications, low side switch current sensing will be a good solution (Figure 3c).

For high current applications where efficiency (power dissipation) is very important, a current sense transformer may be used. As shown in Figure 3d, the I_S^- pin should be tied off to V_{CC} when a current sense transformer is used. This causes the I_S^+ pin to become a single ended (nondifferential) current sense input with a maximum current sense voltage of 1.28V. Figure 3d shows a typical application circuit using a current transformer.

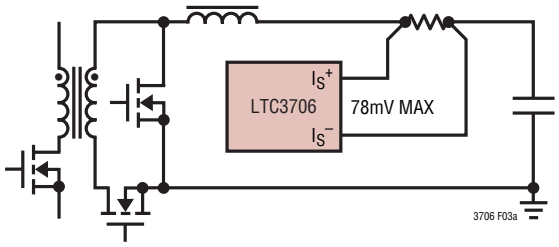


Figure 3a. High Side Inductor: Easier Layout, Low Noise, Accurate

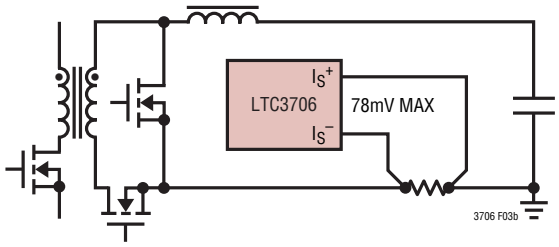


Figure 3b. Low Side Inductor: Accurate, Low Noise, High V_{OUT} Capable

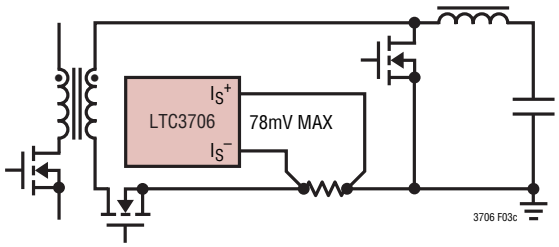


Figure 3c. Switch Current Sensing: Easy Layout, Accurate, Higher Efficiency, High V_{OUT} Capable

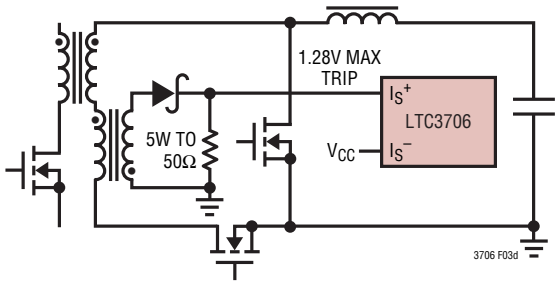


Figure 3d. Current Transformer: Highest Efficiency, High V_{OUT} Capable

Figure 3. Current Sensing Techniques

APPLICATIONS INFORMATION

PolyPhase Applications

Figure 4 shows the basic connections for using the LTC3705 and LTC3706 in PolyPhase applications. One of the phases is always identified as the "master," while all other phases are "slaves." For the LTC3705 (primary side), the master monitors the V_{IN} voltage for undervoltage, performs the open-loop start-up and supplies the initial V_{CC} voltage for the master and all slaves. The LTC3705 slaves simply stand by and wait for PWM signals from their respective pulse transformers. Since the SS/FLT pins of master and slave LTC3705's are interconnected, a FAULT (overcurrent, etc.) on any one of the phases will perform a shutdown/restart on all phases together. The LTC3705 is put into slave mode by omitting the resistor on FS/IN^-. For the LTC3706, the master performs soft-start and voltage-loop regulation by driving all slaves to the same current as the master using the ITH pins. Faults and shutdowns are communicated via the interconnection of the RUN/SS pins. The LTC3706 is put into slave mode by tying the FB pin to V_{CC}.

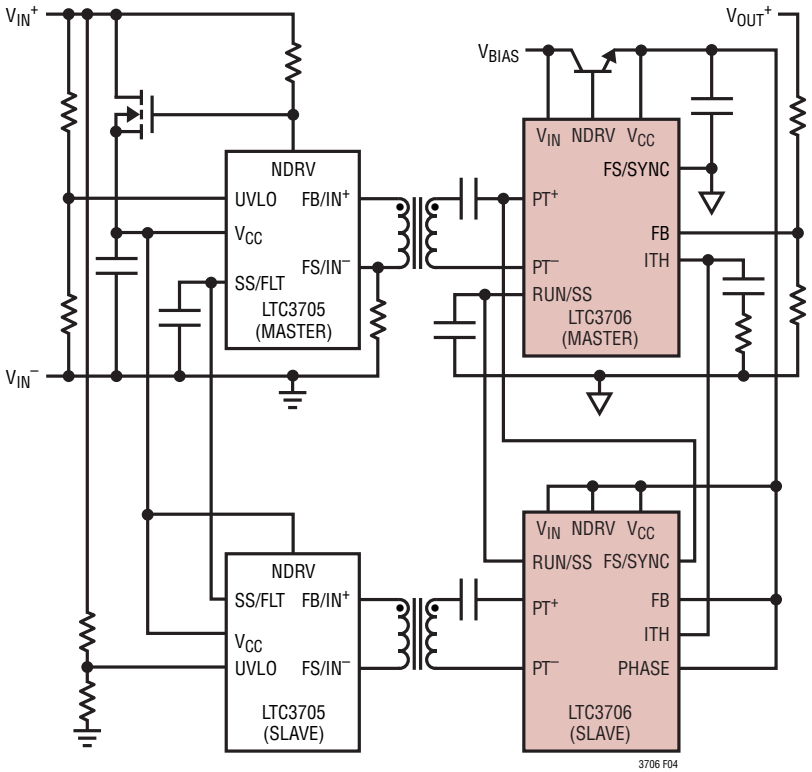


Figure 4. Connections for PolyPhase Operation

TYPICAL APPLICATIONS

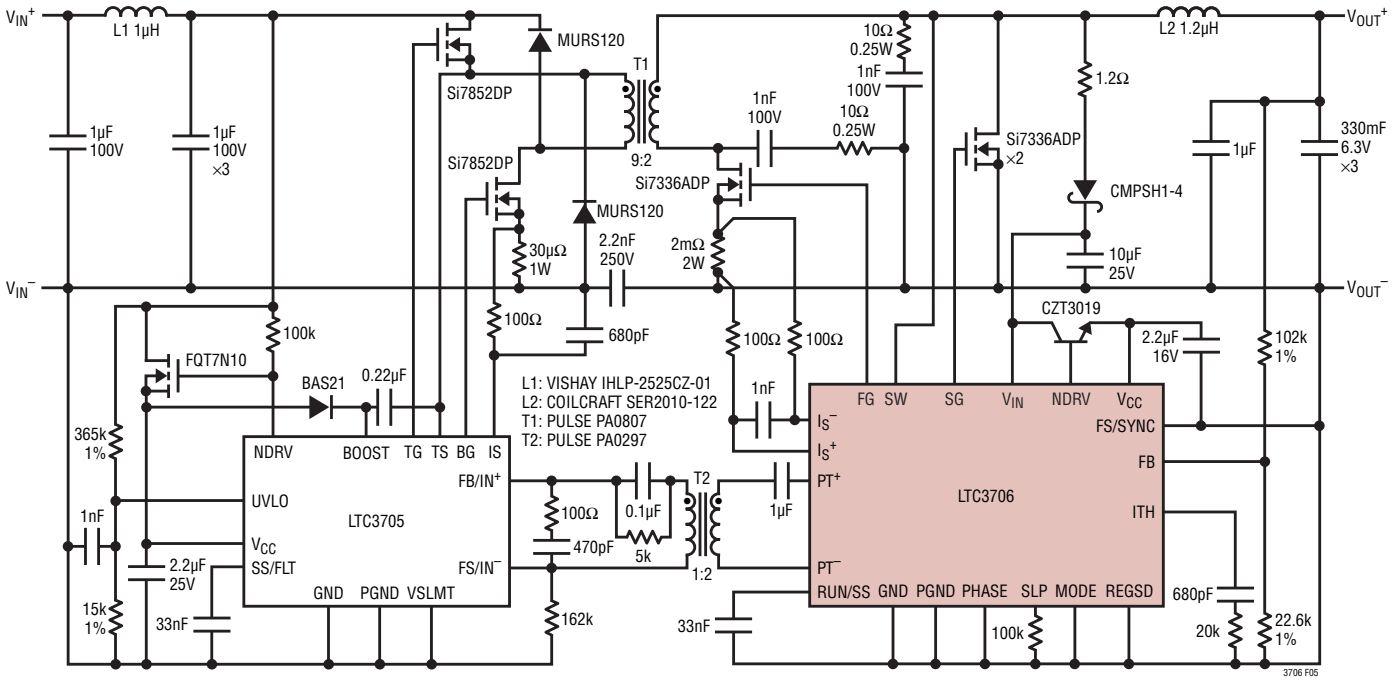
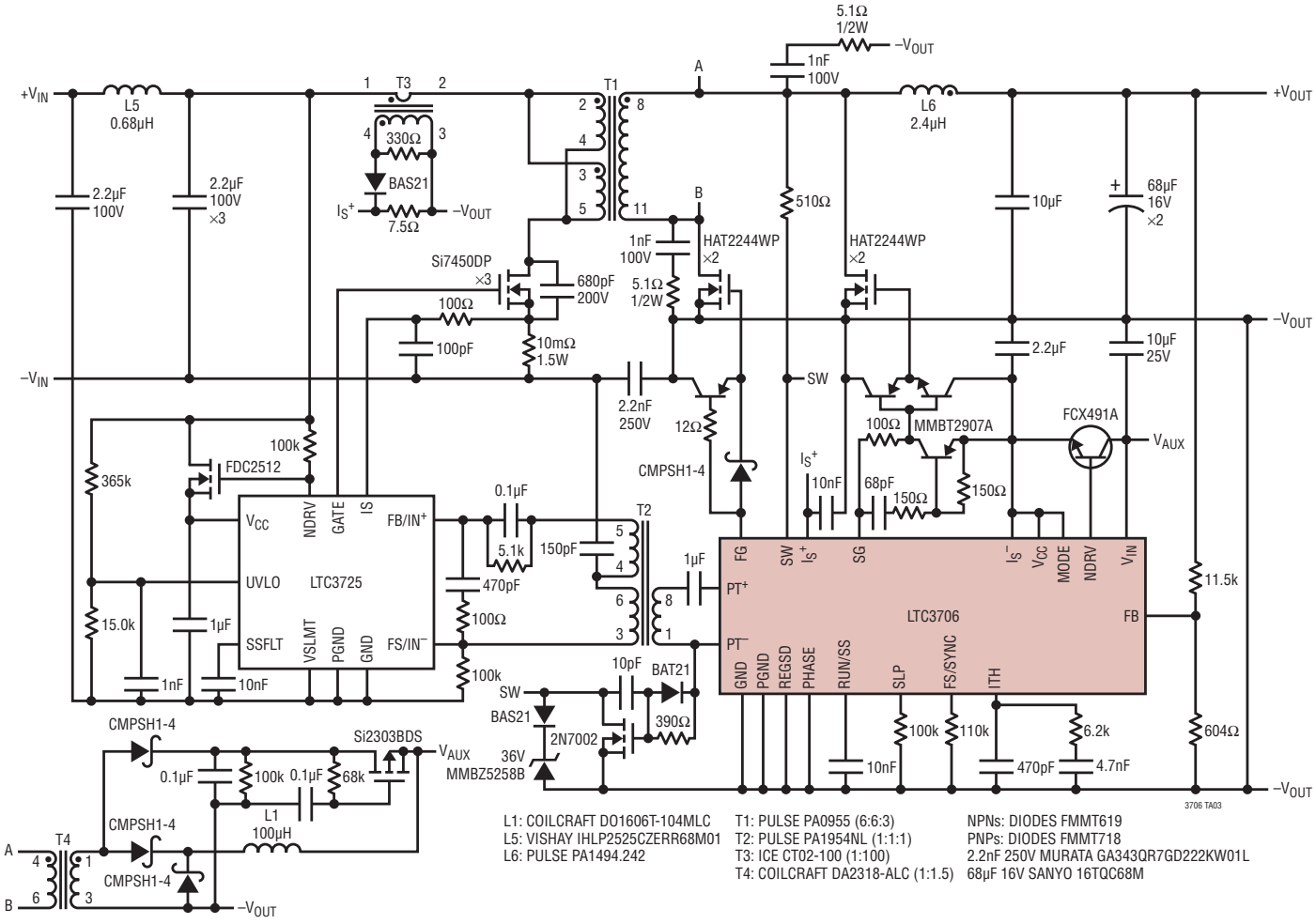


Figure 5. 36V-72V to 3.3V/20A Isolated Forward Converter (See Typical Performance Characteristics)

TYPICAL APPLICATIONS

36V to 72V to 12V/20A Isolated Forward Converter. Can Be Paralleled for Higher Output Power



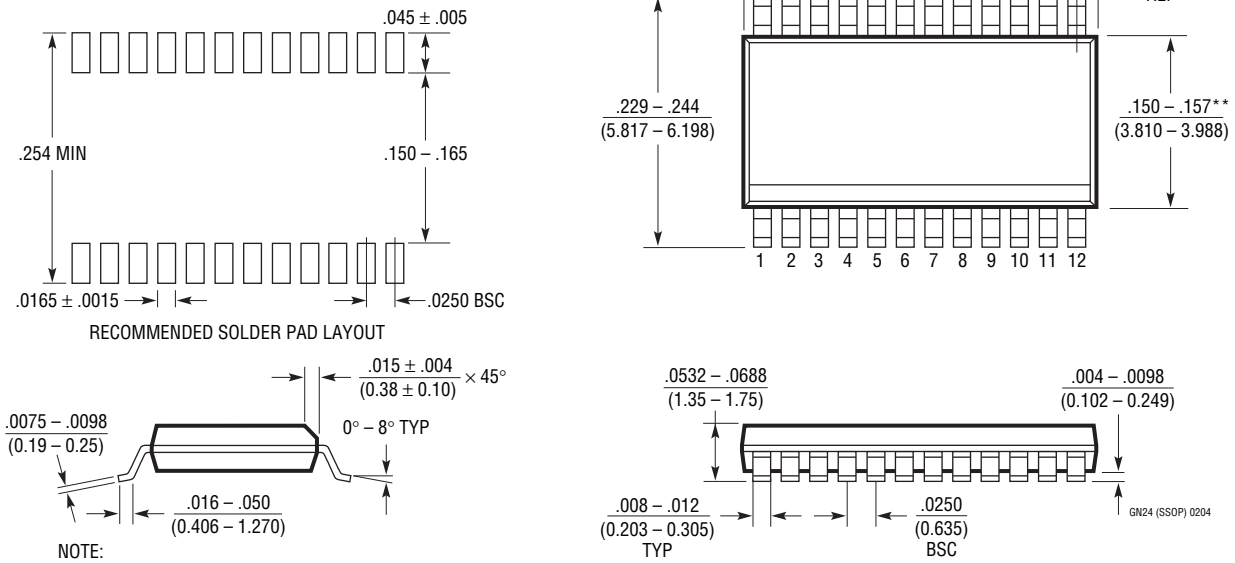
L1: COILCRAFT DO1606T-104MLC
L5: VISHAY IHLP2525CZERR68M01
L6: PULSE PA1494.242

T1: PULSE PA0955 (6:6:3)
T2: PULSE PA1954NL (1:1:1)
T3: ICE CT02-100 (1:100)
T4: COILCRAFT DA2318-ALC (1:1.5)

NPNs: DIODES FMMT619
PNPs: DIODES FMMT718
2.2nF 250V MURATA GA343QR7GD222KW01L
68µF 16V SANYO 16TQC68M

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



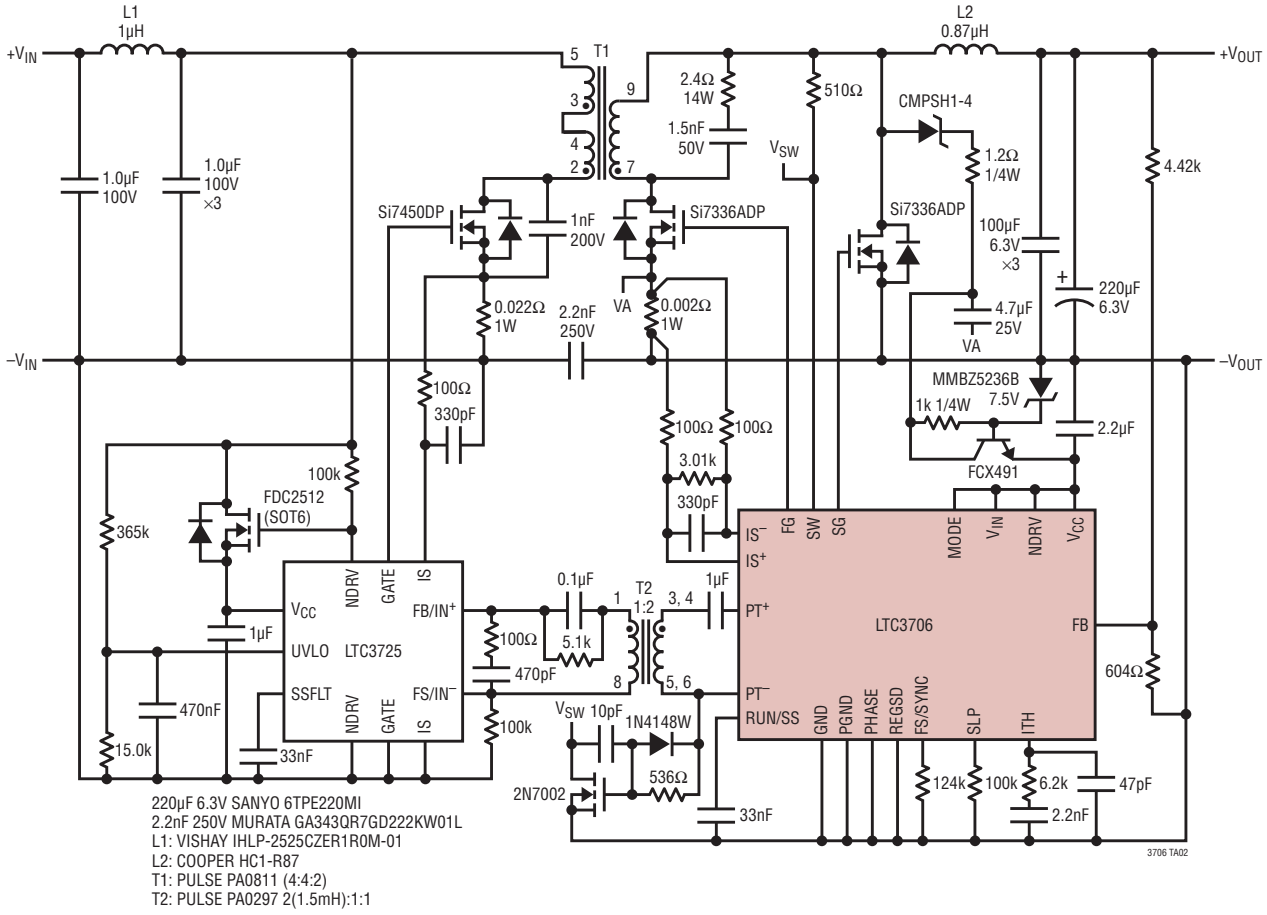
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	7/11	Updated Electrical Characteristics	3, 4
		Updated Table 3	11
		Added new Typical Application schematics	19, 22
		Updated Related Parts	22

TYPICAL APPLICATION

36V to 72V to 5V/20A Isolated Forward Converter



220µF 6.3V SANYO 6TPE220MI
2.2nF 250V MURATA GA343QR7GD222KW01L
L1: VISHAY IHLP-2525CZER1R0M-01
L2: COOPER HC1-R87
T1: PULSE PA0811 (4:4:2)
T2: PULSE PA0297 2(1.5mH):1:1

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3726/LTC3725	Isolated Synchronous No Opto-Forward Controller Chip Set	Ideal for Medium Power 24V or 48V Input Applications
LT1952/LT1952-1	Isolated Synchronous Forward Controllers	Ideal for Medium Power 24V or 48V Input Applications
LTC3723-1/LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers
LTC3721-1/LTC3721-2	Nonsynchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LTC3722/LTC2722-2	Synchronous Isolated Full-Bridge Controllers	Ideal for High Power 24V or 48V Input Applications
LT3748	100V No Opto-Flyback Controller	5V ≤ V_{IN} ≤ 100V, Boundary Mode Operation, MSOP-16 with Extra High Voltage Pin Spacing
LT3758	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, 100kHz to 1MHz Fixed Frequency, 3mm × 3mm DFN-10 and MSOP-10E Package
LTC1871/LTC1871-1 LTC1871-7	Wide Input Range, No R_{SENSE}™ Low Quiescent Current Flyback, Boost and SEPIC Controller	2.5V ≤ V_{IN} ≤ 36V, Burst Mode® Operation at Light Load, MSOP-10
LTC3803/LTC3803-3 LTC3803-5	Flyback DC/DC Controller with Fixed 200kHz or 300kHz Operating Frequency	V_{IN} and V_{OUT} Limited Only by External Components, 6-Pin ThinSOT™ Package
LT3575	Isolated Flyback No Opto-Converter with 2.5A/60V Power Switch	3V ≤ V_{IN} ≤ 40V, Boundary Mode, Up to 14W, TSSOP-16 Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0711 REV D • PRINTED IN USA

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LTC3706EGN#TR LTC3706EGN LTC3706EGN#TRPBF LTC3706IGN#TRPBF LTC3706IGN#TR LTC3706EGN#PBF LTC3706IGN#PBF LTC3706IGN