TUSB320LAI, TUSB320HAI USB Type-C Configuration Channel Logic and Port Control

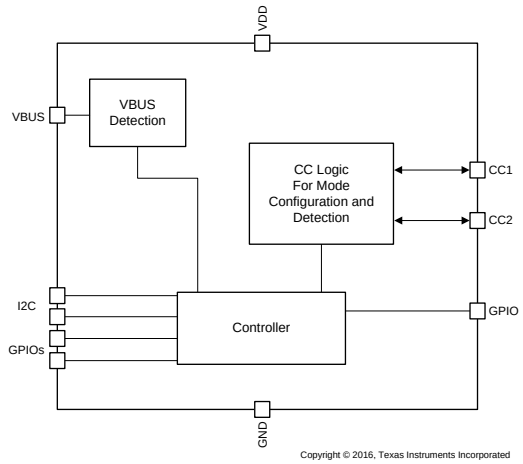
1 Features

- USB Type-C™ Specification 1.1
- Backward Compatible with USB Type-C Specification 1.0
- Supports Up to 3 A of Current Advertisement and Detection
- Mode Configuration
  - Host Only – DFP (Source)
  - Device Only – UFP (Sink)
  - Dual Role Port – DRP
  - Supports both Try.SRC and Try.SNK
- Channel Configuration (CC)
  - Attach of USB Port Detection
  - Cable Orientation Detection
  - Role Detection
  - Type-C Current Mode (Default, Medium, High)
- V_{BUS} Detection
- I^2C or GPIO Control
- Supports up to 400 kHz I^2C
- Role Configuration Control Through I^2C
- Supply Voltage: 2.7 V to 5 V
- Low Current Consumption
- Industrial Temperature Range of –40 to 85°C

2 Applications

- Host, Device, Dual Role Port Applications
- Mobile Phones
- Tablets and Notebooks
- USB Peripherals

Simplified Schematic



3 Description

The TUSB320LA and TUSB320HA devices, hereafter called TUSB320 unless otherwise noted, are Texas Instrument's third generation Type-C configuration channel logic and port controller. The TUSB320 devices use the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The TUSB320 devices can be configured as a downstream facing port (DFP), upstream facing port (UFP) or a dual role port (DRP) making them ideal for any application.

The TUSB320 devices have an alternate configuration as a DFP or UFP according to the Type-C specifications. The CC logic block monitors the CC1 and CC2 pins for pullup or pulldown resistances to determine when a USB port has been attached, the orientation of the cable, and the role detected. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected. V_{BUS} detection is implemented to determine a successful attach in UFP and DRP modes.

The devices operate over a wide supply range and have low-power consumption. The TUSB320 is available in two versions of enable: Active low enable called TUSB320LA and active high enable called TUSB320HA. The TUSB320 family of devices are available in industrial temperature ranges.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB320LAI	X2QFN (12)	1.60 mm × 1.60 mm
TUSB320HAI	X2QFN (12)	1.60 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Sample Applications

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4 Revision History

Changes from Revision C (October 2016) to Revision D — **Page**

- Changed R_{VBUS} values From: MIN = 891, TYP = 900, MAX = 909 KΩ To: MIN = 855, TYP = 887, MAX = 920 KΩ ... 6

Changes from Revision B (September 2016) to Revision C — **Page**

- Changed text for Pin 7 in the Pin Functions table From: "default current mode detected (H); medium or high current mode detected (L)." To: "Refer to Table 3 for more details." ... 3
- Changed text for Pin 8 in the Pin Functions table From: "default or medium current mode detected (H); high current mode detected (L)." To: "Refer to Table 3 for more details." ... 3

Changes from Revision A (March 2016) to Revision B — **Page**

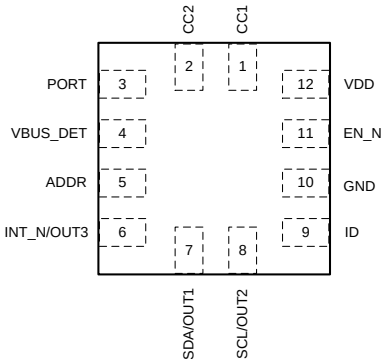
- Changed pins CC1 and CC2 values From: MIN = –0.3 MAX = VDD + 0.3 To: MIN –0.3 MAX = 6 in the *Absolute Maximum Ratings* ... 4

Changes from Original (October 2015) to Revision A — **Page**

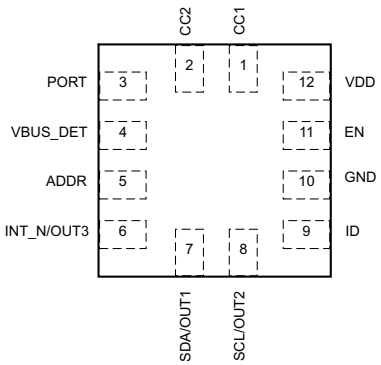
- Added Note 1 and 2 to the *Pin Functions* table ... 3
- Changed the DESCRIPTION of pin EN_N pin in the *Pin Functions* table ... 3
- Changed the DESCRIPTION of pin EN pin in the *Pin Functions* table ... 3
- Changed the DESCRIPTION of pin V_{DD} in the *Pin Functions* table ... 3
- Added Note 2 to the *Electrical Characteristics* table ... 5
- Added Test Condition "See Figure 1" to VBUS_THR in the *Electrical Characteristics* ... 6
- Changed the last sentence of the *Debug Accessory* section ... 12
- Added Note: "SW must make sure..." to the Description of INTERRUPT_STATUS in Table 9 ... 18
- Added text to list item 2 in the *TUSB320LA Initialization Procedure* section ... 28
- Added text to list item 2 in the *TUSB320HA Initialization Procedure* section ... 28

5 Pin Configuration and Functions

RWB Package
12-Pin X2QFN
TUSB320LA Top View



RWB Package
12-Pin X2QFN
TUSB320HA Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TUSB320LA	TUSB320HA		
CC1	1	1	I/O	Type-C configuration channel signal 1
CC2	2	2	I/O	Type-C configuration channel signal 2
PORT(1)	3	3	I	Tri-level input pin to indicate port mode. The state of this pin is sampled when EN_N is asserted low in the TUSB320L device, EN is asserted high in the TUSB320H device, and VDD is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to V_{DD} if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)
VBUS_DET(1)	4	4	I	5-V to 28-V V_{BUS} input voltage. V_{BUS} detection determines UFP attachment. One 900-kΩ external resistor required between system V_{BUS} and VBUS_DET pin.
ADDR(1)	5	5	I	Tri-level input pin to indicate I^2C address or GPIO mode: H — I^2C is enabled and I^2C 7-bit address is 0x67. NC — GPIO mode (I^2C is disabled) L — I^2C is enabled and I^2C 7-bit address is 0x47. ADDR pin should be pulled up to V_{DD} if high configuration is desired
INT_N/OUT3(1)	6	6	O	The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I^2C control mode and is an active low interrupt signal for indicating changes in I^2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: no detection (H), audio accessory connection detected (L).
SDA/OUT1(1)(2)	7	7	I/O	The SDA/OUT1 is a dual-function pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: Refer to Table 3 for more details.
SCL/OUT2(1)(2)	8	8	I/O	The SCL/OUT2 is a dual function pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: Refer to Table 3 for more details.
ID	9	9	O	Open drain output; asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
GND	10	10	G	Ground
EN_N	11	—	I	Enable signal; active low. Pulled up to V_{DD} internally to disable the TUSB320L device. If controlled externally, must be held low at least for 50 ms after VDD has reached its valid voltage level.
EN	—	11	I	Enable signal; active high. Pulled down to GND internally to disable the TUSB320H device. If controlled externally, must be held low at least for 50 ms after VDD has reached its valid voltage level.
V_{DD}	12	12	P	Positive supply voltage. V_{DD} must ramp within 25 ms or less

(1) When V_{DD} is off, the TUSB320 non-failsafe pins (VBUS_DET, ADDR, PORT, OUT[3:1] pins) could back-drive the TUSB320 device if not handled properly. When necessary to pull these pins up, it is recommended to pullup PORT, ADDR, and INT_N/OUT3 to the device V_{DD} supply. The VBUS_DET must be pulled up to VBUS through a 900-kΩ resistor.
(2) When using the 3.3 V supply for I^2C, the end user must ensure that the V_{DD} is 3 V and above. Otherwise the I^2C may back power the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	6	V
Control pins	PORT, ADDR, ID, EN_N, INT_N/OUT3	–0.3	V_{DD} + 0.3	V
	CC1, CC2	–0.3	6	
	SDA/OUT1, SCL/OUT2	–0.3	V_{DD} + 0.3	
	VBUS_DET , EN	–0.3	4	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	2.7		5	V
V_{BUS}	System V_{BUS} voltage	4	5	28	V
T_A	TUSB320HAI and TUSB320LAI Operating free air temperature range	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB320 RWB (X2QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and C Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
$I_{UNATTACHED\_UFP}$	Current consumption in unattached mode when port is unconnected and waiting for connection. [V_{DD} = 4.5 V, EN_N (TUSB320LA) = L, EN (TUSB320HA) = H, ADDR = NC, PORT = L]			70		µA
I_{ACTIVE_UFP}	Current consumption in active mode. [V_{DD} = 4.5 V, EN_N (TUSB320LA) = L, EN (TUSB320HA) = H, ADDR = NC, PORT = L]			70		µA
$I_{SHUTDOWN}$	Leakage current when V_{DD} is supplied, but the TUSB320 device is not enabled. [V_{DD} = 4.5 V, EN_N (TUSB320LA) = H, EN (TUSB320HA) = L]			0.04		µA
CC1 AND CC2 PINS						
R_{CC_DB}	Pulldown resistor when in dead-battery mode.		4.1	5.1	6.1	kΩ
R_{CC_D}	Pulldown resistor when in UFP or DRP mode.		4.6	5.1	5.6	kΩ
$V_{UFP\_CC\_USB}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising default current source capability.		0.25		0.61	V
$V_{UFP\_CC\_MED}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising medium (1.5-A) current source capability.		0.7		1.16	V
$V_{UFP\_CC\_HIGH}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising high (3-A) current source capability.		1.31		2.04	V
$V_{TH\_DFP\_CC\_USB}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising default current source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_MED}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising medium current (1.5-A) source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_HIGH}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising high current (3.0-A) source capability.		2.46	2.6	2.74	V
$I_{CC\_DEFAULT\_P}$	Default mode pullup current source when operating in DFP or DRP mode.		64	80	96	µA
$I_{CC\_MED\_P}$	Medium (1.5-A) mode pullup current source when operating in DFP or DRP mode.		166	180	194	µA
$I_{CC\_HIGH\_P}$	High (3-A) mode pullup current source when operating in DFP or DRP mode.(1)		304	330	356	µA
CONTROL PINS: PORT, ADDR, INT/OUT3, EN_N, EN, ID						
V_{IL}	Low-level control signal input voltage (PORT, ADDR, EN_N, EN)				0.4	V
V_{IM}	Mid-level control signal input voltage (PORT, ADDR)		0.28 × V_{DD}		0.56 × V_{DD}	V
V_{IH}	High-level control signal input voltage (PORT, ADDR, EN_N)		V_{DD} – 0.3		V_{DD}	V
V_{IH_EN}	High-Level control signal input voltage for EN for TUSB320HA		1.05		3.65	V
I_{IH}	High-level input current		–20		20	µA
I_{IL}	Low-level input current		–10		10	µA
$I_{ID\_LEAKAGE}$	Current Leakage on ID pin	V_{DD} = 0 V; ID = 5 V			10	µA
R_{EN_N}	Internal pullup resistance for EN_N for TUSB320LA			1.1		MΩ
R_{EN}	Internal pulldown resistance for EN for TUSB320HA			500		kΩ
R_{pu} (2)	Internal pullup resistance (PORT, ADDR)			588		kΩ
R_{pd} (2)	Internal pulldown resistance (PORT, ADDR)			1.1		MΩ
V_{OL}	Low-level signal output voltage (open-drain) (INT_N/OUT3, ID)	I_{OL} = –1.6 mA			0.4	V

(1) V_{DD} must be 3.5 V or greater to advertise 3 A current.
(2) Internal pullup and pulldown for PORT and ADDR are removed after the device has sampled EN = high or EN_N = low.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{p_ODext}	External pullup resistor on open drain IOs (INT_N/OUT3, ID)			200		kΩ
R_{p_TLext}	Tri-level input external pullup resistor (PORT, ADDR)			4.7		kΩ
I^2C - SDA/OUT1, SCL/OUT2 CAN OPERATE FROM 1.8 V OR 3.3 V (±10%)(3)						
V_{DD_I2C}	Supply range for I^2C (SDA/OUT1, SCL/OUT2)		1.65	1.8	3.6	V
V_{IH}	High-level signal voltage		1.05		3.6	V
V_{IL}	Low-level signal voltage				0.4	V
V_{OL}	Low-level signal output voltage (open drain)	I_{OL} = –1.6 mA			0.4	V
VBUS_DET IO PINS (CONNECTED TO SYSTEM V_{BUS} SIGNAL)						
V_{BUS_THR}	V_{BUS} threshold range	See Figure 1	2.95	3.3	3.8	V
R_{VBUS}	External resistor between V_{BUS} and VBUS_DET pin		855	887	920	KΩ
R_{VBUS_PD}	Internal pulldown resistance for VBUS_DET			95		KΩ

(3) When using 3.3 V for I^2C, customer must ensure V_{DD} is above 3.0 V at all times.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
I^2C (SDA, SCL)					
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	10			ns
$t_{SU:STA}$	Set-up time, SCL to start condition	0.6			µs
$t_{HD:STA}$	Hold time (repeated), start condition to SCL	0.6			µs
$t_{SU:STO}$	Set up time for stop condition	0.6			µs
t_{BUF}	Bus free time between a stop and start condition	1.3			µs
$t_{VD:DAT}$	Data valid time			0.9	µs
$t_{VD:ACK}$	Data valid acknowledge time			0.9	µs
f_{SCL}	SCL clock frequency; I^2C mode for local I^2C control			400	kHz
t_r	Rise time of both SDA and SCL signals			300	ns
t_f	Fall time of both SDA and SCL signals			300	ns
C_{BUS_100KHZ}	Total capacitive load for each bus line when operating at ≤ 100 kHz			400	pF
C_{BUS_400KHz}	Total capacitive load for each bus line when operating at 400 kHz			100	pF

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CCCB\_DEFAULT}$	Power on default of CC1 and CC2 voltage debounce time	DEBOUCE register = 2'b00		168		ms
t_{VBUS_DB}	Debounce of VBUS_DET pin after valid V_{BUS_THR}			2		ms
$t_{DRP\_DUTY\_CYCLE}$	Power-on default of percentage of time DRP advertises DFP during a t_{DRP}	DRP_DUTY_CYCLE register = 2'b00		30%		
t_{DRP}	The period during which the TUSB320HA or the TUSB320LA in DFP mode completes a DFP to UFP and back advertisement.		50	75	100	ms
t_{I2C_EN}	Time from TUSB320LA EN_N low or TUSB320HA EN high and V_{DD} active to I^2C access available				100	ms
t_{SOFT_RESET}	Soft reset duration		26	49	95	ms

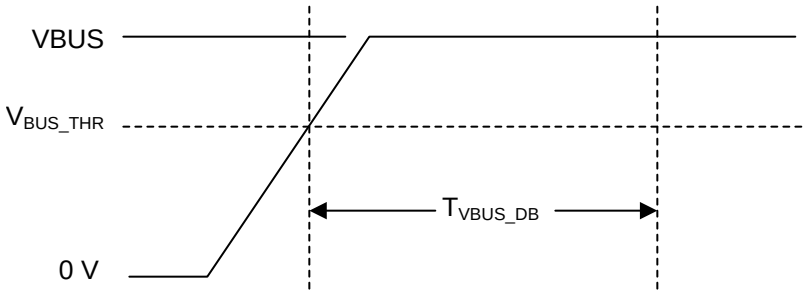


Figure 1. VBUS Detect and Debounce

7 Detailed Description

7.1 Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Because of the nature of the connector, a scheme is required to determine the connector orientation. Additional schemes are required to determine when a USB port is attached and what the acting role of the USB port (DFP, UFP, DRP) is, as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C pecification. The TUSB320 devices provide Configuration Channel (CC) logic for determining USB port attach and detach, role detection, cable orientation, and Type-C current mode. The TUSB320 devices also contains several features such as mode configuration and low standby current which make these devices ideal for source or sinks in USB2.0 applications.

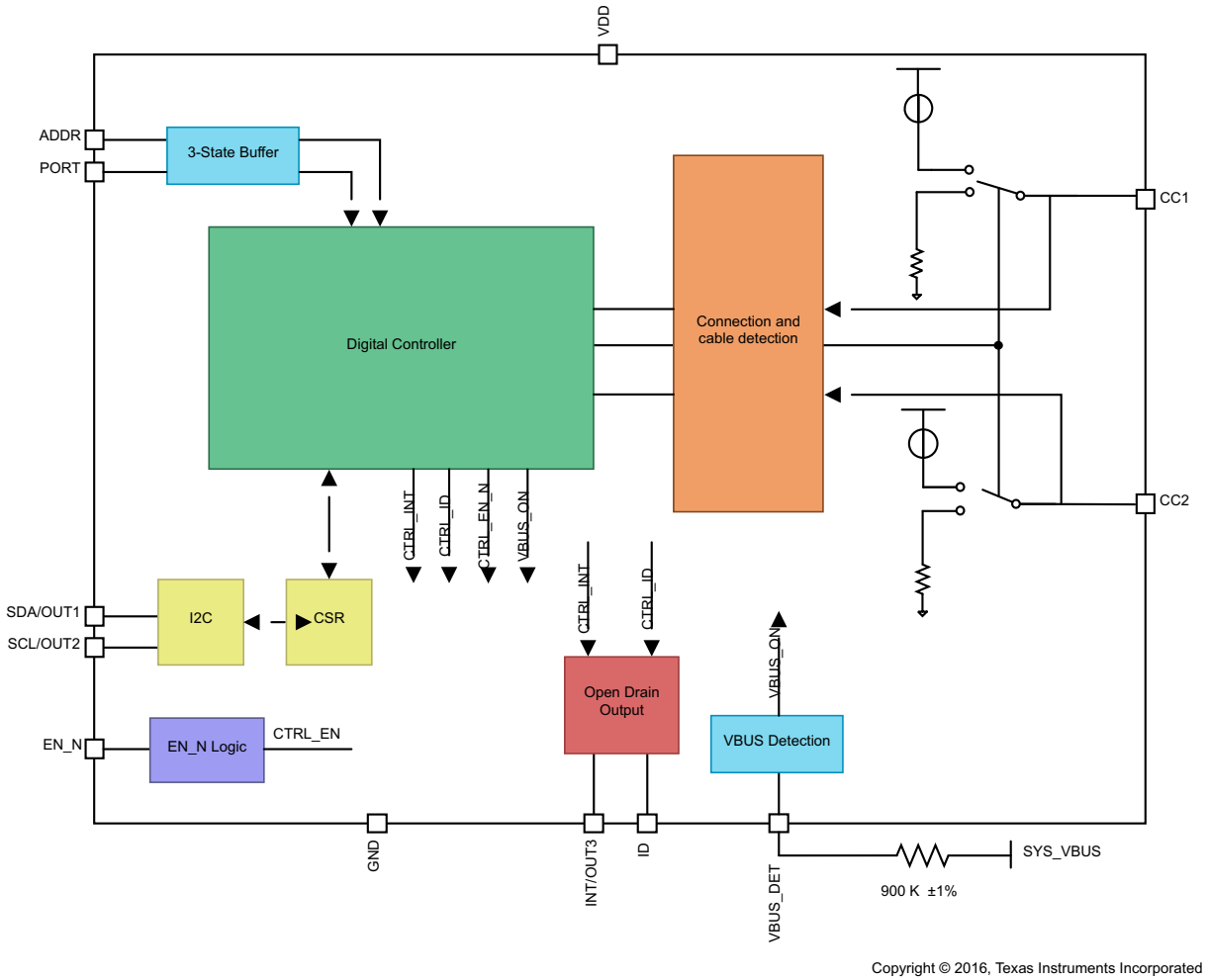


Figure 2. Functional Block Diagram of TUSB320

7.1.1 Cables, Adapters, and Direct Connect Devices

Type-C specification defines several cables, plugs, and receptacles to be used to attach ports. The TUSB320 devices support all cables, receptacles, and plugs. The TUSB320 devices do not support any USB Type-C feature which requires USB power delivery communication over CC lines like e-marking or alternate mode.

7.1.1.1 USB Type-C Receptacles and Plugs

Below is list of Type-C receptacles and plugs supported by the TUSB320 devices:

- USB Type-C receptacle for USB2.0 platforms and devices

Overview (continued)

- USB full-featured Type-C plug
- USB2.0 Type-C plug

7.1.1.2 USB Type-C Cables

Below is a list of Type-C cables types supported by the TUSB320 devices:

- USB full-featured Type-C cable
- USB2.0 Type-C cable with USB2.0 plug
- Captive cable on remote device with either a USB full-featured plug or USB2.0 plug

7.1.1.3 Legacy Cables and Adapters

The TUSB320 devices support legacy cable adapters as defined by the Type-C specification. The cable adapter must correspond to the mode configuration of a TUSB320 device.

Figure 3 displays the TUSB320 Legacy Adapter Implementation Circuit.

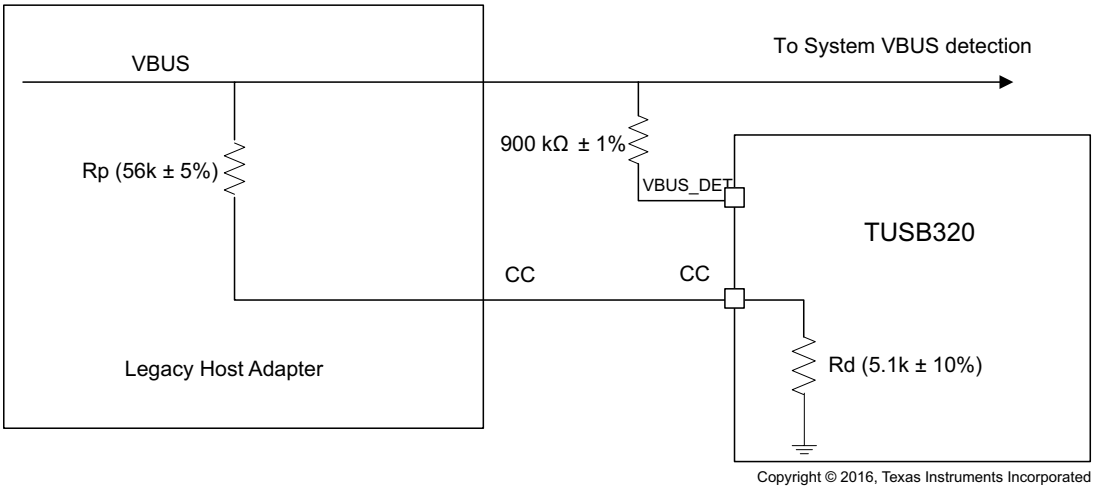


Figure 3. Legacy Adapter Implementation Circuit

7.1.1.4 Direct Connect Devices

The TUSB320 devices support the attaching and detaching of a direct-connect device.

7.1.1.5 Audio Adapters

Additionally, the TUSB320 devices support audio adapters for audio accessory mode, including:

- Passive Audio Adapter
- Charge Through Audio Adapter

7.2 Feature Description

7.2.1 Port Role Configuration

The TUSB320 devices can be configured as a downstream facing port (DFP), upstream facing port (UFP), or dual-role port (DRP) using the tri-level PORT pin. The PORT pin should be pulled high to V_{DD} using a pullup resistance, low to GND or left as floated on the PCB to achieve the desired mode. This flexibility allows a TUSB320 device to be used in a variety of applications. A TUSB320 device samples the PORT pin after reset and maintains the desired mode until the TUSB320 device is reset again. The port role can also be selected through I^2C registers. Table 1 lists the supported features in each mode:

Feature Description (continued)

Table 1. Supported Features for the TUSB320 Device by Mode

PORT PIN / SUPPORTED FEATURES	HIGH (DFP ONLY)	LOW (UFP ONLY)	NC (DRP)
Port attach and detach	Yes	Yes	Yes
Cable orientation (through I^2C)	Yes	Yes	Yes
Current advertisement	Yes	-	Yes (DFP)
Current detection	-	Yes	Yes (UFP)
Accessory modes (audio and debug)	Yes	Yes	Yes
Try.SRC	-	-	Yes
Try.SNK	-	-	Yes
Active cable detection	Yes	-	Yes (DFP)
I^2C / GPIO	Yes	Yes	Yes
Legacy cables	Yes	Yes	Yes
V_{BUS} detection	-	Yes	Yes (UFP)

7.2.1.1 Downstream Facing Port (DFP) - Source

The TUSB320 device can be configured as a DFP-only by pulling the PORT pin high through a resistance to V_{DD} or by changing the MODE_SELECT register. In DFP-only mode, the TUSB320 device constantly presents Rps on both CC. In DFP-only mode, the TUSB320 device initially advertises default USB Type-C current. The Type-C current can be adjusted through I^2C if the system requires to increase the amount advertised. The TUSB320 device adjusts the Rps to match the desired Type-C current advertisement. In GPIO mode, the TUSB320 device only advertises default Type-C current.

When configured as a DFP, the TUSB320 device can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. A USB Type-C 1.1 compliant DFP can not connect to a Type-C 1.0 DRP. Because the TUSB320 device is compliant to Type-C 1.1, the TUSB320 device can not operate with a USB Type-C 1.0 DRP device. This limitation is a result of a backwards compatibility problem between USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

7.2.1.2 Upstream Facing Port (UFP) - Sink

The TUSB320 device can be configured as a UFP only by pulling the PORT pin low to GND. In UFP mode, the TUSB320 device constantly presents pulldown resistors (Rd) on both CC pins. The TUSB320 device monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The TUSB320 device debounces the CC pins and wait for V_{BUS} detection before successfully attaching. As a UFP, the TUSB320 device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs (if in GPIO mode) or through the I^2C CURRENT_MODE_DETECT register one time in the Attached.SNK state.

7.2.1.3 Dual Role Port (DRP)

The TUSB320 device can be configured to operate as a DRP when the PORT pin is left floated on the PCB. In DRP mode, the TUSB320 device toggles between operating as a DFP and a UFP. When functioning as a DFP in DRP mode, the TUSB320 device complies with all operations as defined for a DFP according to the Type-C specification. When presenting as a UFP in DRP mode, the TUSB320 device operates as defined for a UFP according to the Type-C specification.

The TUSB320 supports two optional Type-C DRP features called Try.SRC and Try.SNK. Products supporting dual-role functionality may have a requirement to be a source (DFP) or a sink (UFP) when connected to another dual-role capable product. For example, a dual-role capable notebook can be a source when connected to a tablet, or a cell phone can be a sink when connected to a notebook or tablet. When standard DRP products (products which don't support either Try.SRC or Try.SNK) are connected together, the role (UFP or DFP) outcome is not predetermined. These two optional DRP features provide a means for dual-role capable products to connect to another dual-role capable product in the role desired. Try.SRC and Try.SNK are only available when TUSB320 is configured in I2C mode. When operating in GPIO mode, the TUSB320 will always operate as a standard DRP.

The Try.SRC feature of the TUSB320 device provides a means for a DRP product to connect as a DFP when connected to another DRP product that doesn't implement Try.SRC. When two products which implement Try.SRC are connected together, the role outcome of either UFP or DFP is the same as a standard DRP. Try.SRC is enabled by changing I2C register SOURCE_PREF to 2'b11. Once this register is changed to 2'b11, the TUSB320 will always attempt to connect as a DFP when attached to another DRP capable device.

The Try.SNK feature of the TUSB320 device provides a method for a DRP product to connect as a UFP when connected to another DRP product that doesn't implement Try.SNK. When two products which implement Try.SNK are connected together, the role outcome of either UFP or DFP is the same as a standard DRP. Try.SNK is enabled by changing I2C register SOURCE_PREF to 2'b01. Once this register is changed to 2'b01, the TUSB320 will always attempt to connect as a UFP when attached to another DRP capable device.

7.2.2 Type-C Current Mode

When a valid cable detection and attach have been completed, the DFP has the option to advertise the level of Type-C current a UFP can sink. The default current advertisement for the TUSB320 device is max of 500 mA (for USB2.0) or max of 900 mA (for USB3.1). If a higher level of current is available, the I^2C registers can be written to provide medium current at 1.5 A or high current at 3 A. When the CURRENT_MODE_ADVERTISE register has been written to advertise higher than default current, the DFP adjusts the Rps for the specified current level. If a DFP advertises 3 A, system designer must ensure that the V_{DD} of the TUSB320 device is 3.5 V or greater. Table 2 lists the Type-C current advertisements in GPIO an I^2C modes.

Table 2. Type-C Current Advertisement for GPIO and I^2C Modes

<table>
<tr><th colspan="2" rowspan="2">TYPE-C CURRENT</th><th colspan="2">GPIO MODE (ADDR PIN IN NC)</th><th colspan="2">I²C MODE (ADDR PIN H, L)</th></tr>
<tr><th>UFP (PORT PIN L)</th><th>DFP (PORT PIN H)</th><th>UFP</th><th>DFP</th></tr>
<tr><td rowspan="2">Default</td><td rowspan="2">max of 500 mA (USB2.0) max of 900 mA (USB3.1)</td><td rowspan="3">Current mode detected and output through OUT1 / OUT2</td><td>Only advertisement</td><td rowspan="3">Current mode detected and read through I²C register</td><td>I²C register default is 500 or 900 mA (max)</td></tr>
<tr><td rowspan="2">N/A</td><td rowspan="2">Advertisement selected through writing I²C register</td></tr>
<tr><td colspan="2">Medium - 1.5 A (max)</td></tr>
<tr><td colspan="2">High - 3 A (max)</td><td colspan="3"></td></tr>
</table>

7.2.3 Accessory Support

The TUSB320 device supports audio and debug accessories in UFP, DFP mode and DRP mode. Audio and debug accessory support is provided through reading of I^2C registers. Audio accessory is also supported through GPIO mode with INT_N/OUT3 pin (audio accessory is detected when INT_N/OUT3 pin is low).

7.2.3.1 Audio Accessory

Audio accessory mode is supported through two types of adapters. First, the passive audio adapter can be used to convert the Type-C connector into an audio port. To effectively detect the passive audio adapter, the TUSB320 device must detect a resistance < Ra on both of the CC pins.

Secondly, a charge through audio adapter can be used. The primary difference between a passive and charge through adapter is that the charge through adapter supplies 500 mA of current over VBUS. The charge through adapter contains a receptacle and a plug. The plug acts as a DFP and supply V_{BUS} when the plug detects a connection.

When the TUSB320 device is configured in GPIO mode, OUT3 pin determines if an audio accessory is connected. When an audio accessory is detected, the OUT3 pin is pulled low.

7.2.3.2 Debug Accessory

Debug is an additional state supported by USB Type-C. The specification does not define a specific user scenario for this state, but the specification is important because the end user could use debug accessory mode to enter a test state for production specific to the application. The TUBS320 device will detect a debug accessory if R_d or R_p is detected on both CC1 and CC2.

7.2.4 I^2C and GPIO Control

The TUSB320 device can be configured for I^2C communication or GPIO outputs using the ADDR pin. The ADDR pin is a tri-level control pin. When the ADDR pin is left floating (NC), the TUSB320 device is in GPIO output mode. When the ADDR pin is pulled high or pulled low, the TUSB320 device is in I^2C mode.

All outputs for the TUSB320 device are open drain configuration.

The OUT1 and OUT2 pins are used to output the Type-C current mode when in GPIO mode. Additionally, the OUT3 pin is used to communicate the audio accessory mode in GPIO mode. Table 3 lists the output pin settings. See the *Pin Configuration and Functions* section for more information.

Table 3. Simplified Operation for OUT1 and OUT2

OUT1	OUT2	ADVERTISEMENT
H	H	Default Current in Unattached State
H	L	Default Current in Attached State
L	H	Medium Current (1.5 A) in Attached State
L	L	High Current (3.0 A) in Attached State

When operating in I^2C mode, the TUSB320 device uses the SCL and SDA lines for clock and data and the INT_N pin to communicate a change in I^2C registers, or an interrupt, to the system. The INT_N pin is pulled low when the TUSB320 device updates the registers with new information. The INT_N pin is open drain. The INTERRUPT_STATUS register will be set when the INT_N pin is pulled low. To clear the INTERRUPT_STATUS register, the end user writes to I^2C.

When operating in GPIO mode, the OUT3 pin is used in place of the INT_N pin to determine if an audio accessory is detected and attached. The OUT3 pin is pulled low when an audio accessory is detected.

NOTE

When using the 3.3 V supply for I^2C, the end user must ensure that the V_{DD} is 3 V and above. Otherwise the I^2C can back power the device.

7.2.5 V_{BUS} Detection

The TUSB320 device supports V_{BUS} detection according to the Type-C specification. V_{BUS} detection is used to determine the attachment and detachment of a UFP and to determine the entering and exiting of accessary modes. V_{BUS} detection is also used to successfully resolve the role in DRP mode.

The system V_{BUS} voltage must be routed through a 900-kΩ resistor to the VBUS_DET pin on the TUSB320 device if the PORT pin is configured as a DRP or a UFP. If the TUSB320 device is configured as a DFP and only ever used in DFP mode, the VBUS_DET pin can be left unconnected.

7.3 Device Functional Modes

The TUSB320 device has four functional modes. Table 4 lists these modes:

Table 4. USB Type-C States According to TUSB320 Functional Modes

MODES	GENERAL BEHAVIOR	PORT PIN	STATES(1)
Unattached	USB port unattached. ID, PORT operational. I^2C on. CC pins configure according to PORT pin.	UFP	Unattached.SNK
			Unattached.Accessory
			AttachWait.Accessory
			AttachWait.SNK
		DRP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs operational. I^2C on.	UFP	Attached.SNK
			Audio accessory
			Debug accessory.SNK
		DRP	Attached.SNK
			Attached.SRC
			Audio accessory
			Debug accessory.SNK or Debug accessory.SRC
		DFP	Attached.SRC
			Audio accessory
			Debug accessory.SRC
Dead battery	No operation. V_{DD} not available.	UFP/DRP/DFP	Default device state to UFP/SNK with Rd.
Shutdown	V_{DD} available. TUSB320LA EN_N pin high. TUSB320HA EN pin low.	UFP/DRP/DFP	Default device state to UFP/SNK with Rd.

(1) Required; not in sequential order.

7.3.1 Unattached Mode

Unattached mode is the primary mode of operation for the TUSB320 device, because a USB port can be unattached for a lengthy period of time. In unattached mode, V_{DD} is available, and all IOs and I^2C are operational. After the TUSB320 device is powered up, the part enters unattached mode until a successful attach has been determined. Initially, right after power up, the TUSB320 device comes up as an Unattached.SNK. The TUSB320 device checks the PORT pin and operates according to the mode configuration. The TUSB320 device toggles between the UFP and the DFP if configured as a DRP. In unattached mode, I^2C can be used to change the mode configuration or port role if the board configuration of the PORT pin is not the desired mode. Writing to the I^2C MODE_SELECT register can override the PORT pin in unattached mode. The PORT pin is only sampled at reset (EN_N high to low transition for the TUSB320LA device or the EN low to high transition for theTUSB320HA device), after I2C_SOFT_RESET, or power up. I^2C must be used after reset to change the device mode configuration.

7.3.2 Active Mode

Active mode is defined as the port being attached. In active mode, all GPIOs are operational, and I^2C is read / write (R/W). When in active mode, the TUSB320 device communicates to the AP that the USB port is attached. This communication happens through the ID pin if TUSB320 is configured as a DFP or DRP connect as source. If TUSB320 is configured as a UFP or a DRP connected as a sink, the OUT1/OUT2 and INT_N/OUT3 pins are used. The TUSB320 device exits active mode under the following conditions:

- Cable unplug
- V_{BUS} removal if attached as a UFP
- Dead battery; system battery or supply is removed
- TUSB320LA EN_N pin floated or pulled high
- TUSB320HA EN pin floated or pulled low.

During active mode, I^2C be used to change the mode configuration following the sequence below. This same sequence is valid when TUSB320 is in unattached mode.

- Set the DISABLE_TERM register (address 0x0A bit 0) to a 1'b1.
- Change the MODE_SELECT register (address 0x0A bits 5:4) to desired mode of operation.
- Wait 5 ms.
- Clear the DISABLE_TERM register (address 0x0A bit 0) to 1'b0.

7.3.3 Dead Battery Mode

During dead battery mode, V_{DD} is not available. CC pins always default to pulldown resistors in dead battery mode. Dead battery mode means:

- TUSB320 in UFP with 5.1-kΩ ± 20% Rd; cable connected and providing charge
- TUSB320 in UFP with 5.1-kΩ ± 20% Rd; nothing connected (application could be off or have a discharged battery)

NOTE

When V_{DD} is off, the TUSB320 non-failsafe pins (VBUS_DET, ADDR, PORT, OUT[3:1] pins) could back-drive the TUSB320 device if not handled properly. When necessary to pull these pins up, TI recommendeds pulling up PORT, ADDR, and INT_N/OUT3 to the device's V_{DD} supply. The VBUS_DET must be pulled up to V_{BUS} through a 900-kΩ resistor.

7.3.4 Shutdown Mode

Shutdown mode for TUSB320LA device is defined as follows:

- Supply voltage available and EN_N pin is pulled high or floating.
- EN_N pin has internal pullup resistor.
- The TUSB320LA device is off, but still maintains the Rd on the CC pins

Shutdown mode for TUSB320HA device is defined as follows:

- Supply voltage available and EN pin is pulled low or floating.
- EN pin has internal pulldown resistor.
- The TUSB320HA device is off, but still maintains the Rd on the CC pins

7.4 Programming

For further programmability, the TUSB320 device can be controlled using I²C. The TUSB320 device local I²C interface is available for reading/writing after T_{I2C_EN} when the device is powered up. The SCL and SDA terminals are used for I²C clock and I²C data respectively. If I²C is the preferred method of control, the ADDR pin must be set accordingly.

Table 5. TUSB320 I²C Addresses

TUSB320 I²C Target Address								
ADDR pin	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (W/R)**
H	1	1	0	0	1	1	1	0/1
L	1	0	0	0	1	1	1	0/1

The following procedure should be followed to write to TUSB320 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB320 7-bit address and a zero-value R/W bit to indicate a write cycle.
2. The TUSB320 device acknowledges the address cycle.
3. The master presents the sub-address (I²C register within the TUSB320 device) to be written, consisting of one byte of data, MSB-first.
4. The TUSB320 device acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The TUSB320 device acknowledges the byte transfer.
7. The master can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB320 device.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TUSB320 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB320 7-bit address and a one-value R/W bit to indicate a read cycle.
2. The TUSB320 device acknowledges the address cycle.
3. The TUSB320 device transmits the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I²C register occurred prior to the read, then the TUSB320 device starts at the sub-address specified in the write.
4. The TUSB320 device waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB320 device transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB320 7-bit address and a zero-value R/W bit to indicate a read cycle.
2. The TUSB320 device acknowledges the address cycle.
3. The master presents the sub-address (I²C register within the TUSB320 device) to be read, consisting of one byte of data, MSB-first.
4. The TUSB320 device acknowledges the sub-address cycle.
5. The master terminates the read operation by generating a stop condition (P).

NOTE

If no sub-addressing is included for the read procedure, then the reads start at register offset 00h and continue byte-by-byte through the registers until the I²C master terminates the read operation. If a I²C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

7.5 Register Maps

Table 6. CSR Registers

ACCESS TAG	NAME	MEANING
R	Read	The field can be read by software.
W	Write	The field can be written by software.
S	Set	The field can be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field can be cleared by a write of one. Writes of zeros to the field have no effect.
U	Update	Hardware can autonomously update this field.
NA	No Access	Not accessible or not applicable.

7.5.1 CSR Registers (address = 0x00 – 0x07)

Figure 4. CSR Registers (address = 0x00 – 0x07)

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. CSR Registers (address = 0x00 – 0x07)

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R		For the TUSB320 device these fields return a string of ASCII characters returning TUSB320 Addresses 0x07 - 0x00 = {0x00 0x54 0x55 0x53 0x42 0x33 0x32 0x30}

7.5.2 CSR Registers (address = 0x08)

Figure 5. CSR Registers (address = 0x08)

7	6	5	4	3	2	1	0
CURRENT_MODE_ADVERTISE		CURRENT_MODE_DETECT		ACCESSORY_CONNECTED			ACTIVE_CABLE_DETECTION
RW		RU		RU			RU

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. CSR Registers (address = 0x08)

Bit	Field	Type	Reset	Description
7:6	CURRENT_MODE_ADVERTISE	RW	00	These bits are programmed by the application to raise the current advertisement from default. 00 – Default (500 mA / 900 mA) initial value at startup 01 – Mid (1.5 A) 10 – High (3 A) 11 – Reserved
5:4	CURRENT_MODE_DETECT	RU	00	These bits are set when a UFP determines the Type-C Current mode. 00 – Default (value at start up) 01 – Medium 10 – Audio Charged through accessory – 500 mA 11 – High
3:1	ACCESSORY_CONNECTED	RU	000	These bits are read by the application to determine if an accessory was attached. 000 – No accessory attached (default) 001 – Reserved 010 – Reserved 011 – Reserved 100 – Audio accessory 101 – Audio charged thru accessory 110 – Debug accessory when the TUSB320 device is connected as a DFP. 111 – Debug accessory when the TUSB320 device is connected as a UFP.
0	ACTIVE_CABLE_DETECTION	RU	0	This flag indicates that an active cable has been plugged into the Type-C connector. When this field is set, an active cable is detected.

7.5.3 CSR Registers (address = 0x09)

Figure 6. CSR Registers (address = 0x09)

7	6	5	4	3	2	1	0
ATTACHED_STATE		CABLE_DIR	INTERRUPT_STATUS	—	DRP_DUTY_CYCLE		DISABLE_UFP_ACCESSORY
RU		RU	RCU	R	RW		RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. CSR Registers (address = 0x09)

Bit	Field	Type	Reset	Description
7:6	ATTACHED_STATE	RU	00	This is an additional method to communicate attach other than the ID pin. These bits can be read by the application to determine what was attached. 00 – Not attached (default) 01 – Attached.SRC (DFP) 10 – Attached.SNK (UFP) 11 – Attached to an accessory
5	CABLE_DIR	RU	1	Cable orientation. The application can read these bits for cable orientation information. 0 – CC1 1 – CC2 (default)
4	INTERRUPT_STATUS	RCU	0	The INT pin is pulled low whenever a CSR with RU in Access field changes. When a CSR change has occurred this bit should be held at 1 until the application clears it. A write of 1'b1 is required to clear this field. 0 – Clear 1 – Interrupt (When INT_N is pulled low, this bit will be 1.) Note: SW must make sure the INTERRUPT_STATUS has been cleared to zero. Rewrites to this register are needed for the INT_N to be correctly asserted for all interrupt events.
3	Reserved	R	0	Reserved
2:1	DRP_DUTY_CYCLE	RW	00	Percentage of time that a DRP advertises DFP during tDRP 00 – 30% (default) 01 – 40% 10 – 50% 11 – 60%
0	DISABLE_UFP_ACCESSORY	RW	0	Settings this field will disable UFP accessory support. 0 – UFP accessory support enabled (Default) 1 – UFP accessory support disabled

7.5.4 CSR Registers (address = 0x0A)

Figure 7. CSR Registers (address = 0x0A)

7	6	5	4	3	2	1	0
DEBOUNCE		MODE_SELECT		I^2C_SOFT_RESET	SOURCE_PREF		DISABLE_TERM
RW		RW		RSU	RW		RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. CSR Registers (address = 0x0A)

Bit	Field	Type	Reset	Description
7:6	DEBOUNCE	RW	00	The nominal amount of time the TUSB320 device debounces the voltages on the CC pins. 00 – 168 ms (default) 01 – 118 ms 10 – 134 ms 11 – 152 ms
5:4	MODE_SELECT	RW	00	This register can be written to set the TUSB320 device mode operation. The ADDR pin must be set to I^2C mode. If the default is maintained, the TUSB320 device operates according to the PORT pin levels and modes. 00 – Maintain mode according to PORT pin selection (default) 01 – UFP mode (unattached.SNK) 10 – DFP mode(unattached.SRC) 11 – DRP mode(start from unattached.SNK)
3	I^2C_SOFT_RESET	RSU	0	This resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers can be affected after setting this bit: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR
2:1	SOURCE_PREF	RW	00	This field controls the TUSB320 behavior when configured as a DRP. 00 – Standard DRP (default) 01 – DRP will perform Try.SNK. 10 – Reserved. 11 – DRP will perform Try.SRC.
0	DISABLE_TERM	RW	0	This field will disable the termination on the CC pins and transition the CC state machine of the TUSB320 device to the Disable State. 0 – Termination enabled according to Port (Default) 1 – Termination disabled and state machine held in Disabled state.

7.5.5 CSR Registers (address = 0x45)

Figure 8. CSR Registers (address = 0x45)

7	6	5	4	3	2	1	0
—					DISABLE_RD_RP		—
R					RW		RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. CSR Registers (address = 0x45)

Bit	Field	Type	Reset	Description
7:3	Reserved	R	00000	Reserved
2	DISABLE_RD_RP	RW	0	When this field is set, Rd and Rp are disabled. 0 – Normal operation (default) 1 – Disable Rd and Rp
1:0	Reserved	RW	00	For TI internal use only. Do not change default value.

7.5.6 CSR Registers (address = 0xA0)

Figure 9. CSR Registers (address = 0xA0)

7	6	5	4	3	2	1	0
REVISION							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. CSR Registers (address = 0xA0)

Bit	Field	Type	Reset	Description
7:0	REVISION	R	0x02	Revision of TUSB320. Defaults to 0x02.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB320 device is a Type-C configuration channel logic and port controller. The TUSB320 device can detect when a Type-C device is attached, what type of device is attached, the orientation of the cable, and power capabilities (both detection and broadcast). The TUSB320 device can be used in a source application (DFP), in a sink application (UFP), or a combination source/sink application (DRP).

8.2 Typical Application

8.2.1 DRP in I²C Mode

Figure 10 and Figure 11 show a Type-C configuration for the DRP mode.

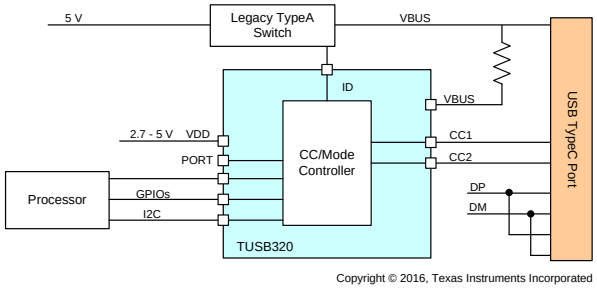


Figure 10. TUSB320 in DRP Mode Supporting Default Implementation

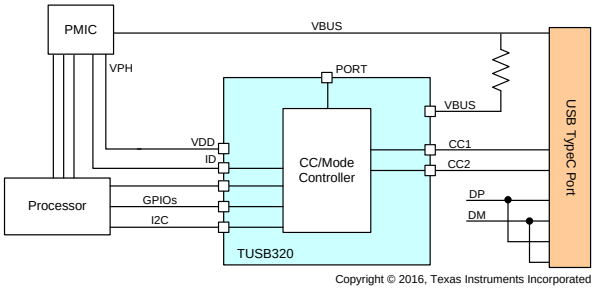


Figure 11. TUSB320 in DRP Mode Supporting Advanced Power Delivery

Figure 12 shows the TUSB320 device configured as a DRP in I²C mode.

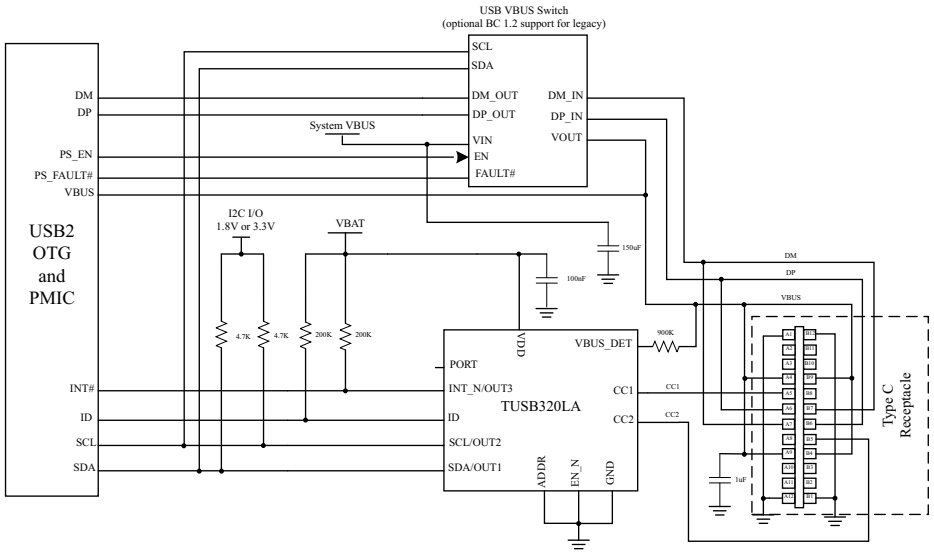


Figure 12. DRP in I²C Mode Schematic

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 13:

Table 13. Design Requirements for DRP in I^2C Mode

DESIGN PARAMETER	VALUE
V_{DD} (2.75 V to 5 V)	VBAT (less than 5 V)
Mode (I^2C or GPIO)	I^2C: ADDR pin must be pulled down or pulled up
I^2C address (0x67 or 0x47)	0x47: ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DRP: PORT pin is NC
Shutdown support	No

8.2.1.2 Detailed Design Procedure

The TUSB320 device supports a V_{DD} in the range of 2.75 V to 5 V. In this particular use case, VBAT which must be in the required V_{DD} range is connected to the V_{DD} pin. A 100-nF capacitor is placed near V_{DD}.

The TUSB320 device is placed into I^2C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The TUSB320LA device can enter shutdown mode by pulling the EN_N pin high, which puts the TUSB320LA device into a low power state. In this case, external control of the EN_N pin is not implemented and therefore the EN_N pin is tied to GND. The TUSB320HA device can enter shutdown mode by pulling the EN pin low, which puts the TUSB320HA device into a low power state. In this case, external control of the EN pin is not implemented and therefore the EN pin is tied to 1.8 V or 3.3 V.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The ID pin is used to indicate when a connection has occurred if the TUSB320 device is a DFP while configured for DRP. An OTG USB controller can use this pin to determine when to operate as a USB Host or USB Device. When this pin is driven low, the OTG USB controller functions as a host and then enables V_{BUS}. The Type-C standard requires that a DFP not enable V_{BUS} until the DFP is in the Attached.SRC state. If the ID pin is not low but V_{BUS} is detected, then OTG USB controller functions as a device. The ID pin is open drain output and requires an external pullup resistor. THe ID pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is not connected, the TUSB320 device is in DRP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I^2C interface.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB320 device in a DRP mode, it alternates between UFP and DFP. If the TUSB320 device connects as a UFP, the large bulk capacitance must be removed.

Table 14. USB2 Bulk Capacitance Requirements

PORT CONFIGURATION	MIN	MAX	UNIT
Downstream facing port (DFP)	120		µF
Upstream facing port (UFP)	1	10	µF

8.2.1.3 Application Curves

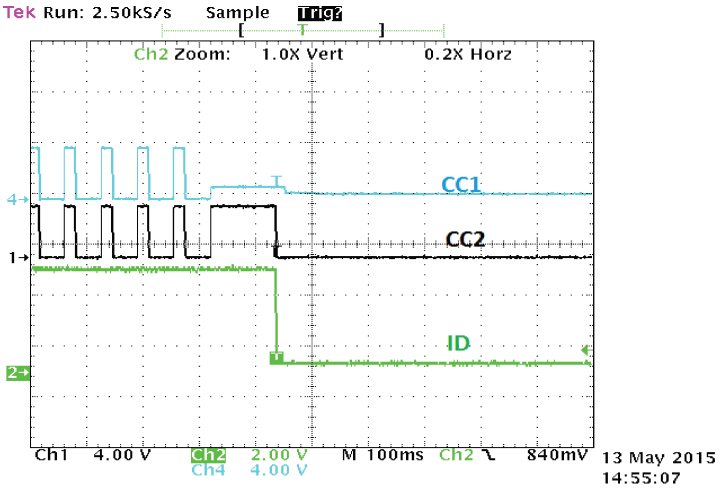


Figure 13. Application Curve for DRP in I²C Mode

8.2.2 DFP in I²C Mode

Figure 14 and Figure 15 show a Type-C configuration for the DFP mode.

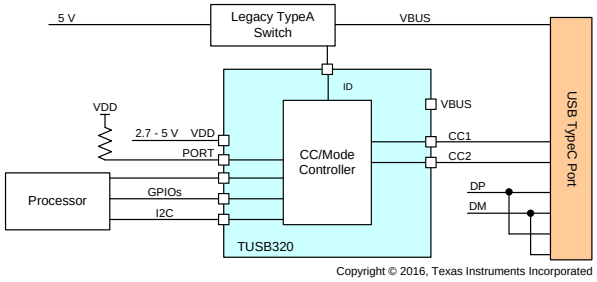


Figure 14. TUSB320 in DFP Mode Supporting Default Implementation

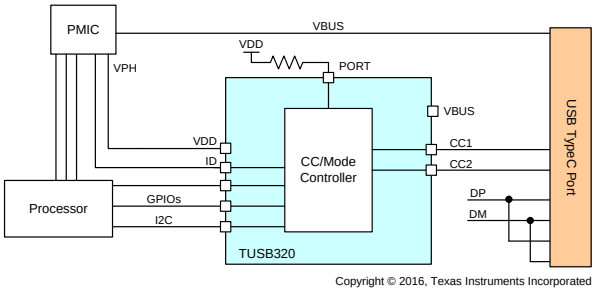


Figure 15. TUSB320 in DFP Mode Supporting Advanced Power Delivery

Figure 16 shows the TUSB320 device configured as a DFP in I²C mode.

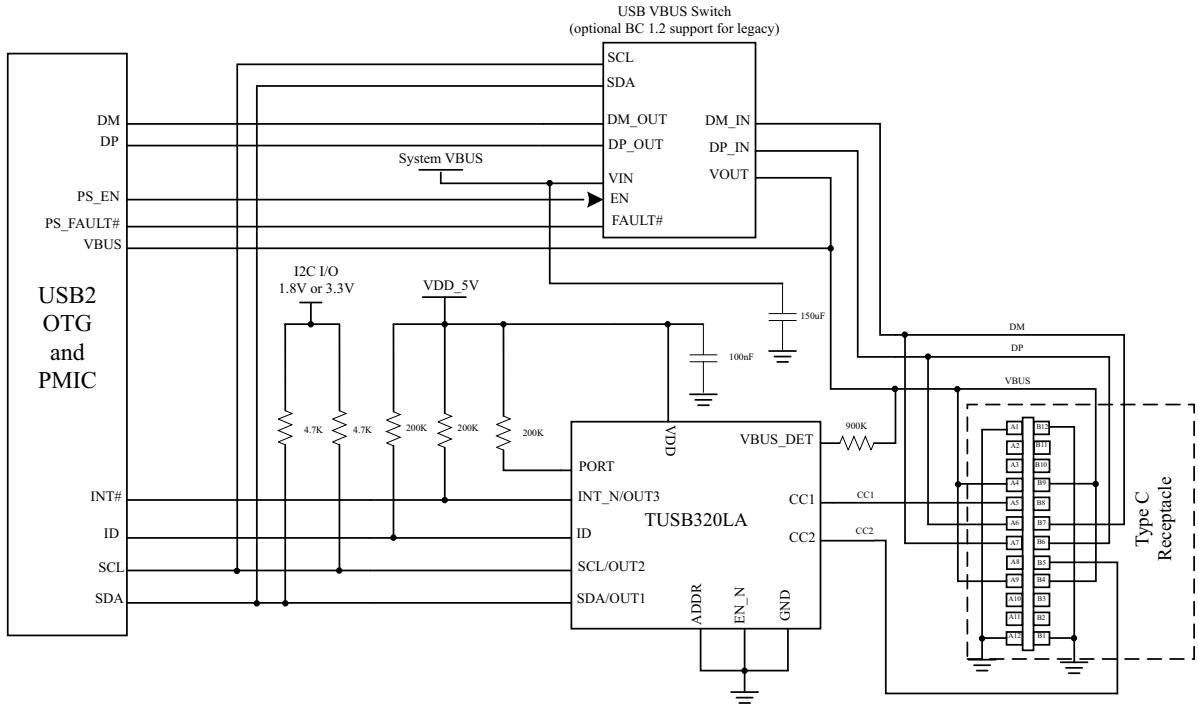


Figure 16. DFP in I²C Mode Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 15:

Table 15. Design Requirements for DFP in I²C Mode

DESIGN PARAMETER	VALUE
V_{DD} (2.75 V to 5 V)	5 V
Mode (I²C or GPIO)	I²C: ADDR pin must be pulled down or pulled up
I²C address (0x67 or 0x47)	0x47: ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DFP: PORT pin is pulled up
Shutdown support	No

8.2.2.2 Detailed Design Procedure

The TUSB320 device supports a V_{DD} in the range of 2.75 V to 5 V. In this particular case, V_{DD} is set to 5 V. A 100-nF capacitor is placed near V_{DD}.

The TUSB320 device is placed into I^2C mode by either pulling the ADDR pin high or low. In this particular case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The TUSB320LA device can enter shutdown mode by pulling the EN_N pin high, which puts the TUSB320LA device into a low power state. In this case, external control of the EN_N pin is not implemented and therefore the EN_N pin is tied to GND. The TUSB320HA device can enter shutdown mode by pulling the EN pin low, which puts the TUSB320HA device into a low power state. In this case, external control of the EN pin is not implemented and therefore the EN pin is tied to 1.8 V or 3.3 V.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled high, the TUSB320 device is in DFP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I^2C interface.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB320 device in a DFP mode, a bulk capacitance of at least 120 µF is required. In this particular case, a 150-µF capacitor was chosen.

8.2.2.3 Application Curves

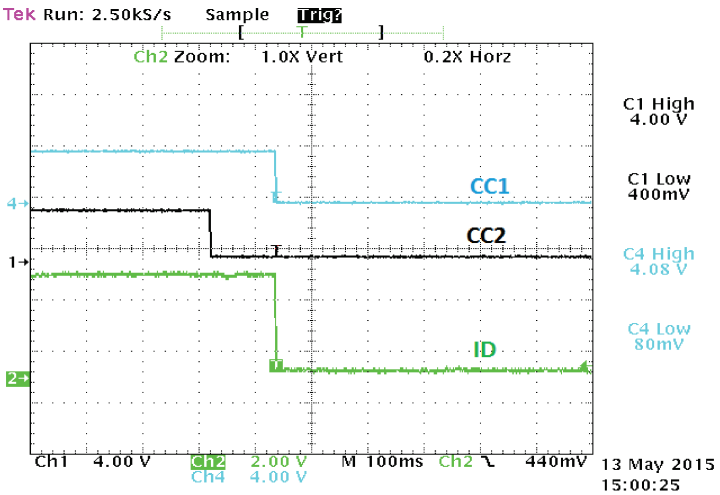


Figure 17. Application Curve for DFP in I^2C Mode

8.2.3 UFP in I²C Mode

Figure 18 and Figure 19 show a Type-C configuration for the UFP mode.

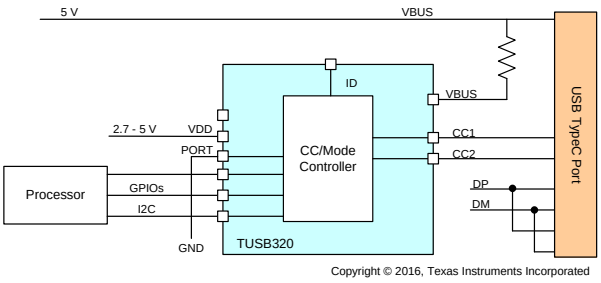


Figure 18. TUSB320 in UFP Mode Supporting Default Implementation

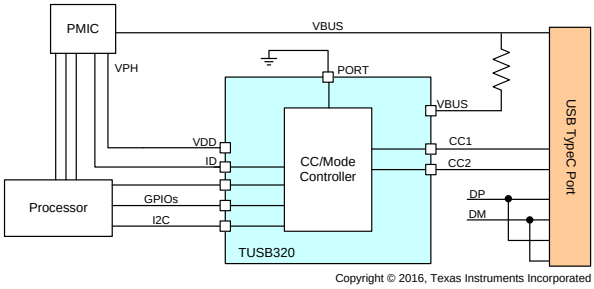


Figure 19. TUSB320 in UFP Mode Supporting Advanced Power Delivery

Figure 20 shows the TUSB320 device configured as a UFP in I²C mode.

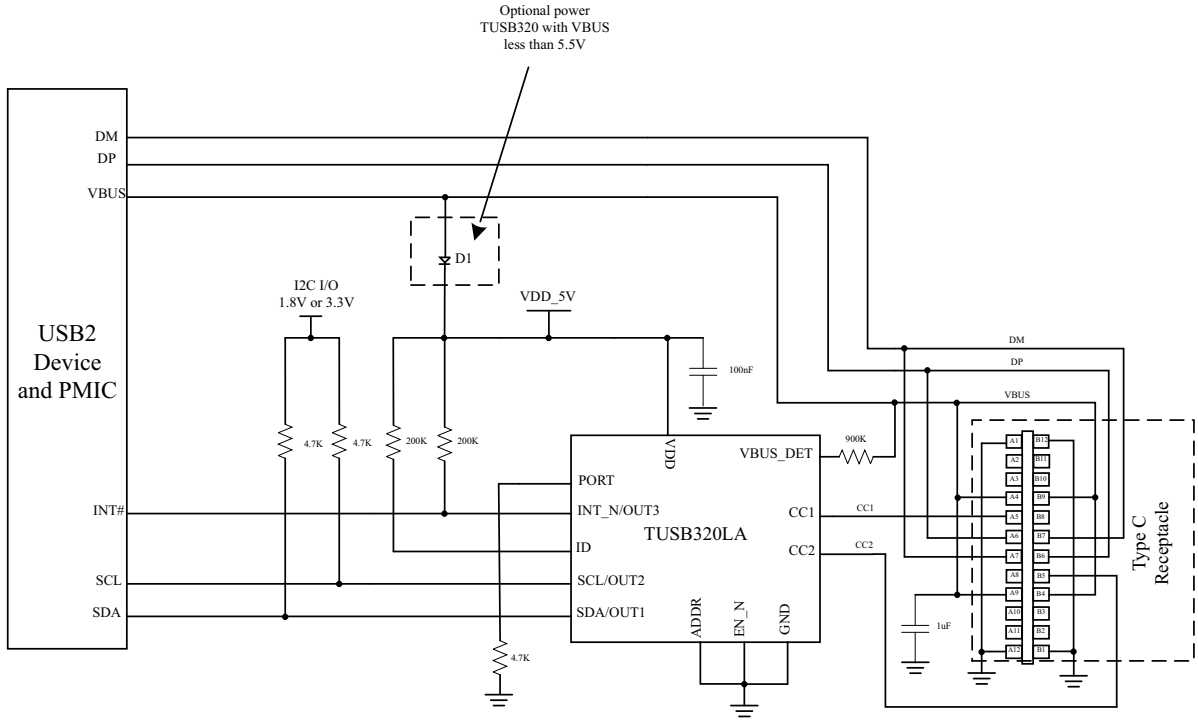


Figure 20. UFP in I²C Mode Schematic

8.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 16:

Table 16. Design Requirements for UFP in I²C Mode

DESIGN PARAMETER	VALUE
V_{DD} (2.75 V to 5 V)	5 V
Mode (I²C or GPIO)	I²C: ADDR pin must be pulled down or pulled up
I²C address (0x67 or 0x47)	0x47: ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	UFP: PORT pin is pulled down

Table 16. Design Requirements for UFP in I²C Mode (continued)

DESIGN PARAMETER	VALUE
Shutdown support	No

8.2.3.2 Detailed Design Procedure

The TUSB320 device supports a V_{DD} in the range of 2.75 V to 5 V. In this particular case, V_{DD} is set to 5 V. A 100-nF capacitor is placed near V_{DD}. If V_{BUS} is guaranteed to be less than 5.5 V, powering the TUSB320 device through a diode can be implemented.

The TUSB320 device is placed into I^2C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The TUSB320LA device can enter shutdown mode by pulling the EN_N pin high, which puts the TUSB320LA device into a low power state. In this case, external control of the EN_N pin is not implemented and therefore the EN_N pin is tied to GND. The TUSB320HA device can enter shutdown mode by pulling the EN pin low, which puts the TUSB320HA device into a low power state. In this case, external control of the EN pin is not implemented and therefore the EN pin is tied to 1.8 V or 3.3 V.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB320 I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled low, the TUSB320 device is in UFP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I^2C interface.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB320 device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB320 device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB320 device in a UFP mode, a bulk capacitance between 1 µF to 10 µF is required. In this particular case, a 1-µF capacitor was chosen.

8.2.3.3 Application Curves

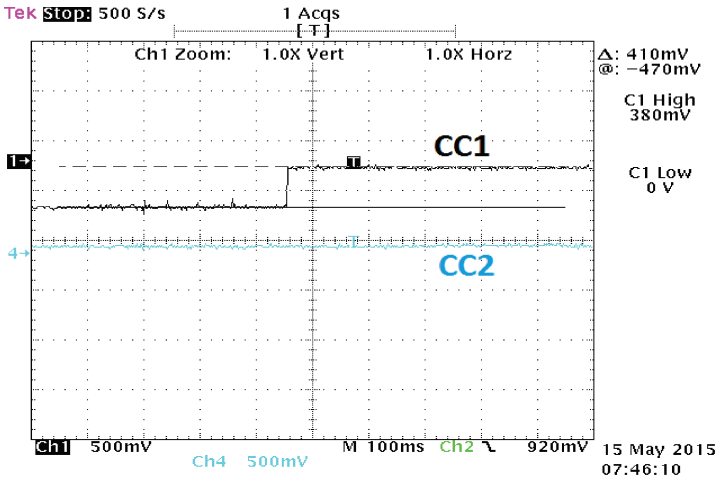


Figure 21. Application Curve for UFP in I^2C Mode

8.3 Initialization Setup

8.3.1 TUSB320LA Initialization Procedure

1. System is powered off (device has no V_{DD}). The TUSB320LA device is configured internally in UFP mode with Rds on CC pins (dead battery).
2. V_{DD} ramps – POR circuit. V_{DD} must ramp within 25 ms or less. IO pull-up power rail (i.e. pull up on ID, INT, SCL, SDA, ADDR, PORT) must ramp with V_{DD} or lag after V_{DD}.
3. I^2C supply ramps up.
4. The TUSB320LA device enters unattached mode and determines the voltage level from the PORT pin. This determines the mode in which the TUSB320LA device operates (DFP, UFP, DRP).
5. The TUSB320LA device monitors the CC pins as a DFP and V_{BUS} for attach as a UFP.
6. The TUSB320LA device enters active mode when attach has been successfully detected.

8.3.2 TUSB320HA Initialization Procedure

1. System is powered off (device has no V_{DD}). The TUSB320HA device is configured internally in UFP mode with Rds on CC pins (dead battery).
2. V_{DD} ramps – POR circuit. V_{DD} must ramp within 25 ms or less. IO pull-up power rail (i.e. pull up on ID, INT, SCL, SDA, ADDR, PORT) must ramp with V_{DD} or lag after V_{DD}.
3. I^2C supply ramps up.
4. The TUSB320HA device enters unattached mode and determines the voltage level from the PORT pin. This determines the mode in which the TUSB320HA device operates (DFP, UFP, DRP).
5. The TUSB320HA device monitors the CC pins as a DFP and V_{BUS} for attach as a UFP.
6. The TUSB320HA device enters active mode when attach has been successfully detected.

9 Power Supply Recommendations

The TUSB320 device has a wide power supply range from 2.7 to 5 V. The TUSB320 device can be run off of a system power such as a battery.

10 Layout

10.1 Layout Guidelines

1. An extra trace (or stub) is created when connecting between more than two points. A trace connecting pin A6 to pin B6 will create a stub because the trace also has to go to the USB Host. Ensure that:
   - A stub created by short on pin A6 (DP) and pin B6 (DP) at Type-C receptacle does not exceed 3.5 mm.
   - A stub created by short on pin A7 (DM) and pin B7 (DM) at Type-C receptacle does not exceed 3.5 mm.
2. A 100-nF capacitor should be placed as close as possible to the TUSB320 V_{DD} pin.

10.2 Layout Example

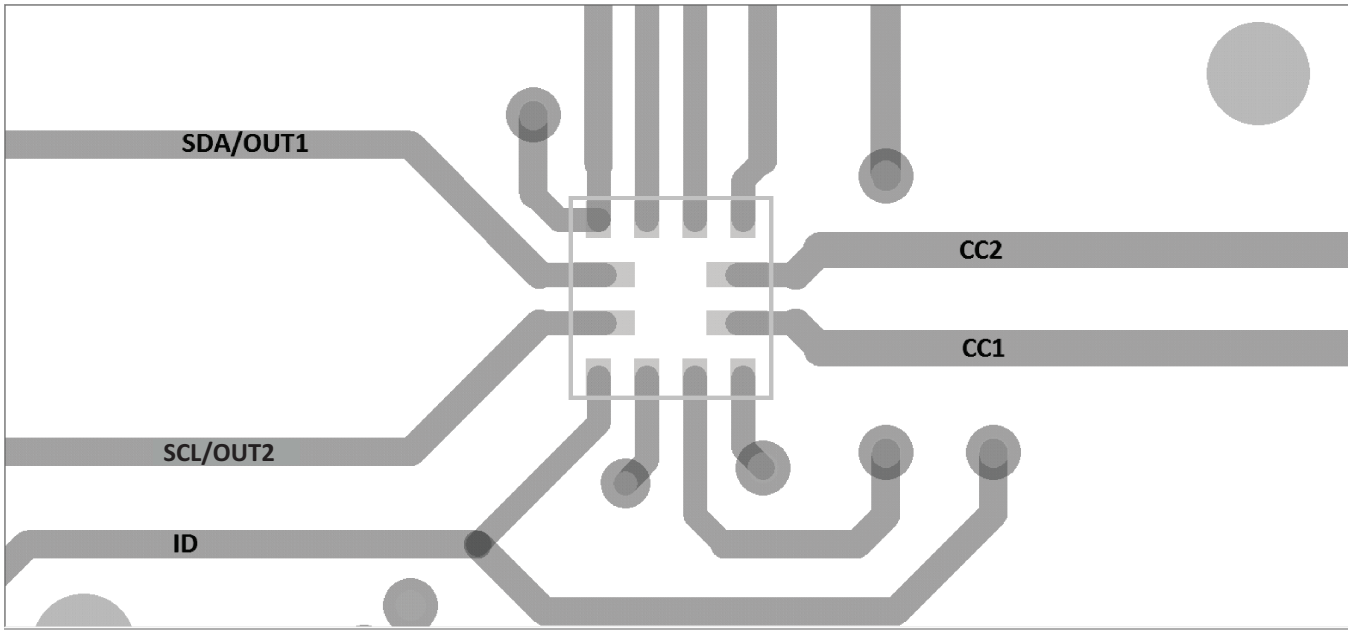


Figure 22. TUSB320 Layout

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 17. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TUSB320LAI	Click here	Click here	Click here	Click here	Click here
TUSB320HAI	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB320HAIRWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA	Samples
TUSB320LAIRWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

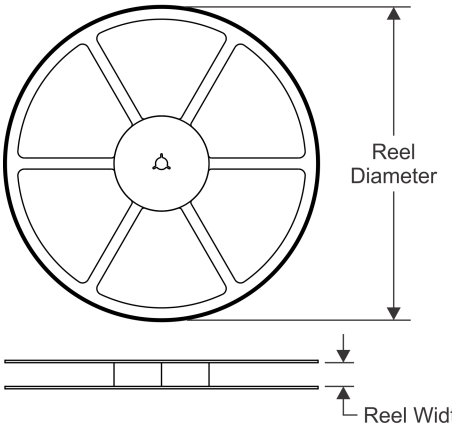
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

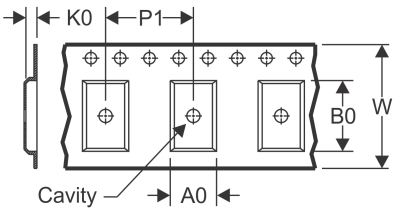
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

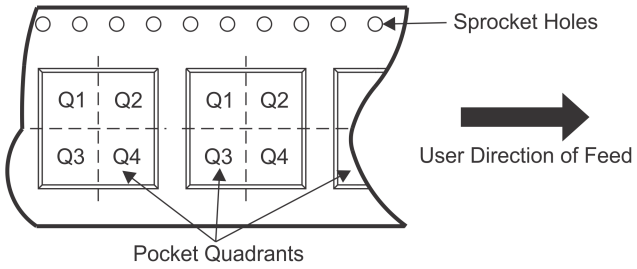


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

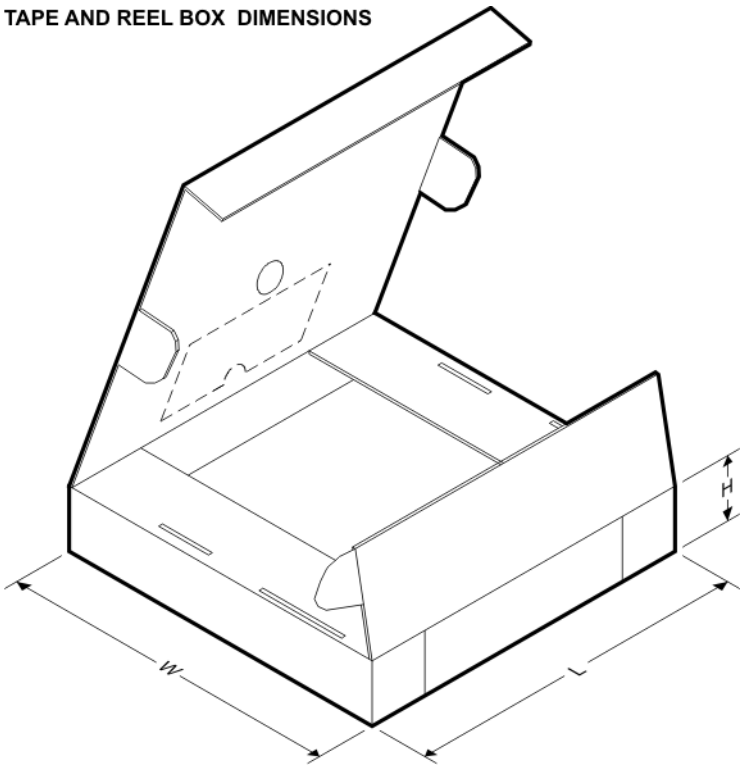
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB320HAIRWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.61	4.0	8.0	Q2
TUSB320LAIRWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.61	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

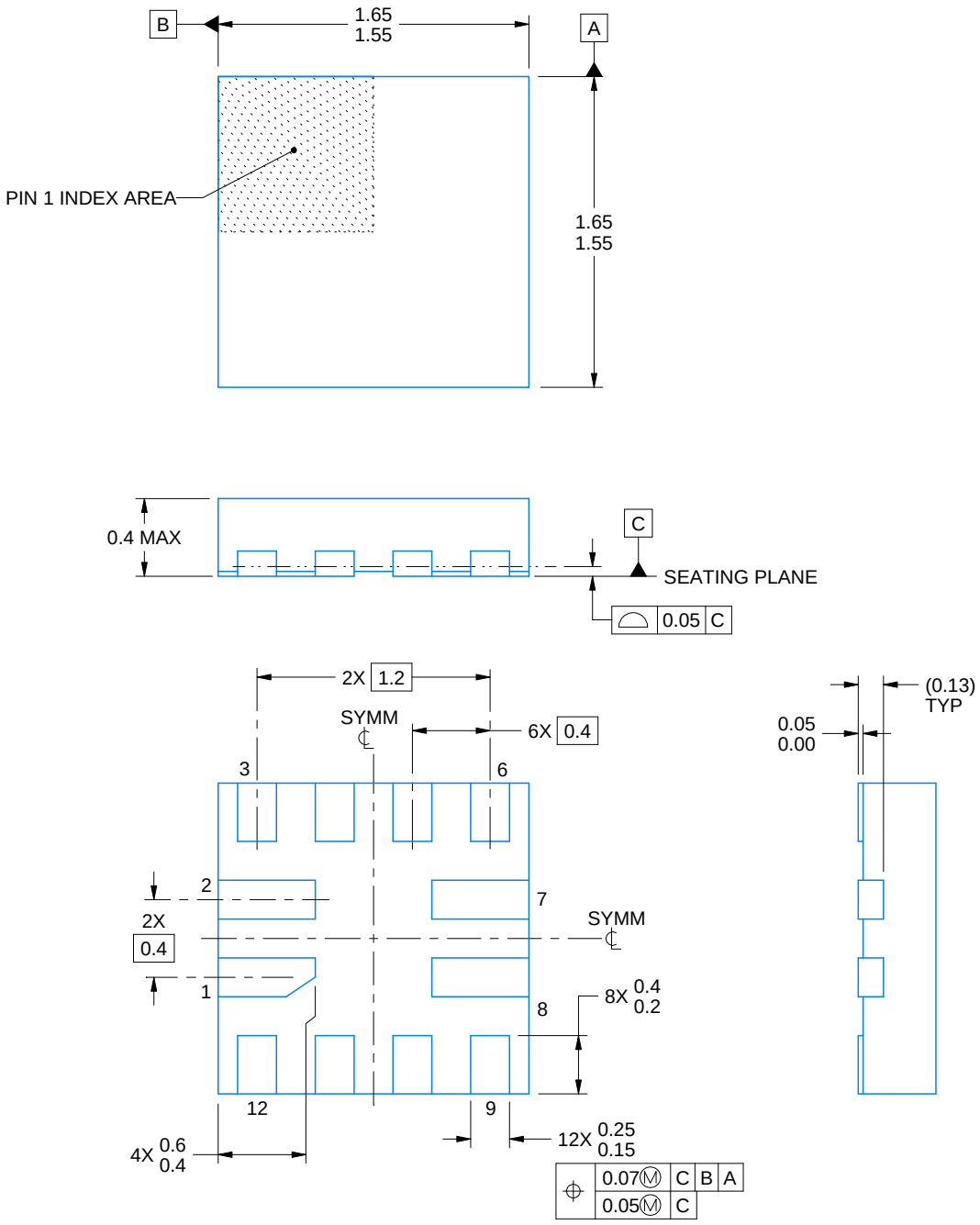
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB320HAIRWBR	X2QFN	RWB	12	3000	195.0	200.0	45.0
TUSB320LAIRWBR	X2QFN	RWB	12	3000	195.0	200.0	45.0

PACKAGE OUTLINE

RWB0012A

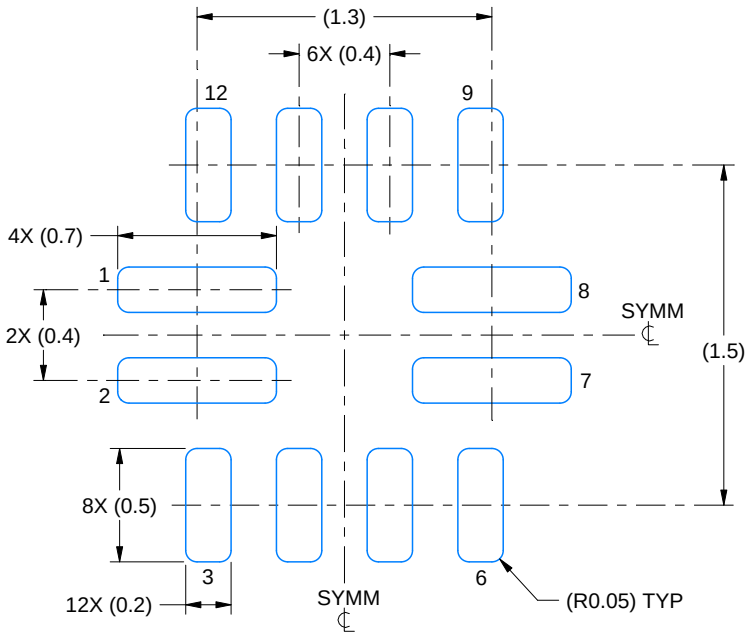
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

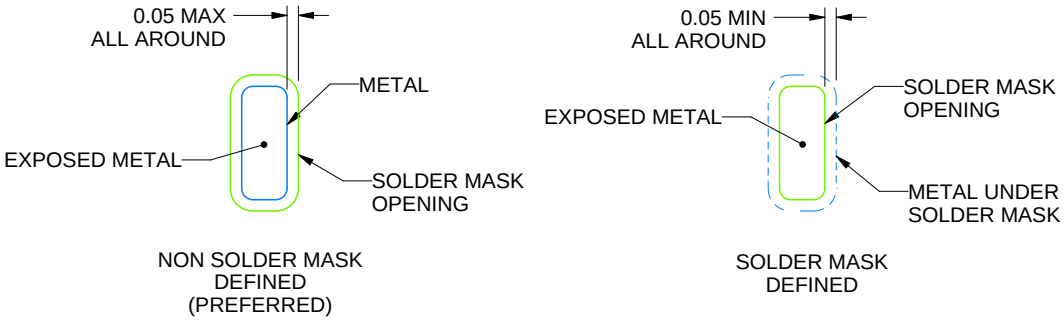


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

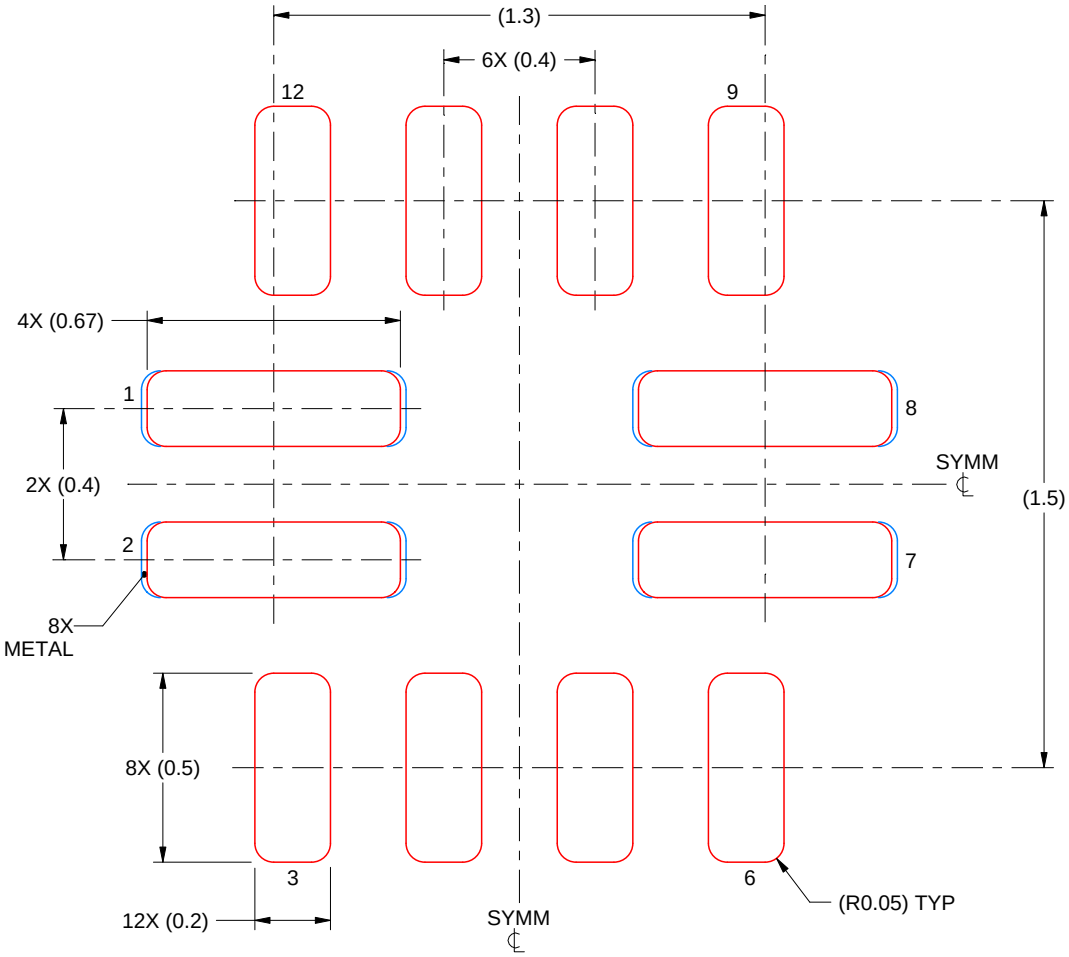
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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