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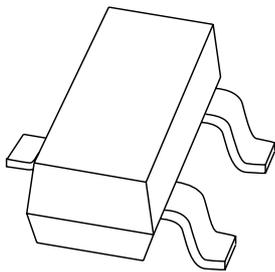
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Kind regards,

Team Nexperia

# DATA SHEET



## **PBSS4240T**

40 V; 2 A NPN low  $V_{CEsat}$   
(BISS) transistor

Product data sheet  
Supersedes data of 2001 Jul 13

2004 Jan 09

# 40 V; 2 A NPN low $V_{CEsat}$ (BISS) transistor

**PBSS4240T**

**FEATURES**

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation
- Replacement for SOT89/SOT223 standard packaged transistors.

**APPLICATIONS**

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

**DESCRIPTION**

NPN low  $V_{CEsat}$  transistor in a SOT23 plastic package. PNP complement: PBSS5240T.

**MARKING**

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PBSS4240T	ZE*

**Note**

- \* = p: Made in Hong Kong.  
 \* = t: Made in Malaysia.  
 \* = W: Made in China.

**ORDERING INFORMATION**

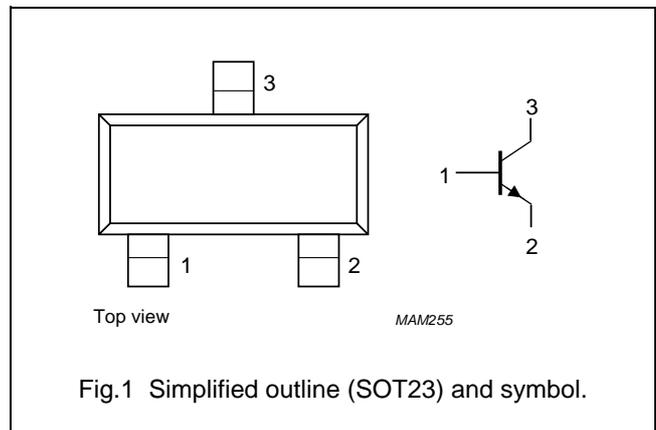
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS4240T	-	plastic surface mounted package; 3 leads	SOT23

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	40	V
$I_{CM}$	peak collector current	3	A
$R_{CEsat}$	equivalent on-resistance	<200	m $\Omega$

**PINNING**

PIN	DESCRIPTION
1	base
2	emitter
3	collector



40 V; 2 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4240T

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	40	V
$V_{CEO}$	collector-emitter voltage	open base	–	40	V
$V_{EBO}$	emitter-base voltage	open collector	–	5	V
$I_C$	collector current (DC)		–	2	A
$I_{CM}$	peak collector current		–	3	A
$I_{BM}$	peak base current		–	300	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	300	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	480	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	417	K/W
		in free air; note 2	260	K/W

**Notes**

1. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

40 V; 2 A NPN low  $V_{CEsat}$  (BISS) transistor

## PBSS4240T

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$I_E = 0; V_{CB} = 30\text{ V}$	–	–	100	nA
		$I_E = 0; V_{CB} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$I_C = 0; V_{EB} = 4\text{ V}$	–	–	100	nA
$h_{FE}$	DC current gain	$I_C = 100\text{ mA}; V_{CE} = 2\text{ V}$	350	470	–	
		$I_C = 500\text{ mA}; V_{CE} = 2\text{ V}$	300	450	–	
		$I_C = 1\text{ A}; V_{CE} = 2\text{ V}$	300	420	–	
		$I_C = 2\text{ A}; V_{CE} = 2\text{ V}$	150	250	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 1\text{ mA}$	–	45	70	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	70	100	mV
		$I_C = 750\text{ mA}; I_B = 15\text{ mA}$	–	120	180	mV
		$I_C = 1\text{ A}; I_B = 50\text{ mA}; \text{note 1}$	–	130	180	mV
		$I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	240	320	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = 500\text{ mA}; I_B = 50\text{ mA}; \text{note 1}$	–	140	<200	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	–	1.1	V
$V_{BEon}$	base-emitter turn on voltage	$I_C = 100\text{ mA}; V_{CE} = 2\text{ V}$	–	–	0.75	V
$C_c$	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	15	20	pF
$f_T$	transition frequency	$I_C = 100\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	100	230	–	MHz

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

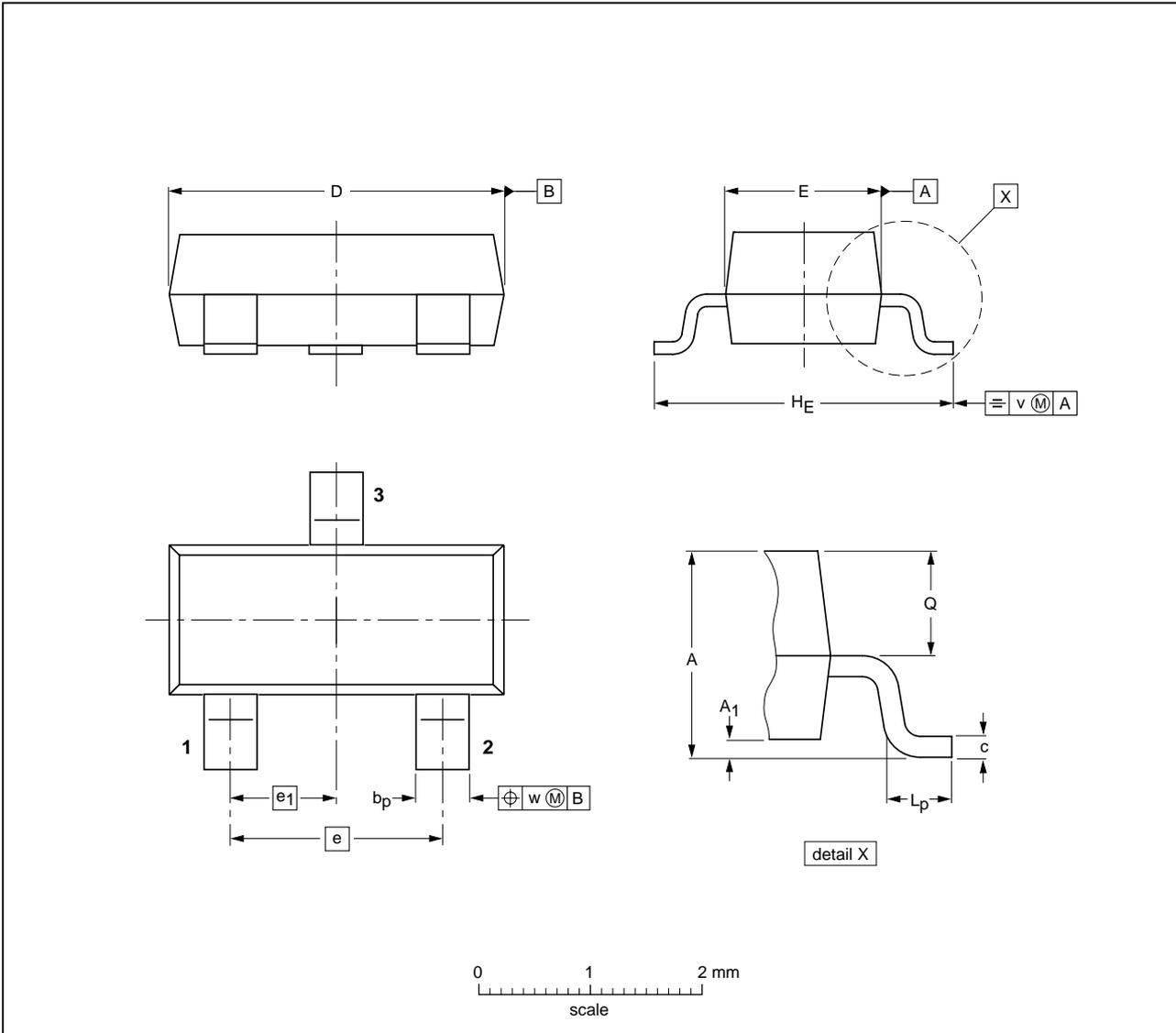
40 V; 2 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4240T

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT23		TO-236AB			<del>04-11-04</del> 06-03-16

40 V; 2 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4240T

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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