OptiMOS™ 2 + OptiMOS™-P 2 Small Signal Transistor

Features

· Complementary P + N channel

· Enhancement mode

· Super Logic level (2.5V rated)

· Avalanche rated

· Qualified according to AEC Q101

· 100% lead-free; RoHS compliant

· Halogen-free according to IEC61249-2-21

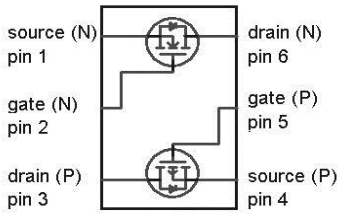
Halogen-Free

AEC Qualified

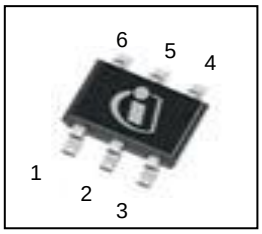
RoHS

Product Summary

		P	N	
V_{DS}		-20	20	V
$R_{DS(on),max}$	V_{GS}=±4.5 V	1200	350	mΩ
	V_{GS}=±2.5 V	2100	600	
I_D		-0.53	0.95	A



PG-SOT-363



Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSD235C	PG-SOT-363	H6327: 3000 pcs / reel	X9s	Yes	Non dry

Maximum ratings, at T_j=25 °C, unless otherwise specified [1)]

Parameter	Symbol	Conditions	Value		Unit
			P	N	
Continuous drain current	I_D	T_A=25 °C	-0.53	0.95	A
		T_A=70 °C	-0.46	0.76	
Pulsed drain current	$I_{D,pulse}$	T_A=25 °C	-2.1	3.8	
Avalanche energy, single pulse	E_{AS}	P: I_D=-0.53 A, N: I_D=0.95 A, R_{GS}=25 Ω	1.4	1.6	mJ
Gate source voltage	V_{GS}		±12		V
Power dissipation	P_{tot}	T_A=25 °C	0.5		W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
ESD class		JESD22-A114-HBM	0 (<250V)		°C
Soldering temperature	T_{solder}		260		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

[1)] Remark: only one of both transistors active

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Thermal characteristics							
Thermal resistance, junction - ambient	P	R_{thJA}	minimal footprint [2]	-	-	250	K/W
	N						
Electrical characteristics, at T_j=25 °C, unless otherwise specified							
Static characteristics							
Drain-source breakdown voltage	P	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250 µA	-	-	-20	V
	N		V_{GS}=0 V, I_D=250 µA	20	-	-	
Gate threshold voltage	P	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-1.5 µA	-1.2	-0.9	-0.6	
	N		V_{DS}=V_{GS}, I_D=1.6 µA	0.7	0.95	1.2	
Zero gate voltage drain current	P	I_{DSS}	V_{DS}=-20 V, V_{GS}=0 V, T_j=25 °C	-	-	-1	µA
	N		V_{DS}=20 V, V_{GS}=0 V, T_j=25 °C	-	-	1	
	P		V_{DS}=-20 V, V_{GS}=0 V, T_j=150 °C	-	-	-100	
	N		V_{DS}=20 V, V_{GS}=0 V, T_j=150 °C	-	-	100	
Gate-source leakage current	P	I_{GSS}	V_{GS}=±12 V, V_{DS}=0 V	-	-	±100	nA
	N						
Drain-source on-state resistance	P	$R_{DS(on)}$	V_{GS}=-2.5 V, I_D=-0.17 A	-	1221	2100	mΩ
	N		V_{GS}=2.5 V, I_D=0.29 A	-	415	600	
	P		V_{GS}=-4.5V, I_D=-0.53 A	-	745	1200	
	N		V_{GS}=4.5 V, I_D=0.95 A	-	266	350	
Transconductance	P	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-0.46 A	-	0.7	-	S
	N		$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=0.76 A	-	2	-	

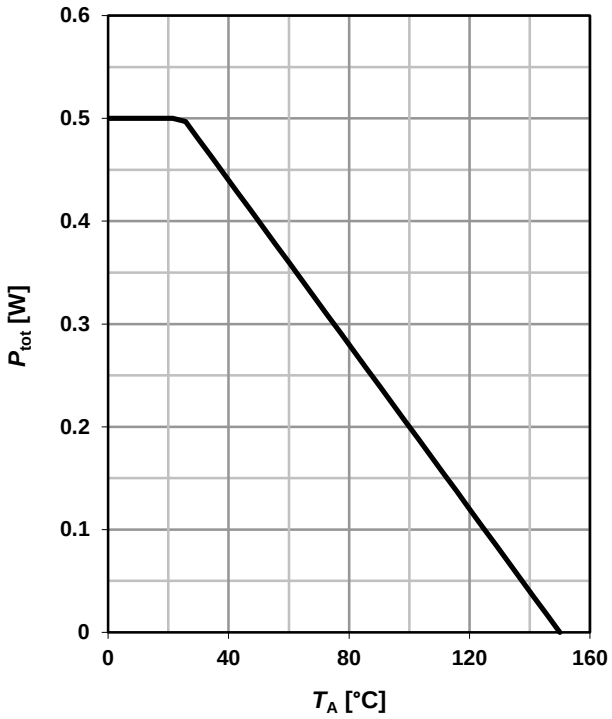
[2] Performed on 40mm^2 FR4 PCB. The traces are 1mm wide, 70µm thick and 20mm long; they are present on both sides of the PCB

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Dynamic characteristics							
Input capacitance	P	C_{iss}	V_{GS}=0 V, P: V_{DS}=-10 V, N: V_{DS}= 10 V, f=1 MHz	-	37	-	pF
	N			-	47	-	
Output capacitance	P	C_{oss}		-	17	-	
	N			-	24	-	
Reverse transfer capacitance	P	C_{rss}		-	14	-	
	N			-	3	-	
Turn-on delay time	P	$t_{d(on)}$	P: V_{DD}=-10 V, V_{GS}=-4.5 V, R_G=6 Ω, I_D=-0.53 A N: V_{DD}=10 V, V_{GS}=4.5 V, R_G=6 Ω, I_D=0.95 A	-	3.8	-	ns
	N			-	3.8	-	
Rise time	P	t_r		-	5.0	-	
	N			-	3.6	-	
Turn-off delay time	P	$t_{d(off)}$		-	5.1	-	
	N			-	4.5	-	
Fall time	P	t_f		-	3.2	-	
	N			-	1.2	-	
Gate Charge Characteristics							
Gate to source charge	P	Q_{gs}	V_{DD}=-10 V, I_D=-0.53 A, V_{GS}=0 to -4.5 V	-	-0.09	-	nC
Gate to drain charge		Q_{gd}		-	-0.2	-	
Switching charge		Q_g		-	-0.4	-	
Gate plateau voltage		$V_{plateau}$		-	-2.4	-	
Gate to source charge	N	Q_{gs}	V_{DD}=16 V, I_D=0.95 A, V_{GS}=0 to 4.5 V	-	0.11	-	
Gate to drain charge		Q_{gd}		-	0.09	-	
Switching charge		Q_g		-	0.34	-	
Gate plateau voltage		$V_{plateau}$		-	2.4	-	

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Reverse Diode							
Diode continuous forward current	P	I_S	T_C=25 °C	-	-	-0.42	A
	N					0.5	
Diode pulse current	P	$I_{S,pulse}$		-	-	-2.1	
	N			-	-	3.8	
Diode forward voltage	P	V_{SD}	V_{GS}=0 V, I_F=-0.53 A, T_j=25 °C	-	-1	-1.2	V
	N		V_{GS}=0 V, I_F=0.95 A, T_j=25 °C	-	0.9	1.1	
Reverse recovery time	P	t_{rr}	V_R=±10 V, I_F=I_S, di_F/dt=100 A/µs	-	7.6	-	ns
	N			-	5.2	-	
Reverse recovery charge	P	Q_{rr}		-	1.1	-	nC
	N			-	0.97	-	

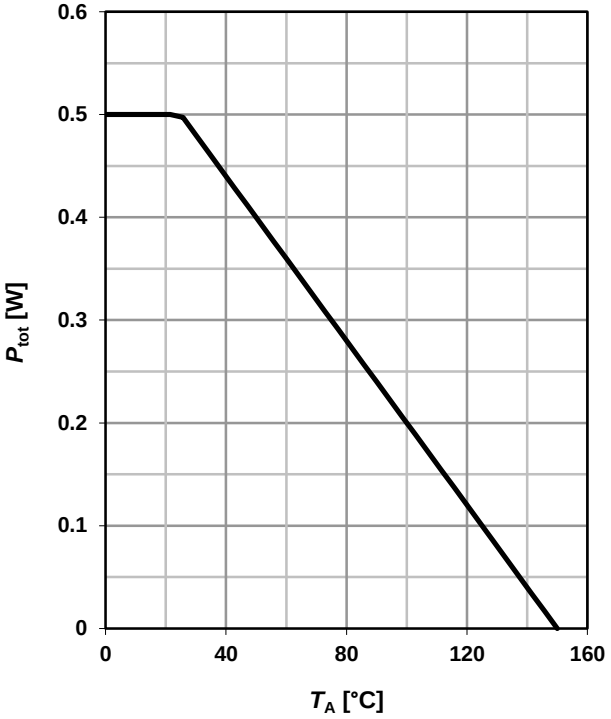
1 Power dissipation (P)

$P_{tot}=f(T_A)$



2 Power dissipation (N)

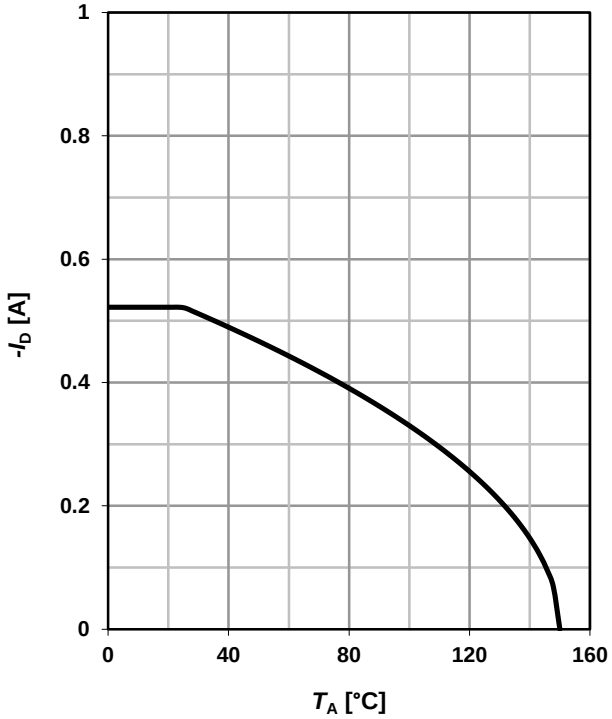
$P_{tot}=f(T_A)$



3 Drain current (P)

$I_D=f(T_A)$

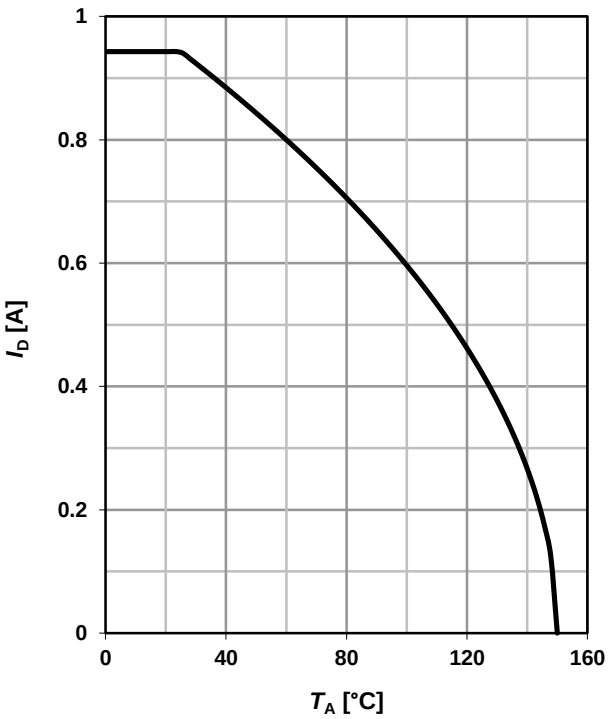
parameter: $V_{GS}\leq$-4.5 V



4 Drain current (N)

$I_D=f(T_A)$

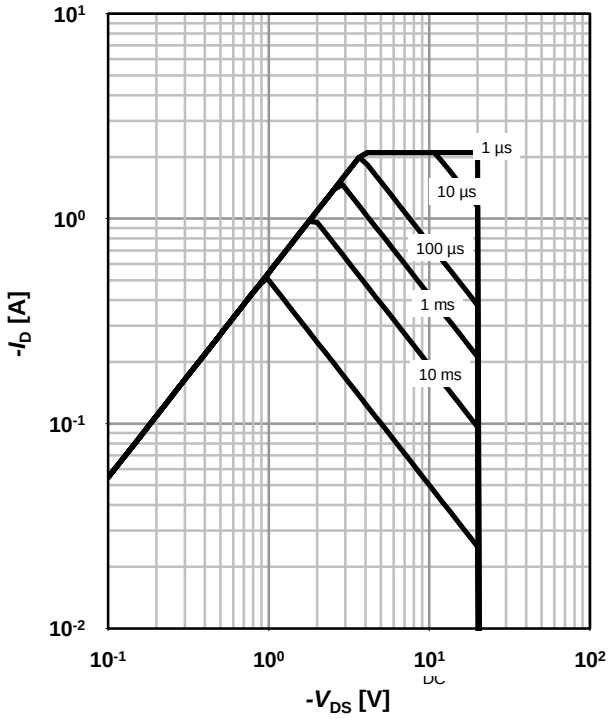
parameter: $V_{GS}\geq$4.5 V



5 Safe operating area (P)

I_D=f(V_{DS}); T_A=25 °C; D=0

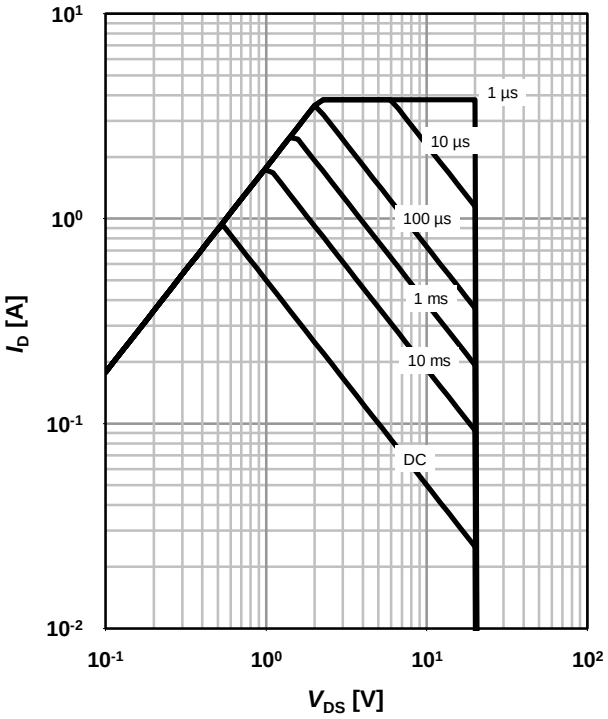
parameter: t_p



6 Safe operating area (N)

I_D=f(V_{DS}); T_A=25 °C; D=0

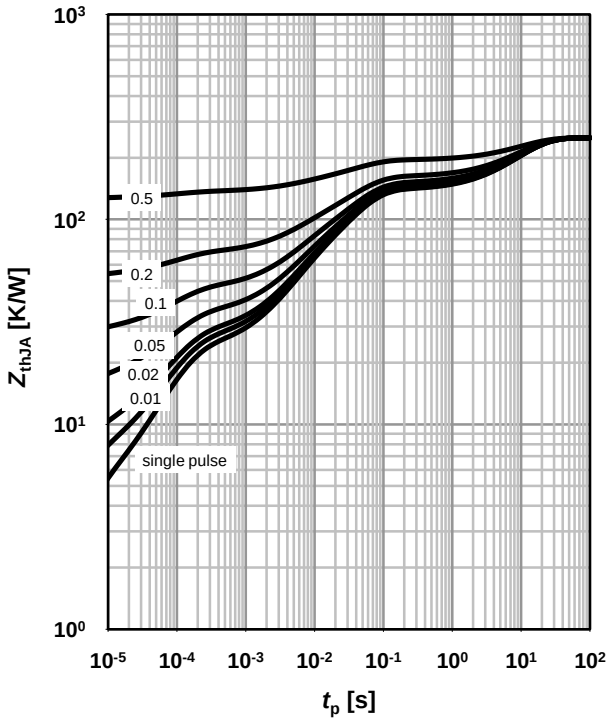
parameter: t_p



7 Max. transient thermal impedance (P)

Z_{thJA}=f(t_p)

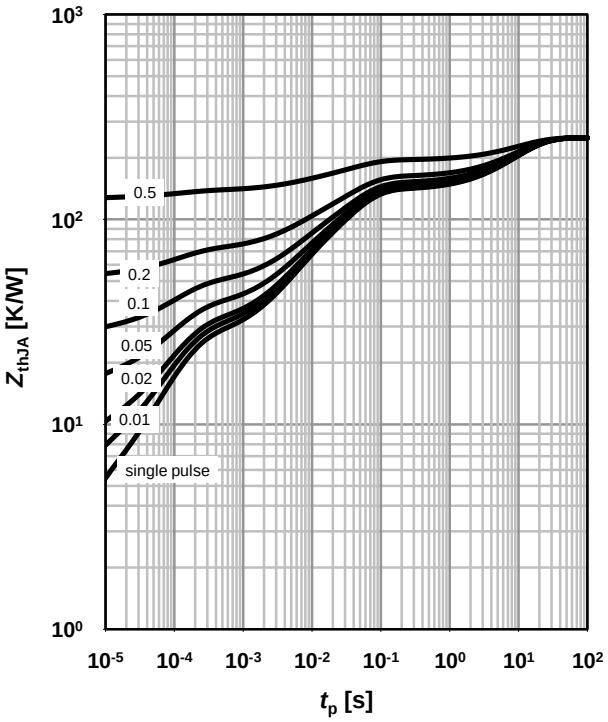
parameter: $D=t_p/T$



8 Max. transient thermal impedance (N)

Z_{thJA}=f(t_p)

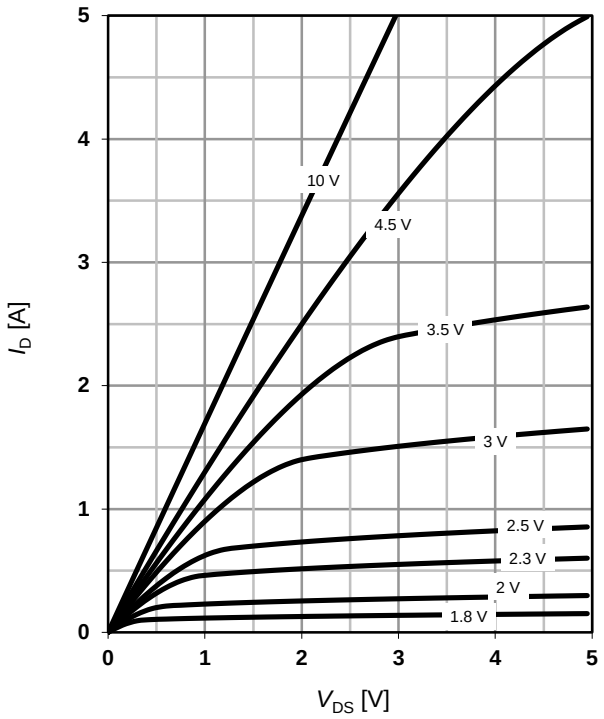
parameter: $D=t_p/T$



9 Typ. output characteristics (P)

I_D=f(V_{DS}); T_j=25 °C

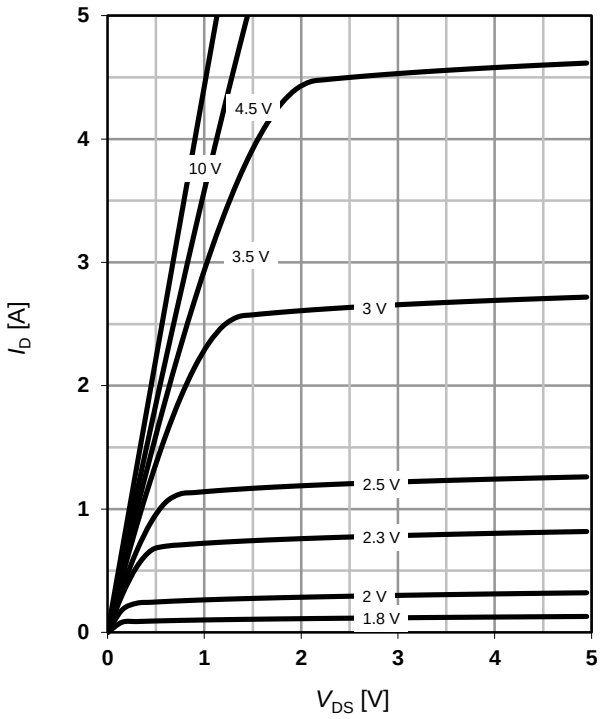
parameter: V_{GS}



10 Typ. output characteristics (N)

I_D=f(V_{DS}); T_j=25 °C

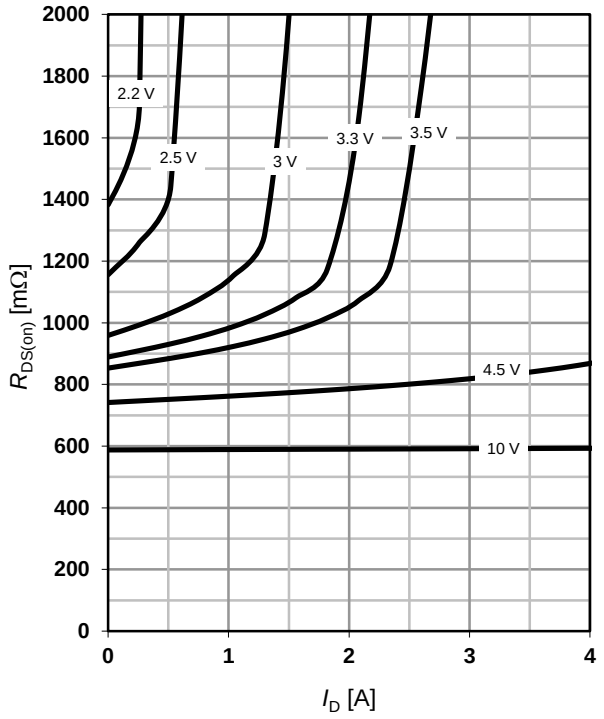
parameter: V_{GS}



11 Typ. drain-source on resistance (P)

$R_{DS(on)}$=f(I_D); T_j=25 °C

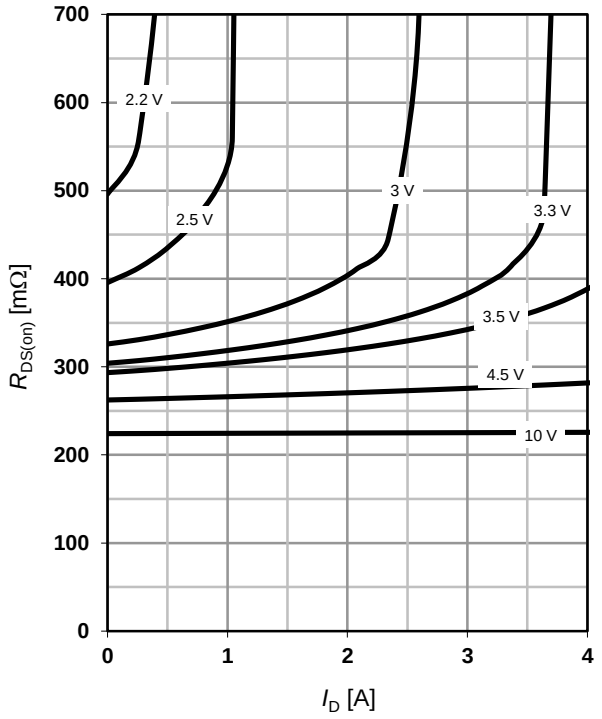
parameter: V_{GS}



12 Typ. drain-source on resistance (N)

$R_{DS(on)}$=f(I_D); T_j=25 °C

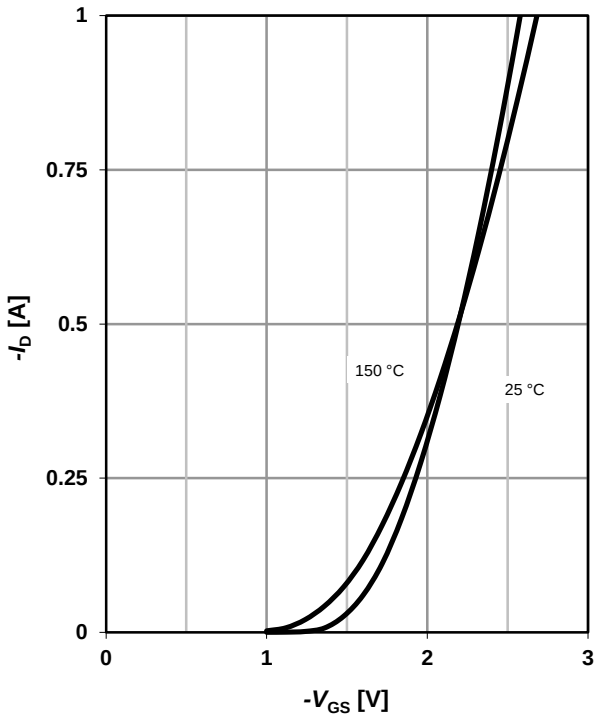
parameter: V_{GS}



13 Typ. transfer characteristics (P)

$I_D=f(V_{GS})$; $|V_{DS}|>2 | I_D| R_{DS(on)max}$

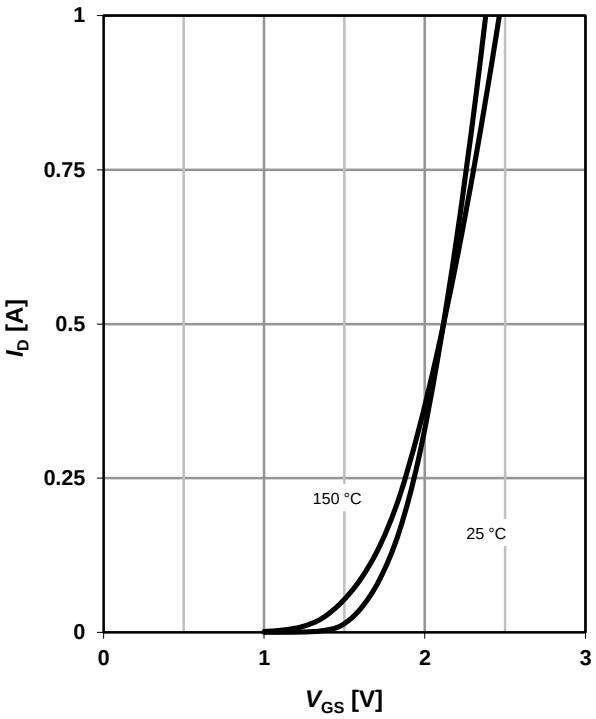
parameter: T_j



14 Typ. transfer characteristics (N)

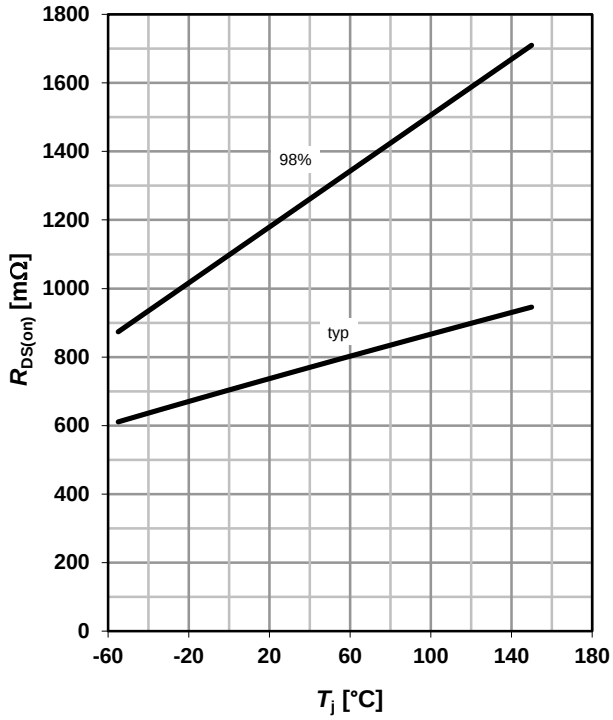
$I_D=f(V_{GS})$; $|V_{DS}|>2 | I_D | R_{DS(on)max}$

parameter: T_j



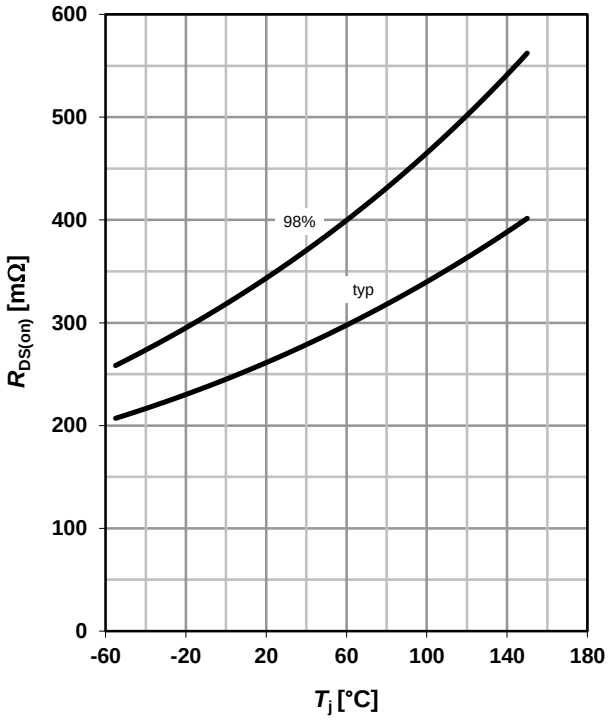
15 Drain-source on-state resistance (P)

$R_{DS(on)}=f(T_j)$; I_D=-0.53 A; V_{GS}=-4.5 V



16 Drain-source on-state resistance (N)

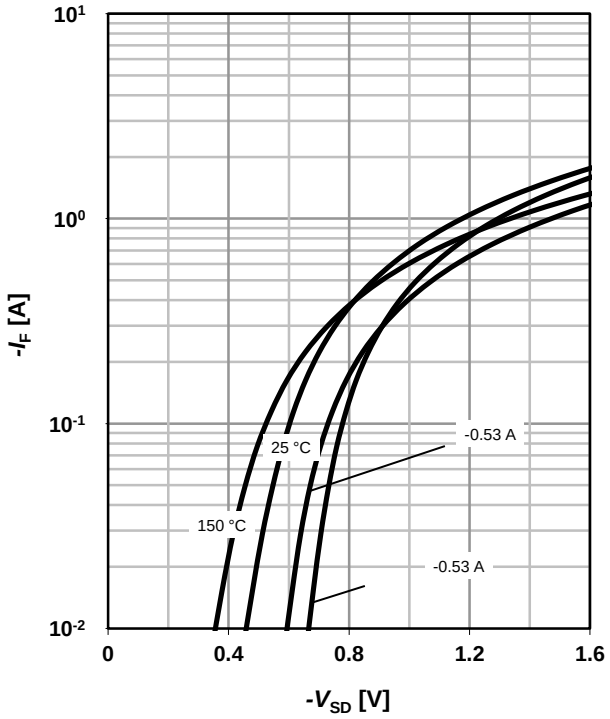
$R_{DS(on)}=f(T_j)$; I_D=0.95 A; V_{GS}=4.5 V



21 Forward characteristics of reverse diode (P)

$I_F=f(V_{SD})$

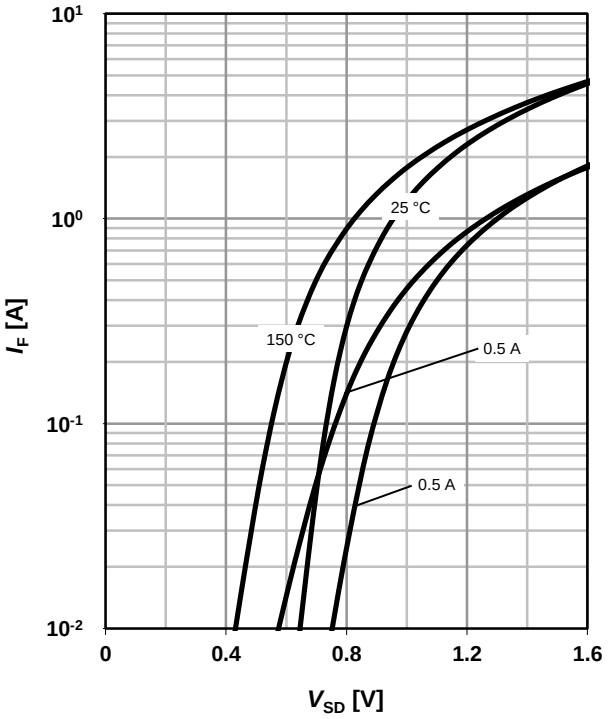
parameter: T_j



22 Forward characteristics of reverse diode (N)

$I_F=f(V_{SD})$

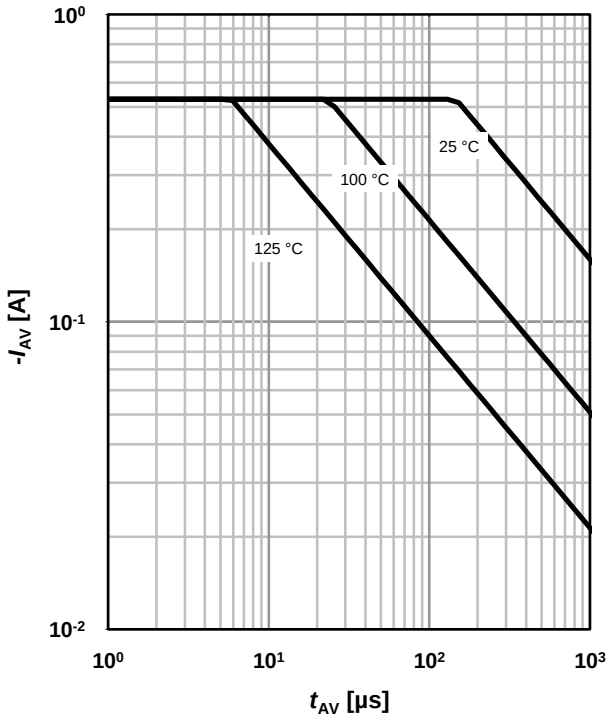
parameter: T_j



23 Avalanche characteristics (P)

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

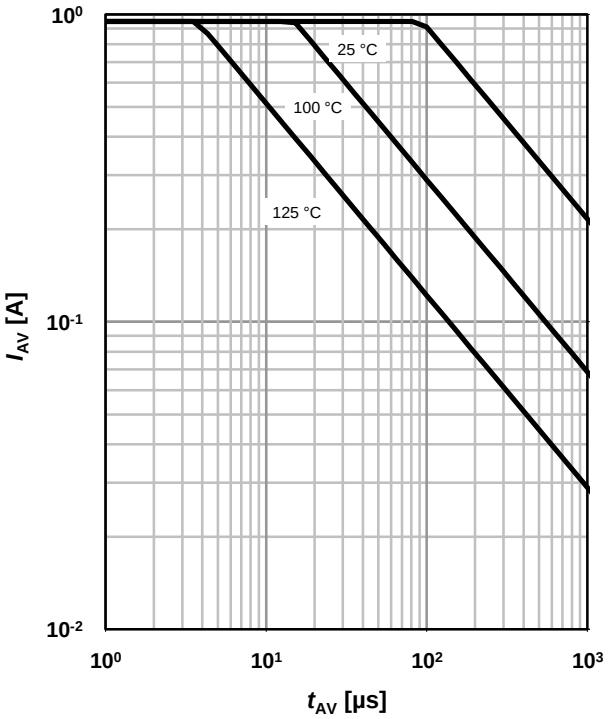
parameter: $T_{j(start)}$



24 Avalanche characteristics (N)

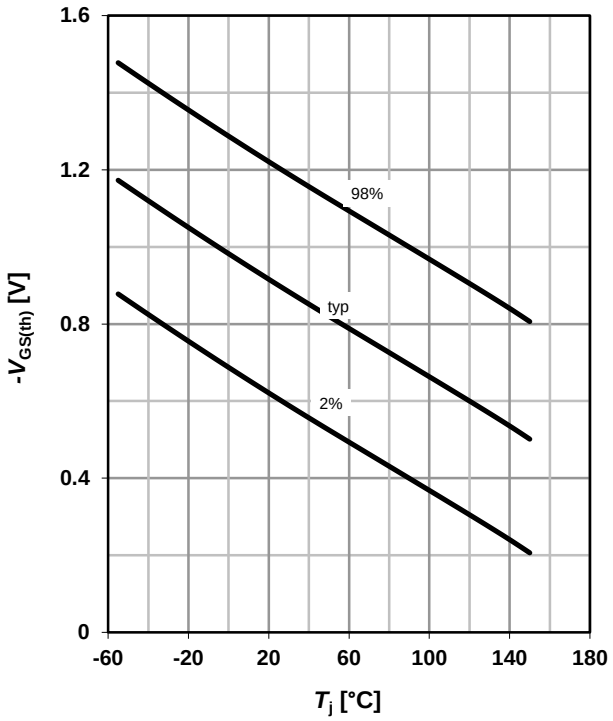
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

parameter: $T_{j(start)}$



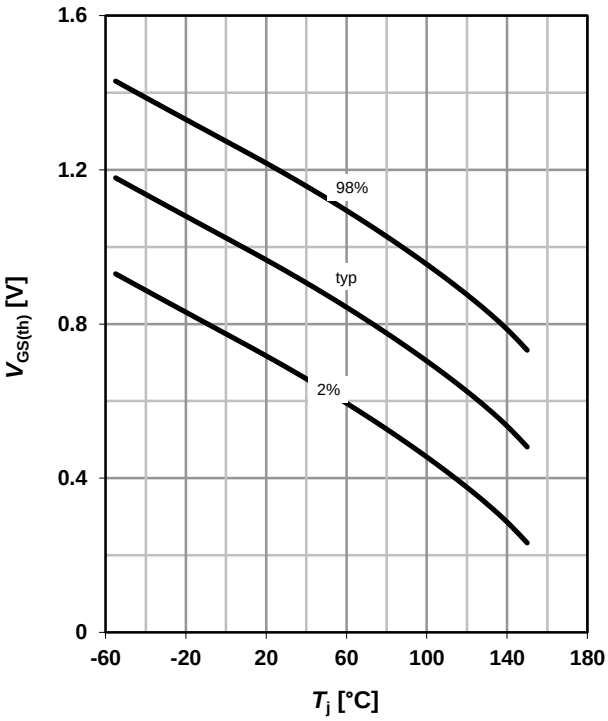
17 Typ. gate threshold voltage (P)

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; I_D=-1.5 µA



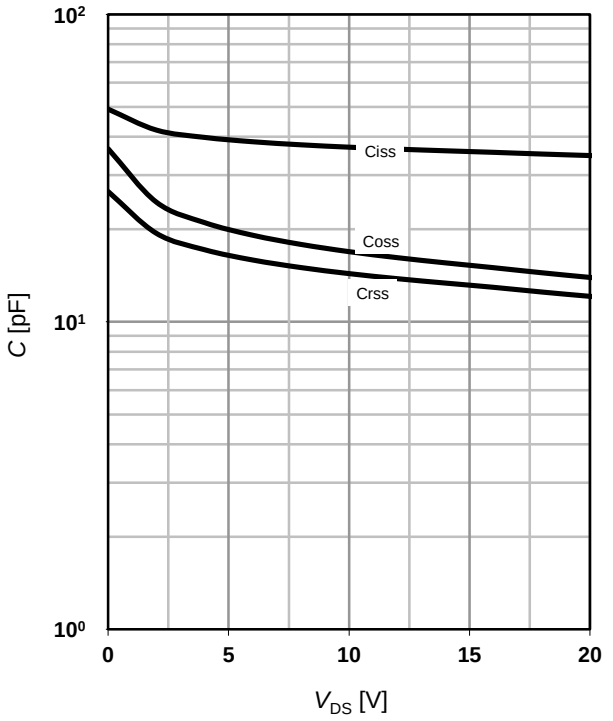
18 Typ. gate threshold voltage (N)

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; I_D=1.6 µA



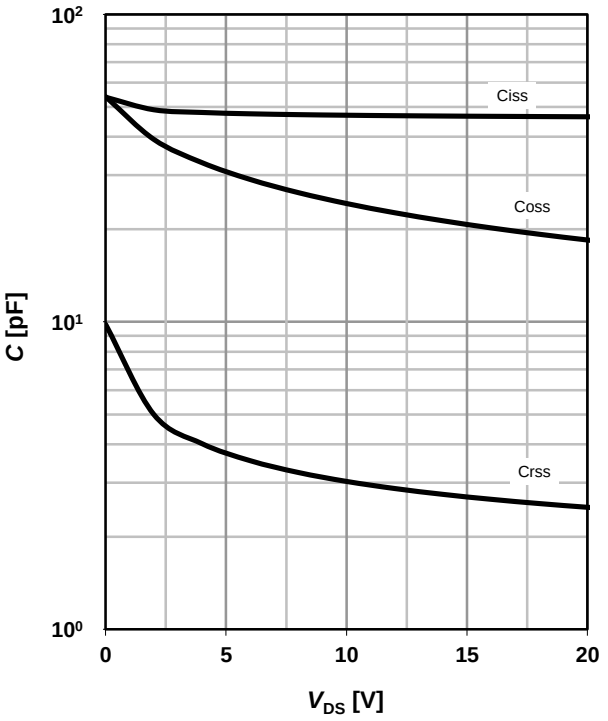
19 Typ. capacitances (P)

$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz



20 Typ. capacitances (N)

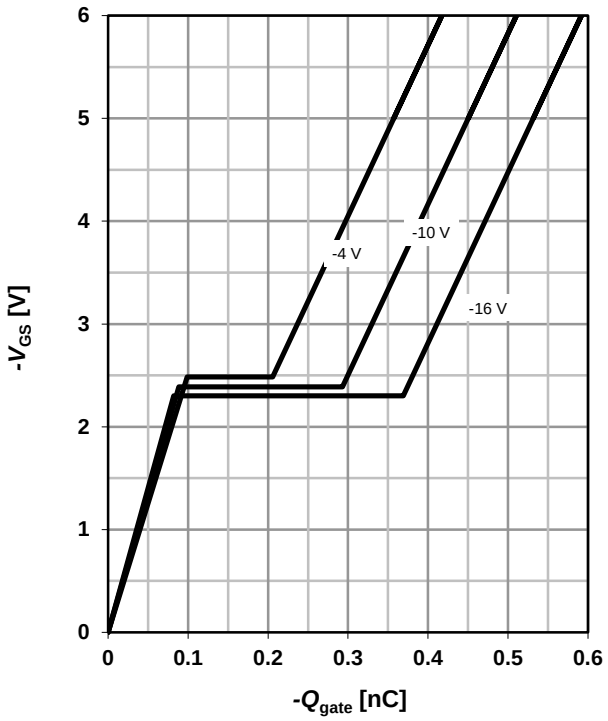
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz



25 Typ. gate charge (P)

V_{GS}=f(Q_{gate}); I_D=-0.53 A pulsed

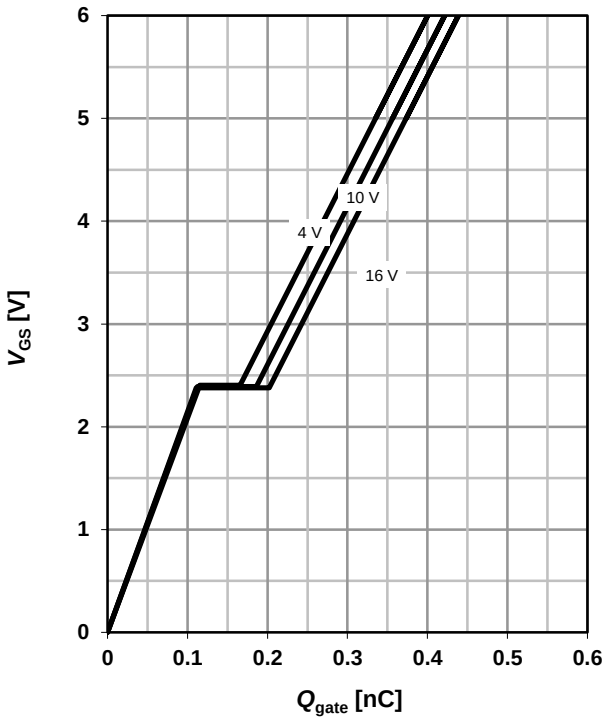
parameter: V_{DD}



26 Typ. gate charge (N)

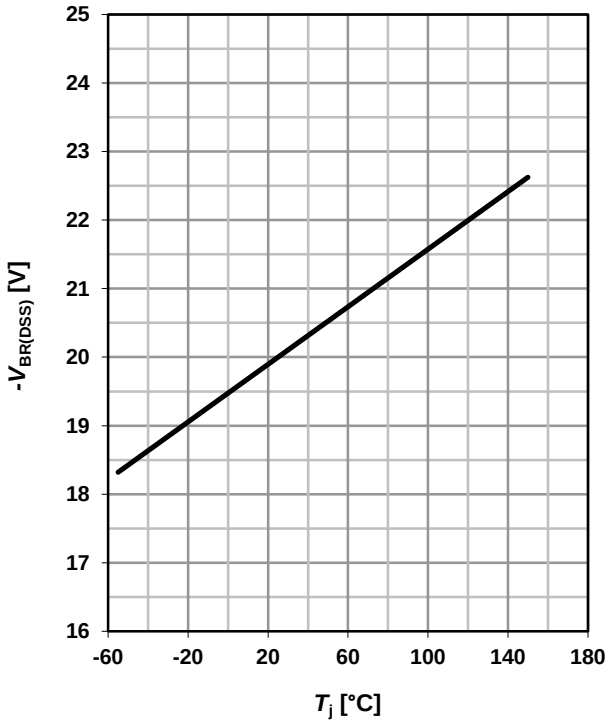
V_{GS}=f(Q_{gate}); I_D=0.95 A pulsed

parameter: V_{DD}



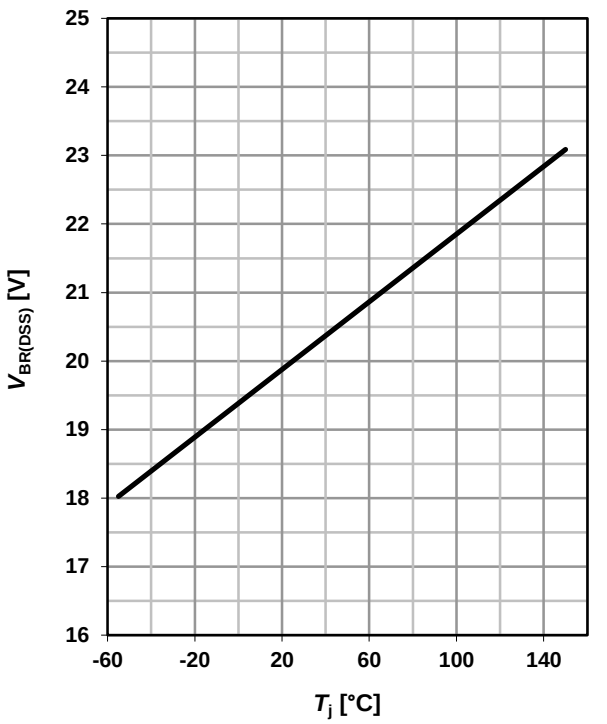
27 Drain-source breakdown voltage (P)

$V_{BR(DSS)}$=f(T_j); I_D=-250 µA



28 Drain-source breakdown voltage (N)

$V_{BR(DSS)}$=f(T_j); I_D=250 µA



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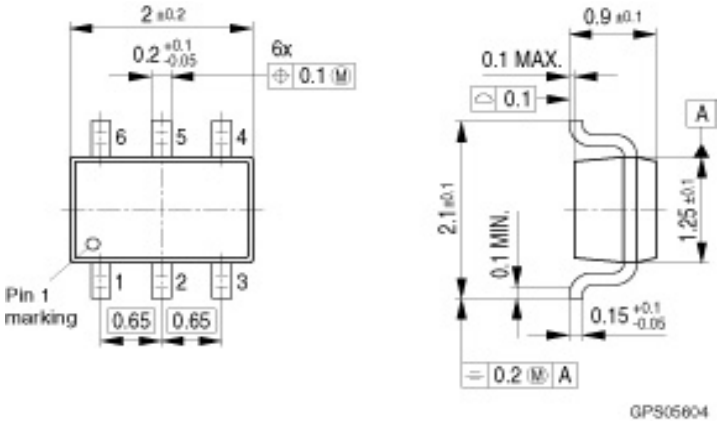
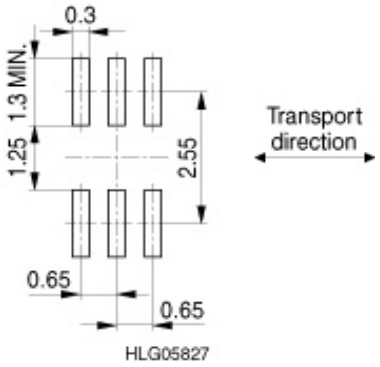
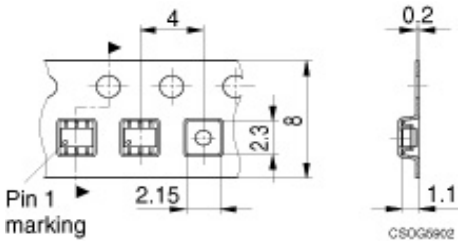
Package Outline:



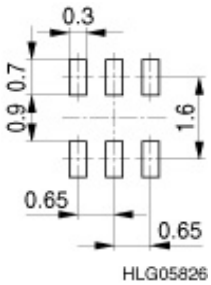
Footprint:



Packing:



Reflow soldering:



Dimensions in mm

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