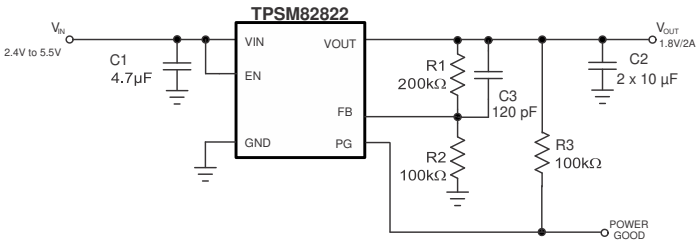
TPSM8282x 1-A and 2-A High Efficiency Step-Down Converter MicroSiP™ Power Module with Integrated Inductor

1 Features

- Low profile MicroSiP™ power module
- Up to 95% efficiency
- 2.4-V to 5.5-V input voltage range
- 0.6-V to 4-V adjustable output voltage
- 4-µA operating quiescent current
- DCS-control topology
- Power save mode for light load efficiency
- 100% duty cycle for lowest dropout
- Hiccup short circuit protection
- Output discharge
- Power good output
- Integrated soft start-up
- Overtemperature protection
- 2.0-mm × 2.5-mm × 1.1-mm 10-Pin µSiL package
- 29 mm^2 total solution size

2 Applications

- Optical modules
- Machine vision
- Embedded camera system
- Patient monitoring and diagnostics



1.8-V Output Application

3 Description

The TPSM8282x device family consists of a 1-A and 2-A step-down converter MicroSiP™ power module optimized for small solution size and high efficiency.

The power modules integrate a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

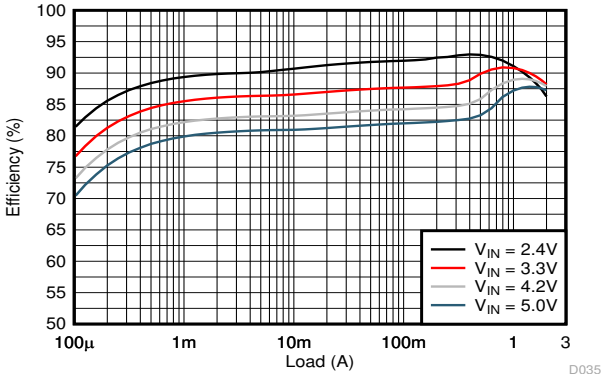
To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 4MHz and automatically enters Power Save Mode operation at light load currents.

In Power Save Mode, the device operates with typically 4-µA quiescent current. Using the DCS-Control topology, the device achieves excellent load transient performance and accurate output voltage regulation. The EN and PG pins, which support sequencing configurations, bring a flexible system design. An integrated soft startup reduces the inrush current required from the input supply. Over temperature protection and hiccup short circuit protection deliver a robust and reliable solution.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPSM82821SIL	µSiL (10)	2.0 mm x 2.5 mm
TPSM82822SIL	µSiL (10)	2.0 mm x 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



1.8-V Output Efficiency

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (December 2019) to Revision B (November 2020) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document. 1
- Changed storage temperature range minimum value from -40°C to -55°C in *Section 6.4* 4
- Updated *Section 8.4.3* 9
- Updated *Section 9.2.1.2.1* 11
- Added sentence to *Section 11.3* 25

Changes from Revision * (August 2019) to Revision A (December 2019) **Page**

- Changed device status from Advance Information to Production Data....1
- Added planned device spins to *Device Comparison Table* 0

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Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	OUTPUT VOLTAGE
TPSM82821SIL	1 A	adjustable
TPSM82822SIL	2 A	adjustable

5 Pin Configuration and Functions

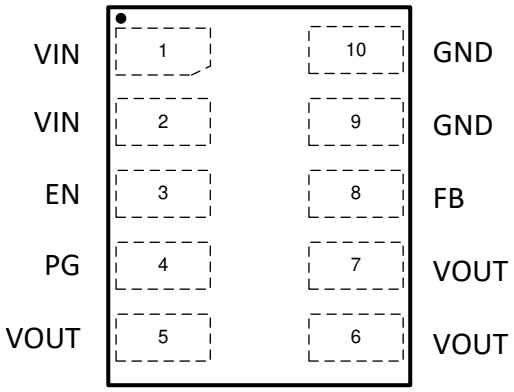

Figure 5-1. µSiL Package (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
FB	8	I	Feedback pin. This pin must be connected to the center of the output voltage resistor divider.
GND	9, 10	PWR	Ground pin
PG	4	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
VIN	1, 2	PWR	Input voltage pin
VOUT	5, 6, 7	PWR	Output voltage pin

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN, VOUT, FB, EN, PG (2)	–0.3	6	V
I_{SINK_PG}	Sink current at PG pin		1	mA
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.4	5.5	V
V_{OUT}	Output voltage range	0.6	4	V
V_{PG}	Pull-up resistor voltage		5.5	V
I_{OUT}	Output current range, TPSM82821 (1)	0	1	A
	Output current range, TPSM82822 (1)	0	2	
T_J	Junction temperature (1)	-40	125	°C

(1) In applications where high power dissipation and high ambient temperatures are present, the maximum output current must be derated to operate the module within its operating temperature range. See Section 11.3 - Thermal Consideration.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8282x		UNIT
		µSiL (JEDEC 51-7)	TPSM82822EVM-080	
		10-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	63.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.3	n/a (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.9	n/a (2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.8	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.5	27.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Not applicable to an EVM.

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6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 2.4V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	EN = High, No load, device not switching		4	10	µA
I_{SD}	Shutdown current into VIN	EN = Low, T_J = -40°C to 85°C		0.05	0.5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage		1.0			V
V_{IL}	Low-level input voltage				0.4	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High		0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		1.25		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94	96	98	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	90	92	94	%
	Power good upper threshold	V_{PG} falling, V_{FB} referenced to V_{FB} nominal	103	105	107	%
		V_{PG} rising, V_{FB} referenced to V_{FB} nominal	108	110	112	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1mA			0.4	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 5V		0.01	0.1	µA
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode	594	600	606	mV
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.6 V		0.01	0.05	µA
I_{DIS}	Output discharge current	EN = Low, V_{SW} = 0.4V	75	400		mA
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			26		mΩ
R_{DP}	Dropout resistance	TPSM82821, 100% mode. V_{IN} = 2.7V, T_J = 25°C		115	145	mΩ
R_{DP}	Dropout resistance	TPSM82822, 100% mode. V_{IN} = 2.7V, T_J = 25°C		90	120	mΩ
I_{LIMF}	High-side FET switch current limit	TPSM82821	1.75	2.2	2.75	A
I_{LIMF}	High-side FET switch current limit	TPSM82822	2.7	3.3	3.9	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		4		MHz

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7 Typical Characteristics

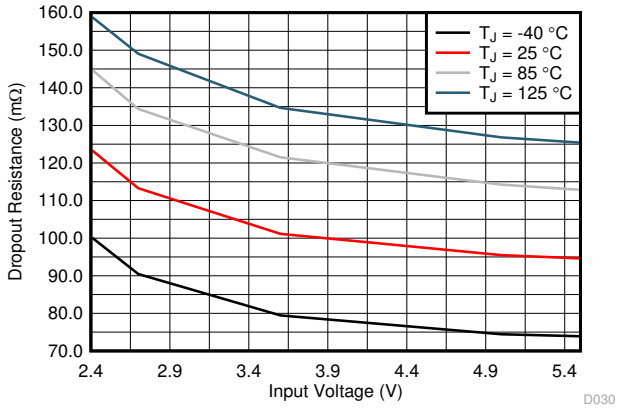

Figure 7-1. TPSM82821 Dropout Resistance

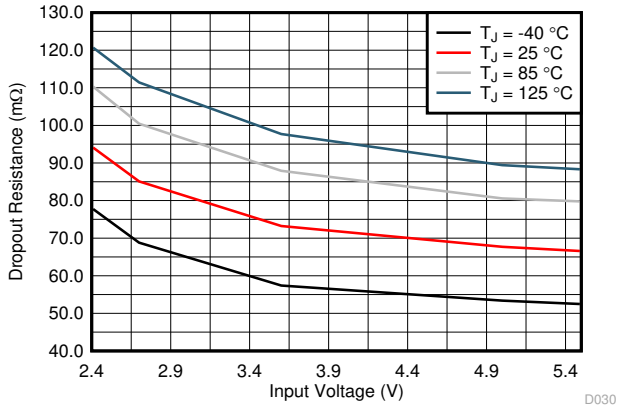

Figure 7-2. TPSM82822 Dropout Resistance

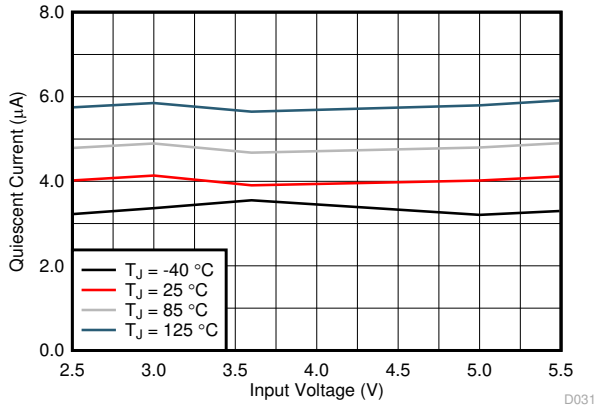

Figure 7-3. Quiescent Current

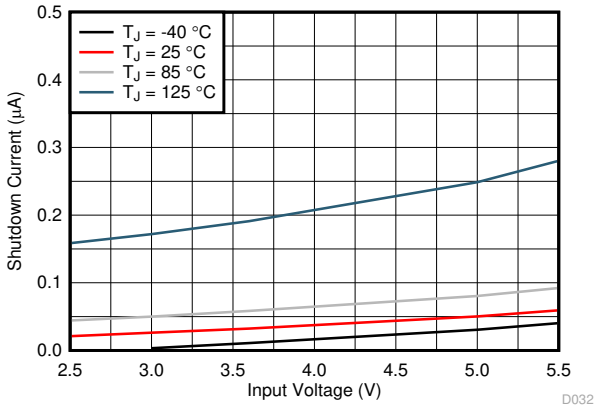

Figure 7-4. Shutdown Current

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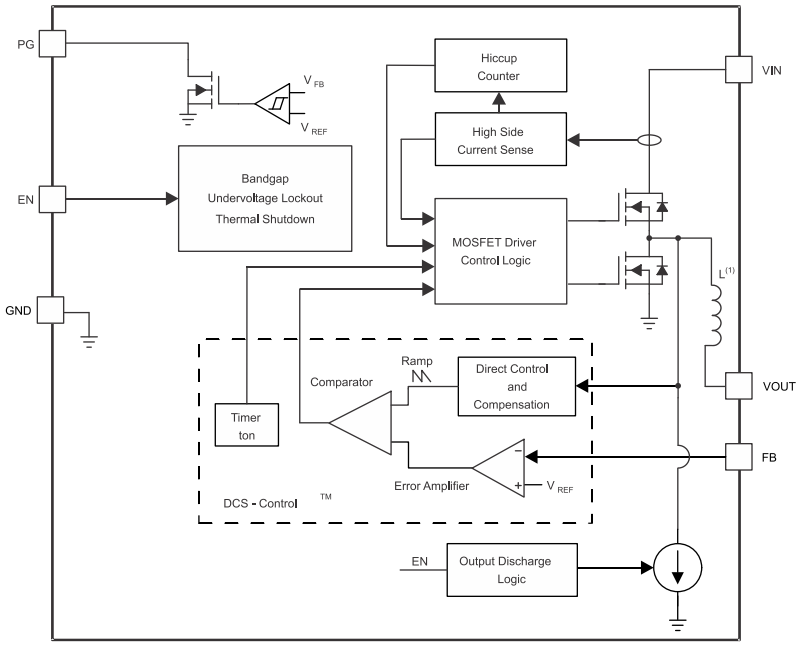
8 Detailed Description

8.1 Overview

The TPSM8282x synchronous step-down converter power module is based on DCS-Control™ (Direct Control with Seamless transition into Power-Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power-Save Mode) at light load currents. In PWM, the converter operates with its nominal switching frequency of 4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power-Save Mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and, therefore, has a seamless transition from PWM to PSM without effects on the output voltage. The TPSM8282x offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



Inductance value is 0.47 µH in TPSM82821 and 0.24 µH in TPSM82822.

8.3 Feature Description

8.3.1 PWM and PSM Operation

The TPSM8282x includes a fixed on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 250ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

In PWM mode, the TPSM8282x operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in Equation 1 at medium and heavy load currents. A PWM switching frequency of typically 4 MHz is achieved by this t_{ON} circuitry.

To maintain high efficiency at light loads, the device enters Power-Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the ripple current of the inductor. In PSM, the converter operates with a reduced switching frequency and with a minimum quiescent current to

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maintain high efficiency. The on-time in PSM is also based on the same t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance.

8.3.2 Low Dropout Operation (100% Duty Cycle)

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN\ (min)} = V_{OUT\ (min)} + I_{OUT} \times R_{DP} \quad (3)$$

where

- R_{DP} = Resistance from V_{IN} to V_{OUT}, which includes the high-side FET on-resistance and DC resistance of the inductor
- $V_{OUT\ (min)}$ = Minimum output voltage the load can accept

8.3.3 Soft Start-up

After enabling the device, there is a 250-µs delay before switching starts. Then, an internal soft start-up circuitry ramps up the output voltage which reaches nominal output voltage during the start-up time of 1 ms. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Hiccup Short Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold of I_{LIMF}, the high-side MOSFET is turned off and the low-side MOSFET remains off while the inductor current flows through its body diode and quickly ramps down.

When this switch current limit is triggered 32 times, the device stops switching. The device then automatically starts a new start-up after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

8.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, undervoltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO}.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops the power stage switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically by switching the power stage again.

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8.4 Device Functional Modes

8.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 50 nA. In shutdown mode, the internal power switches and the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOUT pin in shutdown mode. Do not leave the EN pin floating.

The typical threshold value of the EN pin is 0.89 V for rising input signal, and 0.62 V for falling input signal.

8.4.2 Output Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge is active when the EN pin is set to a logic low and during thermal shutdown. The discharge is not active in UVLO.

8.4.3 Power Good Output

The device has a power good output. The PG pin goes high impedance once the FB pin voltage is above 96% and less than 105% of the nominal voltage, and is driven low once the voltage falls below typically 92% or higher than 110% of the nominal voltage. Table 8-1 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND.

Table 8-1. Power Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN = High)	0.576 V ≤ V_{FB} ≤ 0.63 V	√	
	V_{FB} < 0.552 V or V_{FB} > 0.66 V		√
Shutdown (EN = Low)			√
UVLO	0.7 V ≤ V_{IN} < V_{UVLO}		√
Thermal Shutdown	T_J > T_{JSD}		√
Power Supply Removal	V_{IN} < 0.7 V	√	

The PG pin has a 20-µs deglitch time on the falling edge and a 100-µs delay before PG goes high. See Figure 8-1.

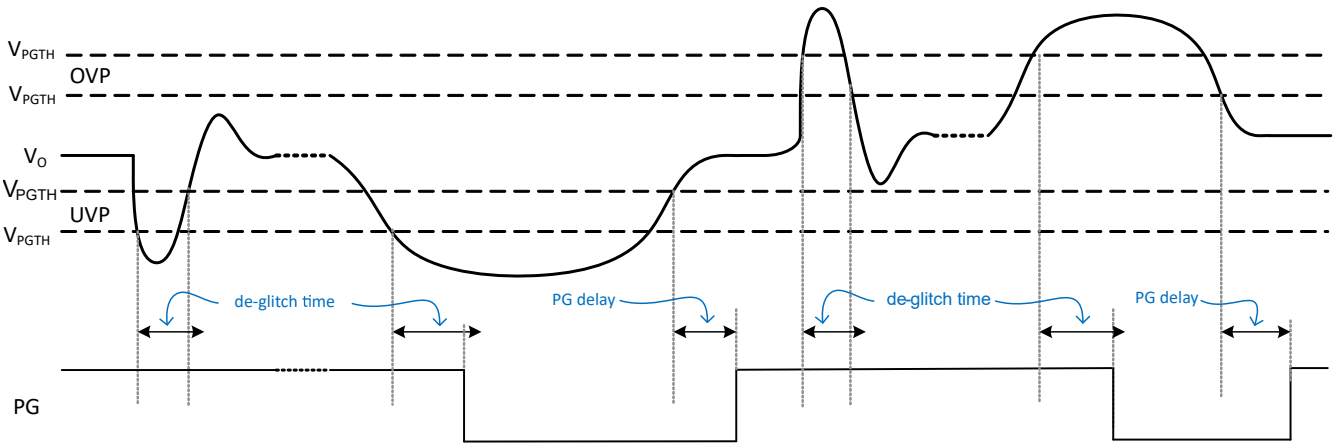

Figure 8-1. Power Good Transient and De-glitch Behavior

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPSM8282x is a synchronous step-down converter power module whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design. The required power inductor is integrated inside the TPSM8282x. The inductor value is 0.47 µH for the TPSM82821 and 0.24 µH for the TPSM82822, with a ±20% tolerance. The TPSM82821 and TPSM82822 are pin-to-pin and BOM-to-BOM compatible.

9.2 Typical Applications

9.2.1 1.8-V Output Application

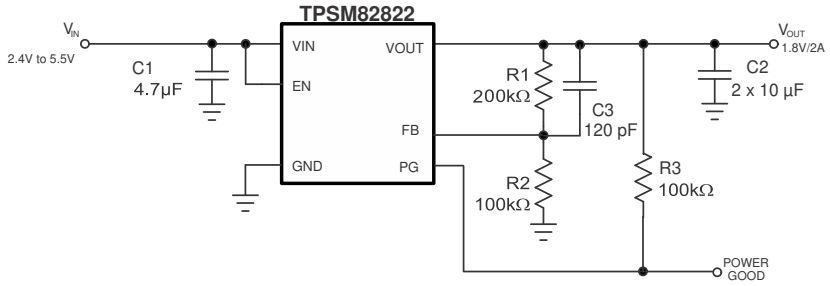

Figure 9-1. 1.8-V Output Application

9.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.4 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 20 mV
Output current rating	2 A

Table 9-2 lists the components used for the example.

Table 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	Ceramic capacitor, 4.7 µF, 6.3 V, X7R, size (0603), JMK107BB7475MA	Taiyo Yuden
C2	Ceramic capacitor, 10 µF, 10 V, X7R, size (0603), GRM188Z71A106MA73D	muRata
C3	Ceramic capacitor, 120 pF, 50 V, size (0603), GRM1885C1H121JA01D	muRata
R1	Resistor, 200 kΩ, 1% accuracy	std
R2	Resistor, 100 kΩ, 1% accuracy	std
R3	Resistor, 100 kΩ, 1% accuracy	std

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9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Setting the Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.6 V to 4 V according to Equation 4. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (4)$$

9.2.1.2.2 Feedforward capacitor

A feedforward capacitor (C3) is required in parallel with R1. Equation 5 calculates the C3 value. For the recommended 100-kΩ value for R2, a 120-pF feedforward capacitor is used.

$$C3 = \frac{12\mu s}{R2} \quad (5)$$

9.2.1.2.3 Input and Output Capacitor Selection

For the best output and input voltage filtering, ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. A 4.7-µF or larger input capacitor is required. The output capacitor value can range from 10 µF up to 47 µF. The recommended typical output capacitor value is 2 × 10-µF or 1 × 22-µF with an X5R or X7R dielectric. Values over 47 µF can degrade the loop stability of the converter. A feedforward capacitor is required for best transient performance.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the effective input capacitance is at least 3 µF and the effective output capacitance is at least 5 µF.

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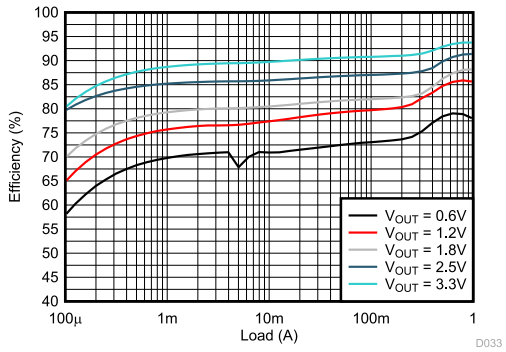
9.2.1.3 Application Performance Curves

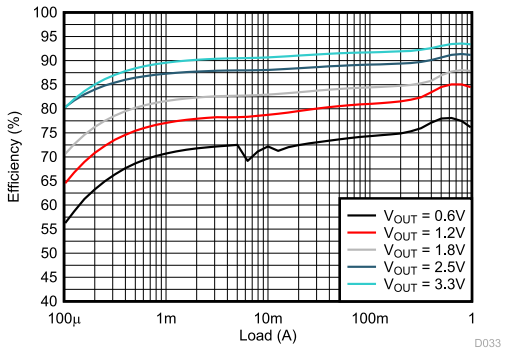
T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, BOM = Table 9-2 unless otherwise noted.

9.2.1.3.1 TPSM82821 Performance Curves



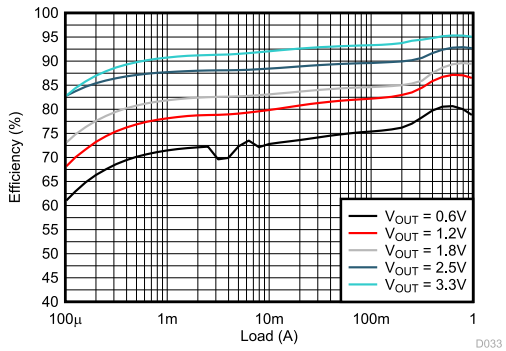
V_{IN} = 5 V T_A = 25°C TPSM82821

Figure 9-2. Efficiency



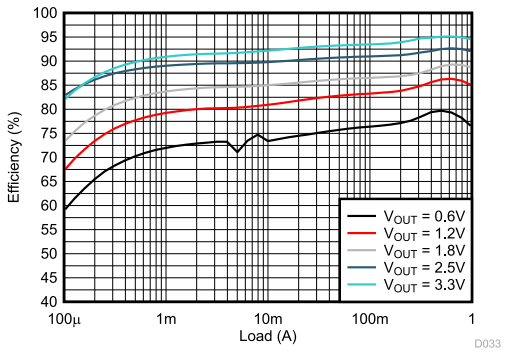
V_{IN} = 5 V T_A = 85°C TPSM82821

Figure 9-3. Efficiency



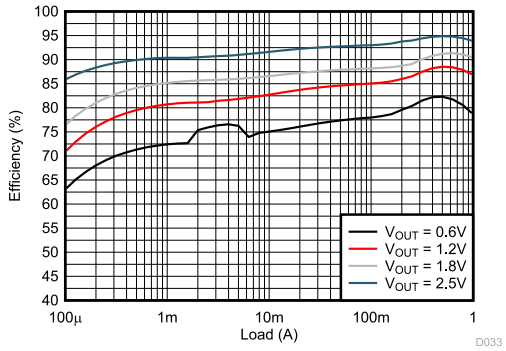
V_{IN} = 4.2 V T_A = 25°C TPSM82821

Figure 9-4. Efficiency



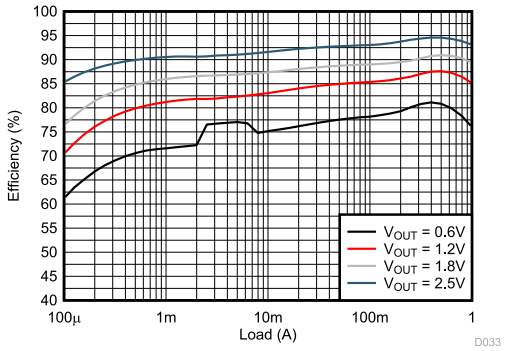
V_{IN} = 4.2 V T_A = 85°C TPSM82821

Figure 9-5. Efficiency



V_{IN} = 3.3 V T_A = 25°C TPSM82821

Figure 9-6. Efficiency



V_{IN} = 3.3 V T_A = 85°C TPSM82821

Figure 9-7. Efficiency

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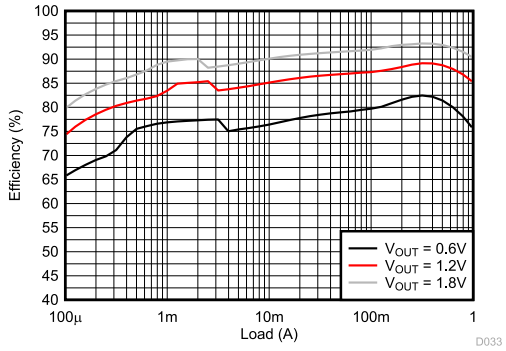
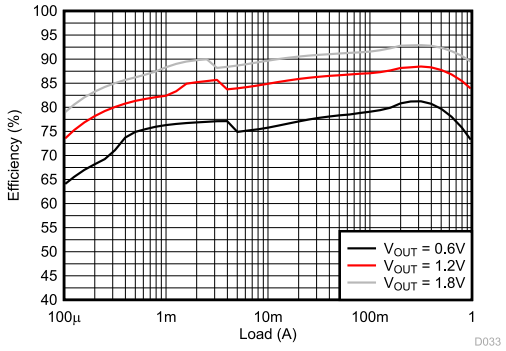


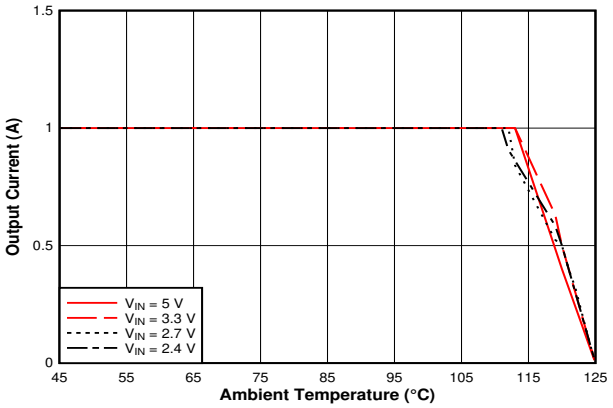
V_{IN} = 2.4 V T_A = 25°C TPSM82821

Figure 9-8. Efficiency



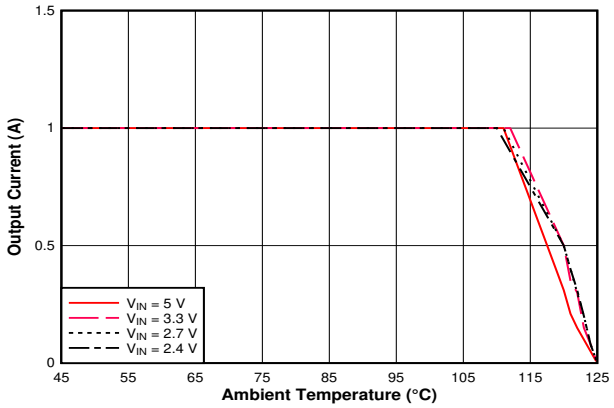
V_{IN} = 2.4 V T_A = 85°C TPSM82821

Figure 9-9. Efficiency



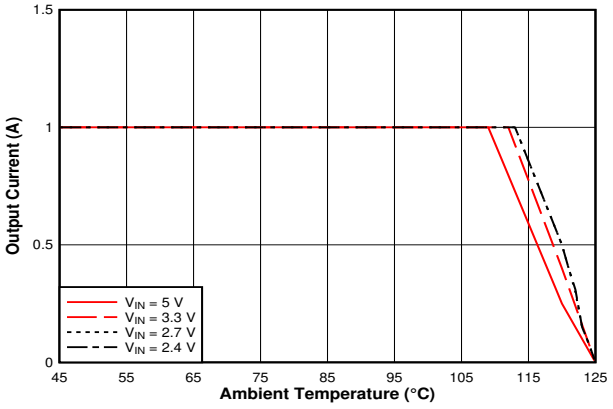
V_{OUT} = 0.6 V TPSM82821 $R_{\theta JA}$ = 63.9°C/W

Figure 9-10. Safe Operating Area



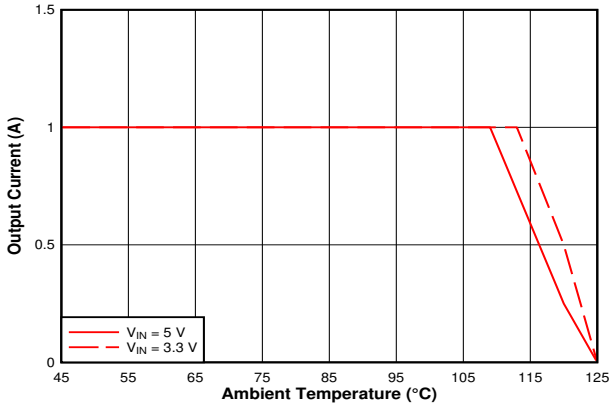
V_{OUT} = 1.2 V TPSM82821 $R_{\theta JA}$ = 63.9°C/W

Figure 9-11. Safe Operating Area



V_{OUT} = 1.8 V TPSM82821 $R_{\theta JA}$ = 63.9°C/W

Figure 9-12. Safe Operating Area



V_{OUT} = 2.5 V TPSM82821 $R_{\theta JA}$ = 63.9°C/W

Figure 9-13. Safe Operating Area

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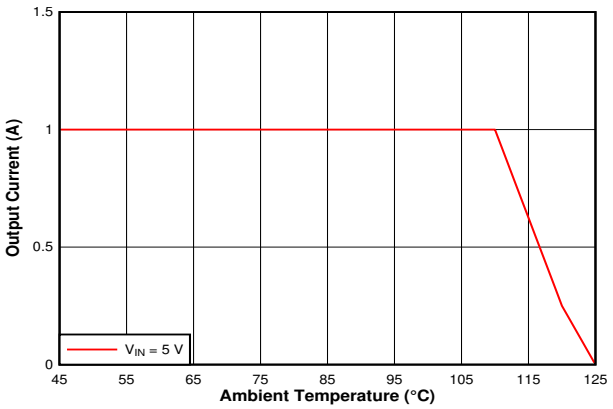
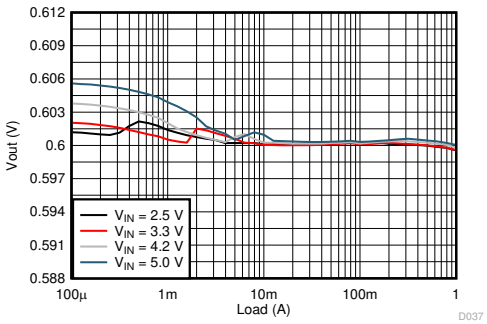


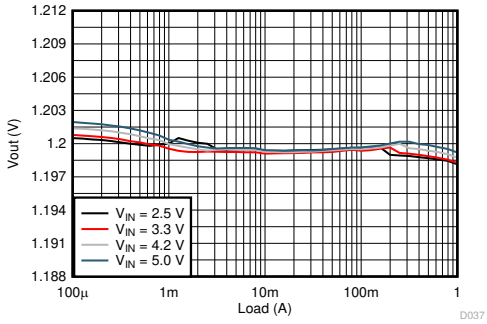
V_{OUT} = 3.3 V TPSM82821 $R_{\theta JA}$ = 63.9°C/W

Figure 9-14. Safe Operating Area



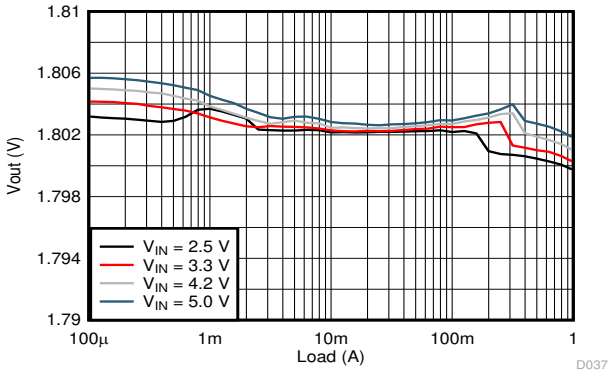
V_{OUT} = 0.6 V TPSM82821

Figure 9-15. Load Regulation



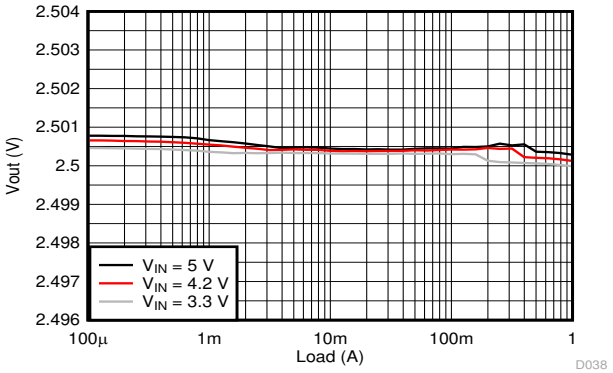
V_{OUT} = 1.2 V TPSM82821

Figure 9-16. Load Regulation



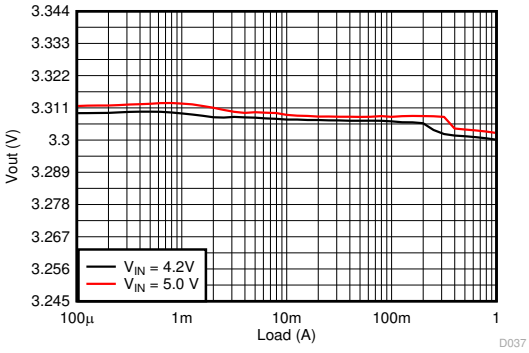
V_{OUT} = 1.8 V TPSM82821

Figure 9-17. Load Regulation



V_{OUT} = 2.5 V TPSM82821

Figure 9-18. Load Regulation



V_{OUT} = 3.3 V TPSM82821

Figure 9-19. Load Regulation

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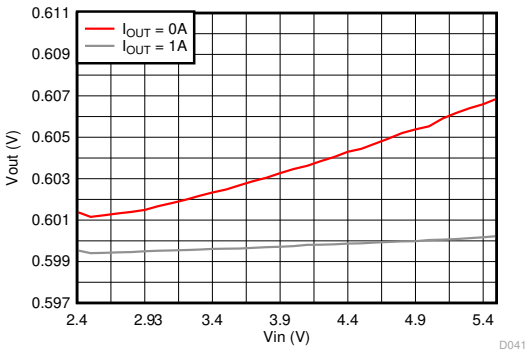
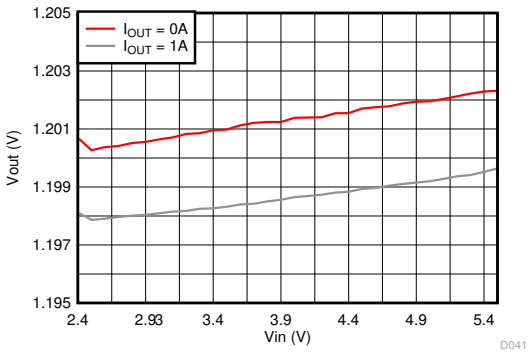


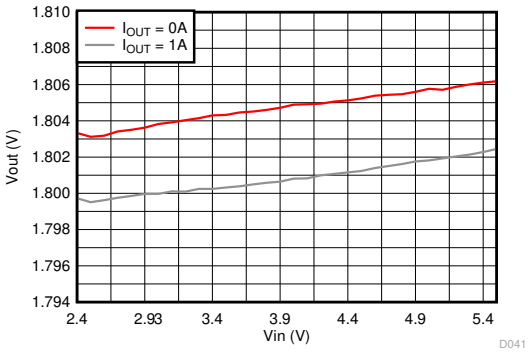
V_{OUT} = 0.6 V TPSM82821

Figure 9-20. Line Regulation



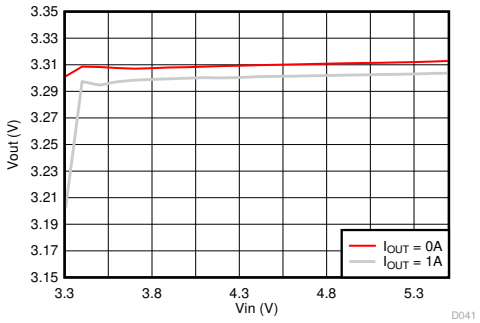
V_{OUT} = 1.2 V TPSM82821

Figure 9-21. Line Regulation



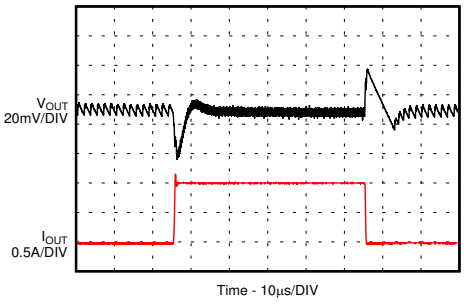
V_{OUT} = 1.8 V TPSM82821

Figure 9-22. Line Regulation



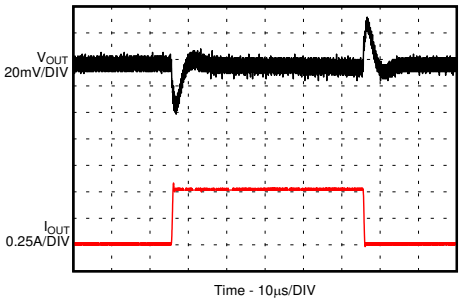
V_{OUT} = 3.3 V TPSM82821

Figure 9-23. Line Regulation



I_{OUT} = 0 A to 1 A Slew Rate = 2 A/µs TPSM82821

Figure 9-24. Load Transient



I_{OUT} = 0.5 A to 1 A Slew Rate = 2 A/µs TPSM82821

Figure 9-25. Load Transient

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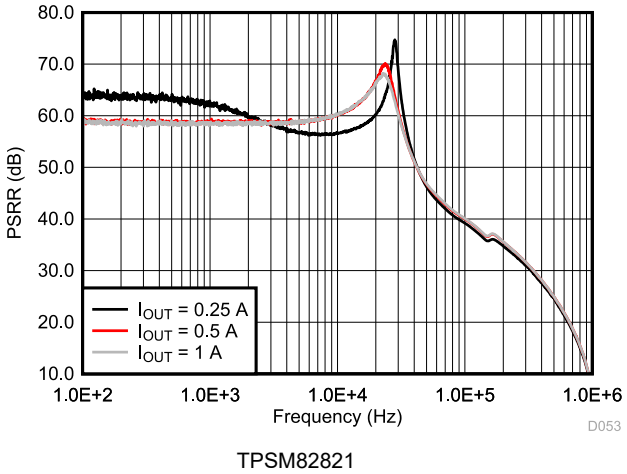

TPSM82821

Figure 9-26. Power Supply Rejection Ratio (PSRR)

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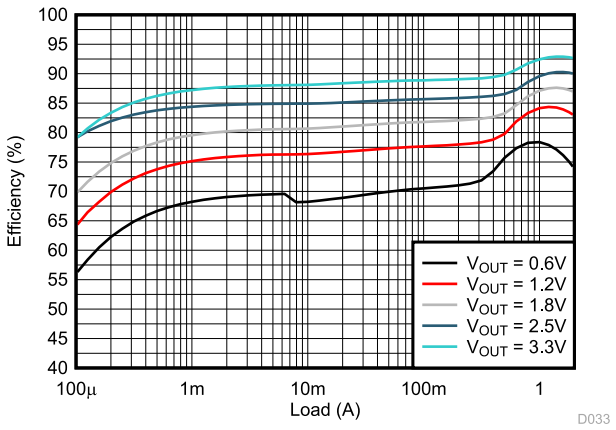
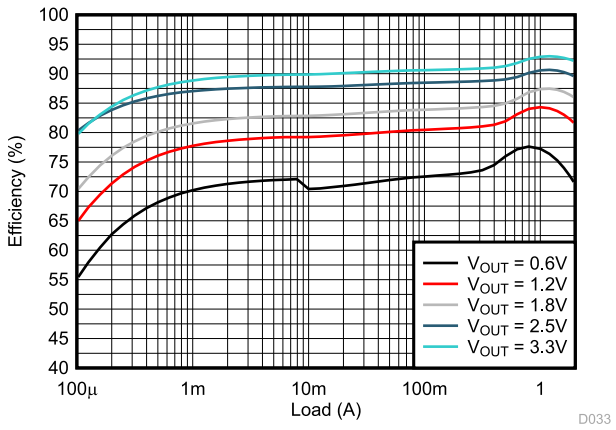
9.2.1.3.2 TPSM82822 Performance Curves



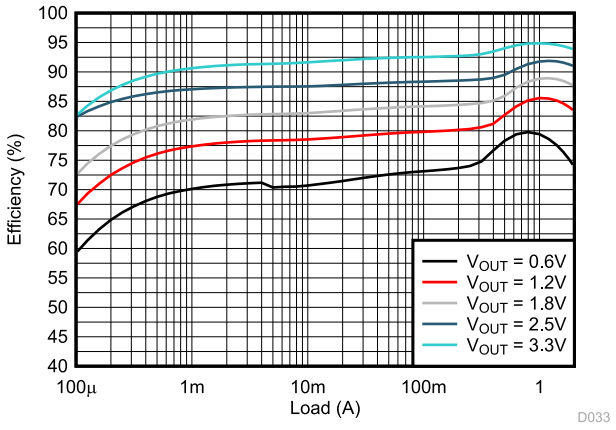
V_{IN} = 5 V T_A = 25°C TPSM82822

Figure 9-27. Efficiency



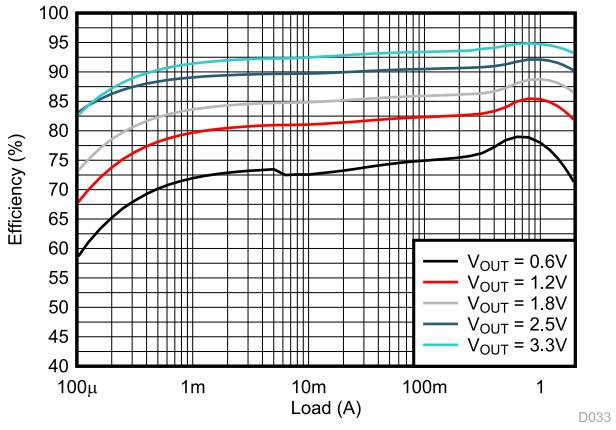
V_{IN} = 5 V T_A = 85°C TPSM82822

Figure 9-28. Efficiency



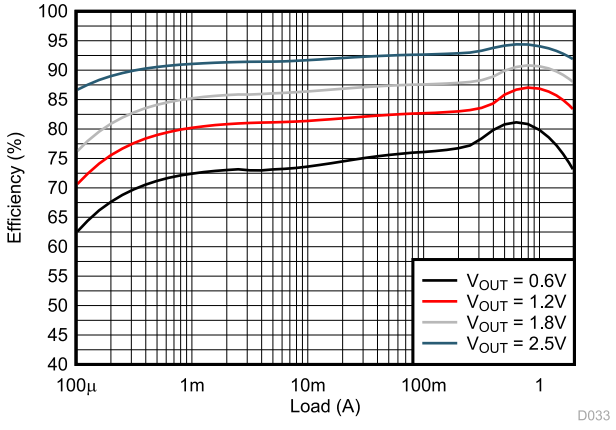
V_{IN} = 4.2 V T_A = 25°C TPSM82822

Figure 9-29. Efficiency



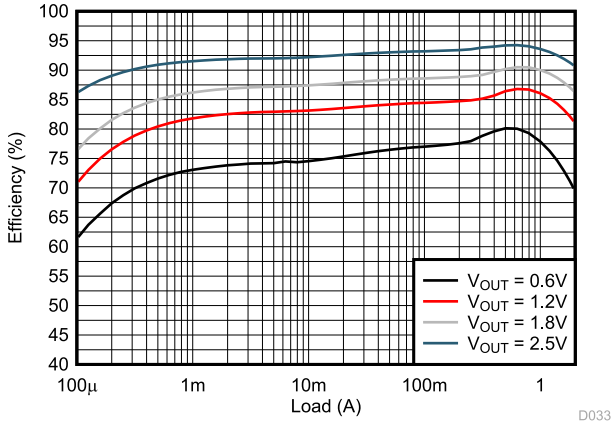
V_{IN} = 4.2 V T_A = 85°C TPSM82822

Figure 9-30. Efficiency



V_{IN} = 3.3 V T_A = 25°C TPSM82822

Figure 9-31. Efficiency



V_{IN} = 3.3 V T_A = 85°C TPSM82822

Figure 9-32. Efficiency

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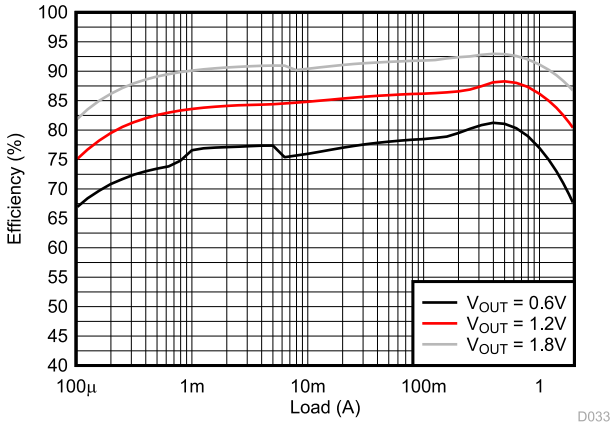
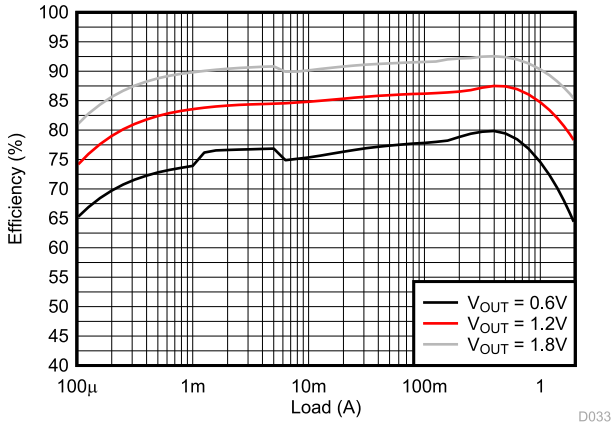


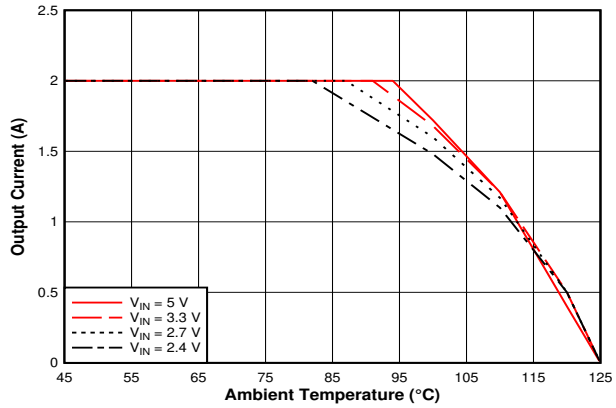
V_{IN} = 2.4 V T_A = 25°C TPSM82822

Figure 9-33. Efficiency



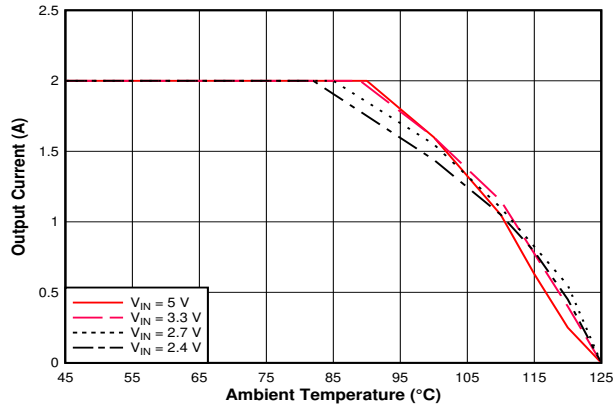
V_{IN} = 2.4 V T_A = 85°C TPSM82822

Figure 9-34. Efficiency



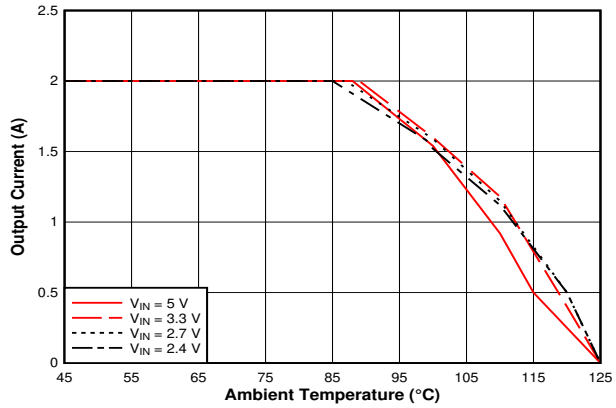
V_{OUT} = 0.6 V TPSM82822 $R_{\theta JA}$ = 63.9°C/W

Figure 9-35. Safe Operating Area



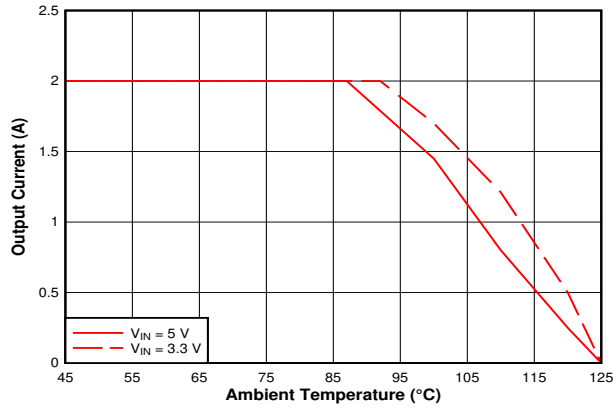
V_{OUT} = 1.2 V TPSM82822 $R_{\theta JA}$ = 63.9°C/W

Figure 9-36. Safe Operating Area



V_{OUT} = 1.8 V TPSM82822 $R_{\theta JA}$ = 63.9°C/W

Figure 9-37. Safe Operating Area



V_{OUT} = 2.5 V TPSM82822 $R_{\theta JA}$ = 63.9°C/W

Figure 9-38. Safe Operating Area

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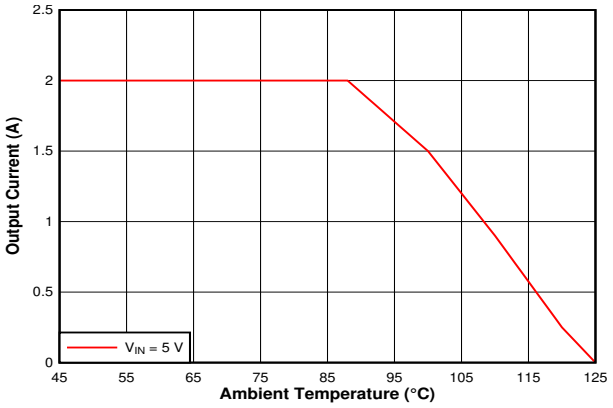
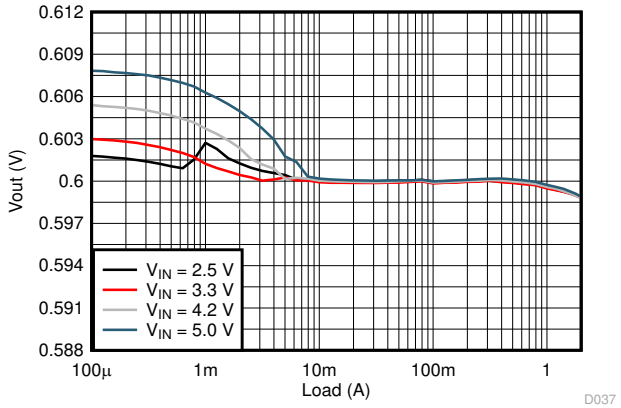


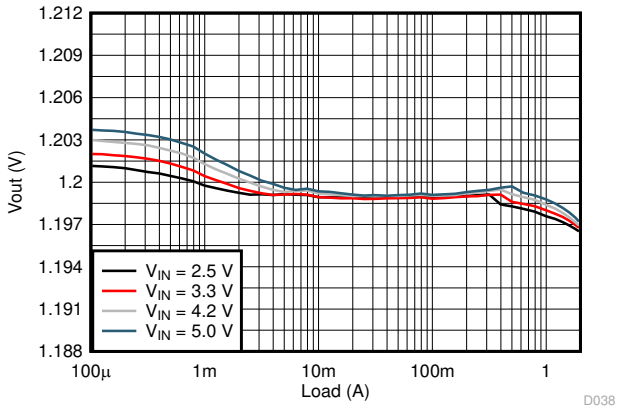
V_{OUT} = 3.3 V TPSM82822 $R_{\theta JA}$ = 63.9°C/W

Figure 9-39. Safe Operating Area



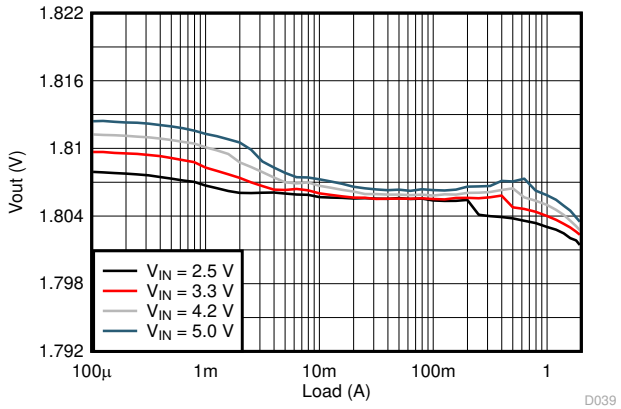
V_{OUT} = 0.6 V TPSM82822

Figure 9-40. Load Regulation



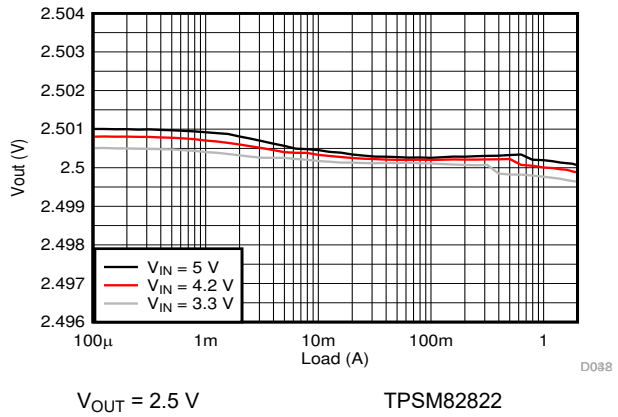
V_{OUT} = 1.2 V TPSM82822

Figure 9-41. Load Regulation



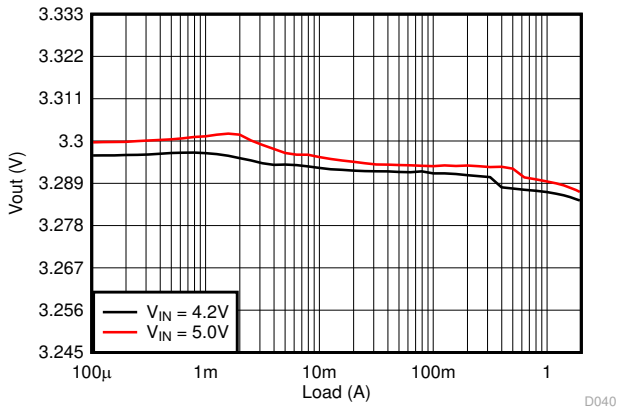
V_{OUT} = 1.8 V TPSM82822

Figure 9-42. Load Regulation



V_{OUT} = 2.5 V TPSM82822

Figure 9-43. Load Regulation



V_{OUT} = 3.3 V TPSM82822

Figure 9-44. Load Regulation

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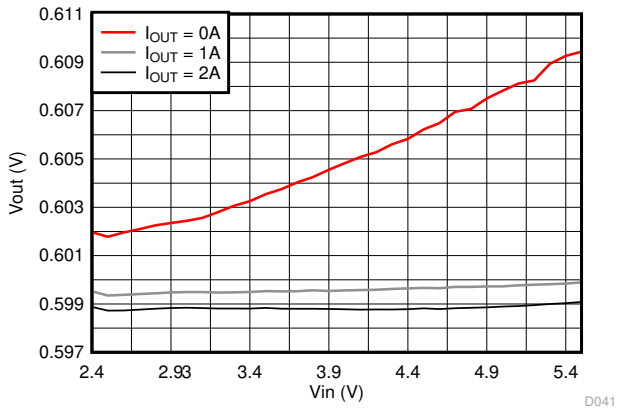
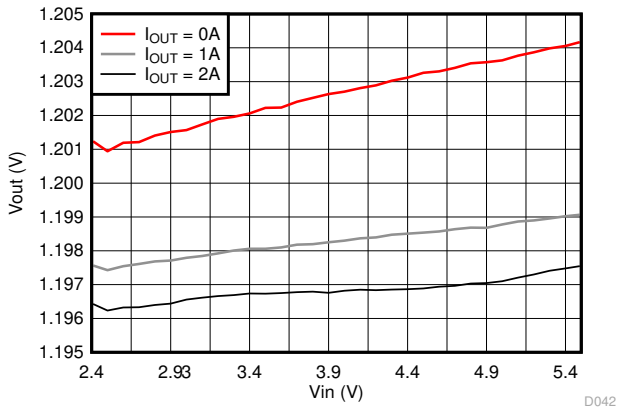


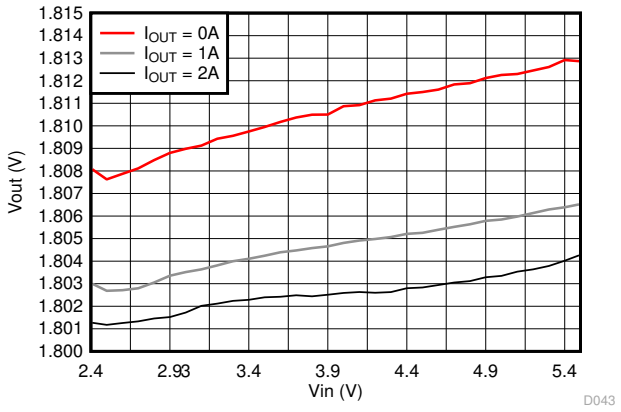
V_{OUT} = 0.6 V TPSM82822

Figure 9-45. Line Regulation



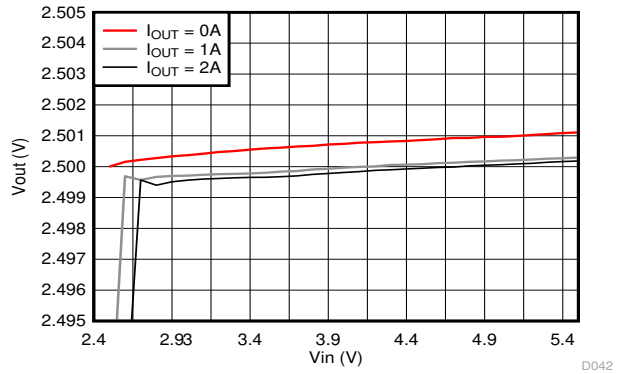
V_{OUT} = 1.2 V TPSM82822

Figure 9-46. Line Regulation



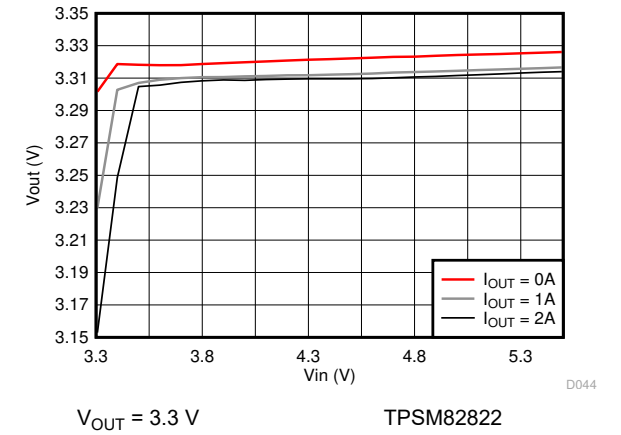
V_{OUT} = 1.8 V TPSM82822

Figure 9-47. Line Regulation



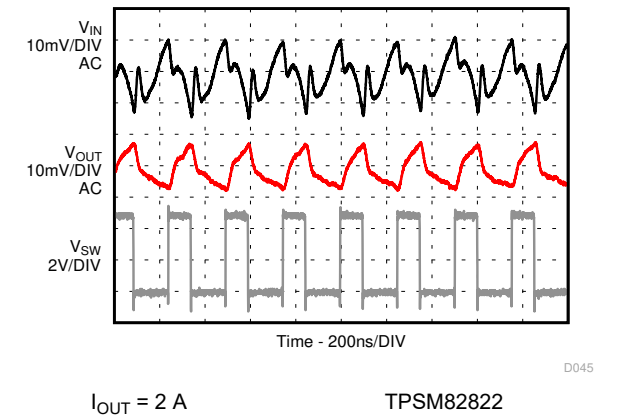
V_{OUT} = 2.5 V TPSM82822

Figure 9-48. Line Regulation



V_{OUT} = 3.3 V TPSM82822

Figure 9-49. Line Regulation



I_{OUT} = 2 A TPSM82822

Figure 9-50. Input and Output Ripple in PWM Mode

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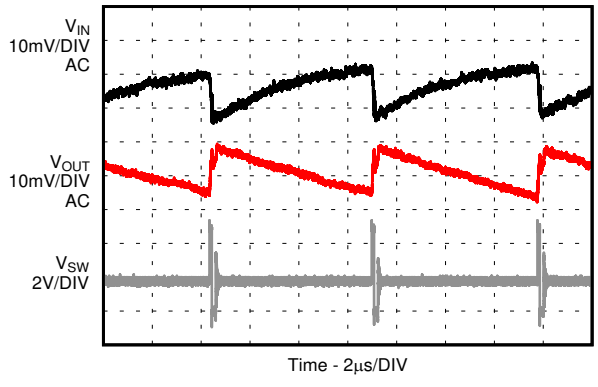
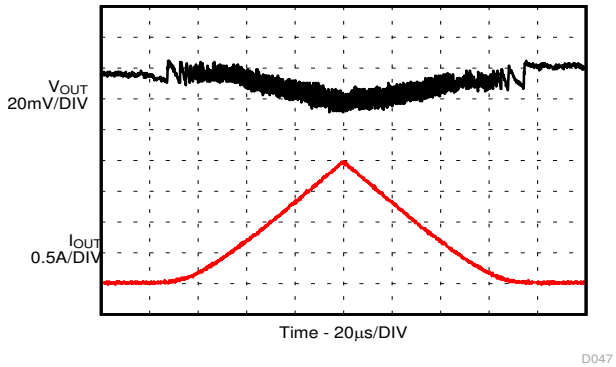


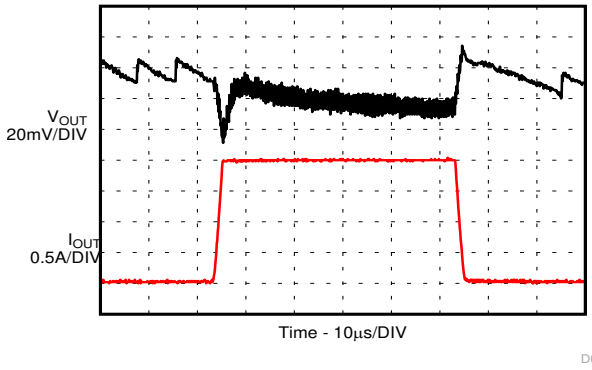
I_{OUT} = 25 mA TPSM82822

Figure 9-51. Input and Output Ripple in PSM Mode



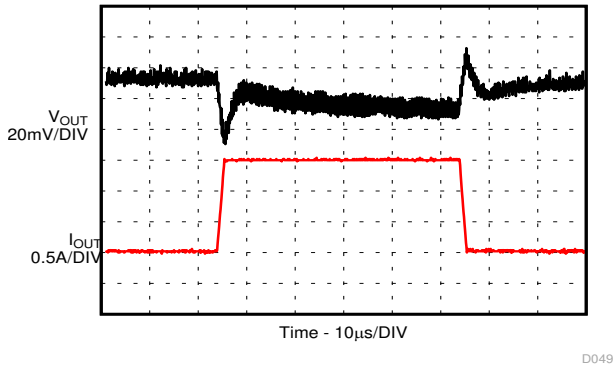
I_{OUT} = 25 mA to 2 A TPSM82822

Figure 9-52. Load Sweep



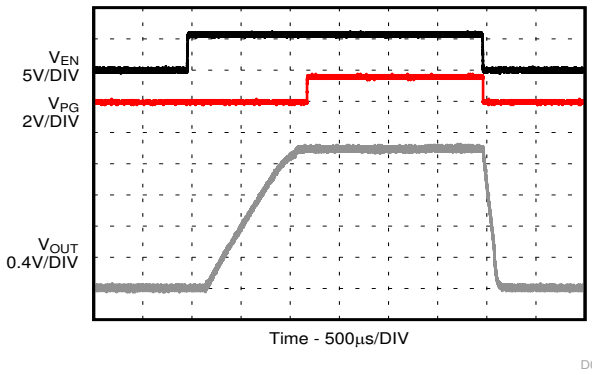
I_{OUT} = 0 A to 2 A Slew Rate = 2 A/µs TPSM82822

Figure 9-53. Load Transient



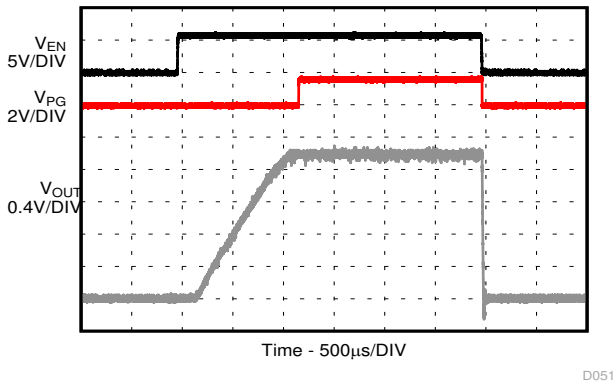
I_{OUT} = 0.5 A to 2 A Slew Rate = 2 A/µs TPSM82822

Figure 9-54. Load Transient



I_{OUT} = no load TPSM82822

Figure 9-55. Start-up / Shutdown without Load



I_{OUT} = 2 A TPSM82822

Figure 9-56. Start-up / Shutdown with Resistive Load

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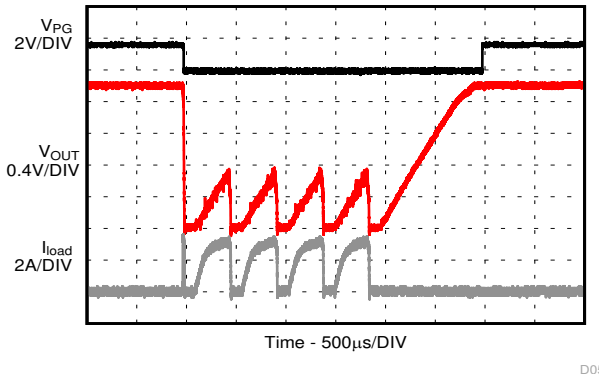
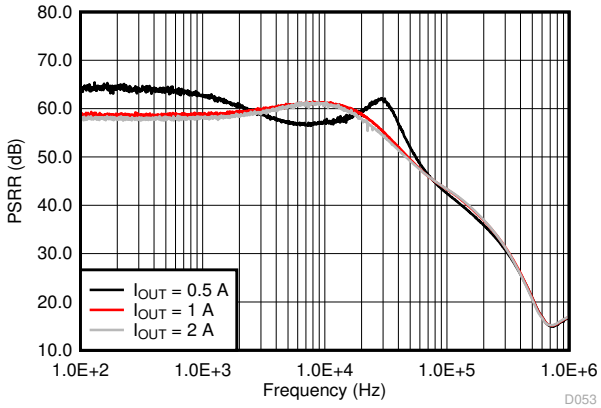


TPSM82822

Figure 9-57. Short Circuit, HICCUP Protection Entry / Exit



TPSM82822

Figure 9-58. Power Supply Rejection Ratio (PSRR)

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10 Power Supply Recommendations

The devices are designed to operate from an input supply voltage range between 2.4 V and 5.5 V. The average input current of the TPSM8282x is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

Ensure that the power supply has a sufficient current rating for the application.

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11 Layout

11.1 Layout Guidelines

- It is recommended to place all components as close as possible to the IC. The input capacitor placement must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- Refer to Figure 11-1 for an example of component placement, routing, and thermal design.
- The recommended land pattern for the TPSM8282x is shown at the end of this data sheet. For best manufacturing results, it is important to create the pads as solder mask defined (SMD). This keeps each pad the same size and avoids solder pulling the device during reflow.

11.2 Layout Example

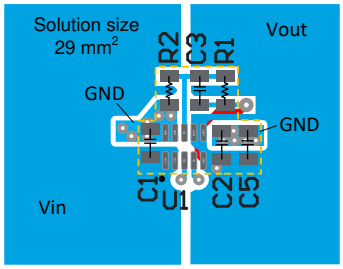

Figure 11-1. TPSM8282x PCB Layout

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11.3 Thermal Consideration

The TPSM8282x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8282x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrate the required derating in maximum output current at high ambient temperatures. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPSM82822EVM-080 Evaluation Module*, SLVUBR5

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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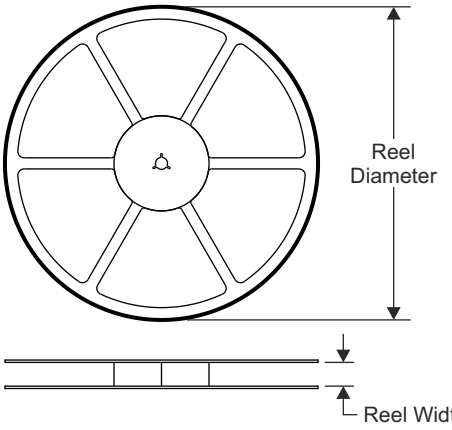
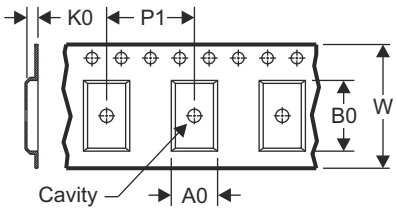
13.1 Tape and Reel Information

REEL DIMENSIONS

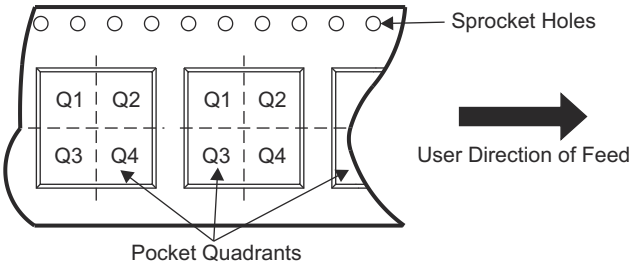


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM82821SILR	uSiP	SIL	10	3000	330.0	8.4	8.0	2.75	1.25	4.0	5.4	Q1
TPSM82822SILR	uSiP	SIL	10	3000	330.0	8.4	8.0	2.75	1.25	4.0	5.4	Q1
XPSM82821SILR	uSiP	SIL	10	3000	330.0	8.4	8.0	2.75	1.25	4.0	5.4	Q1
XPSM82822SILR	uSiP	SIL	10	3000	330.0	8.4	8.0	2.75	1.25	4.0	5.4	Q1

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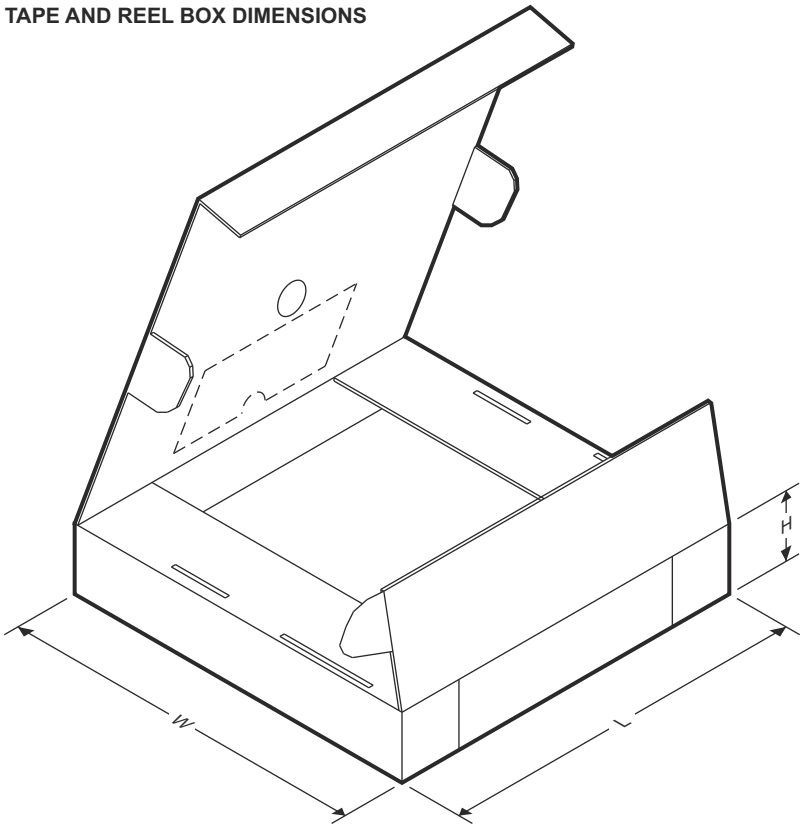
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM82821SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
TPSM82822SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
XPSM82821SILR	uSiP	SIL	10	3000	383.0	353.0	58.0
XPSM82822SILR	uSiP	SIL	10	3000	383.0	353.0	58.0

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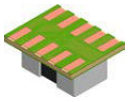
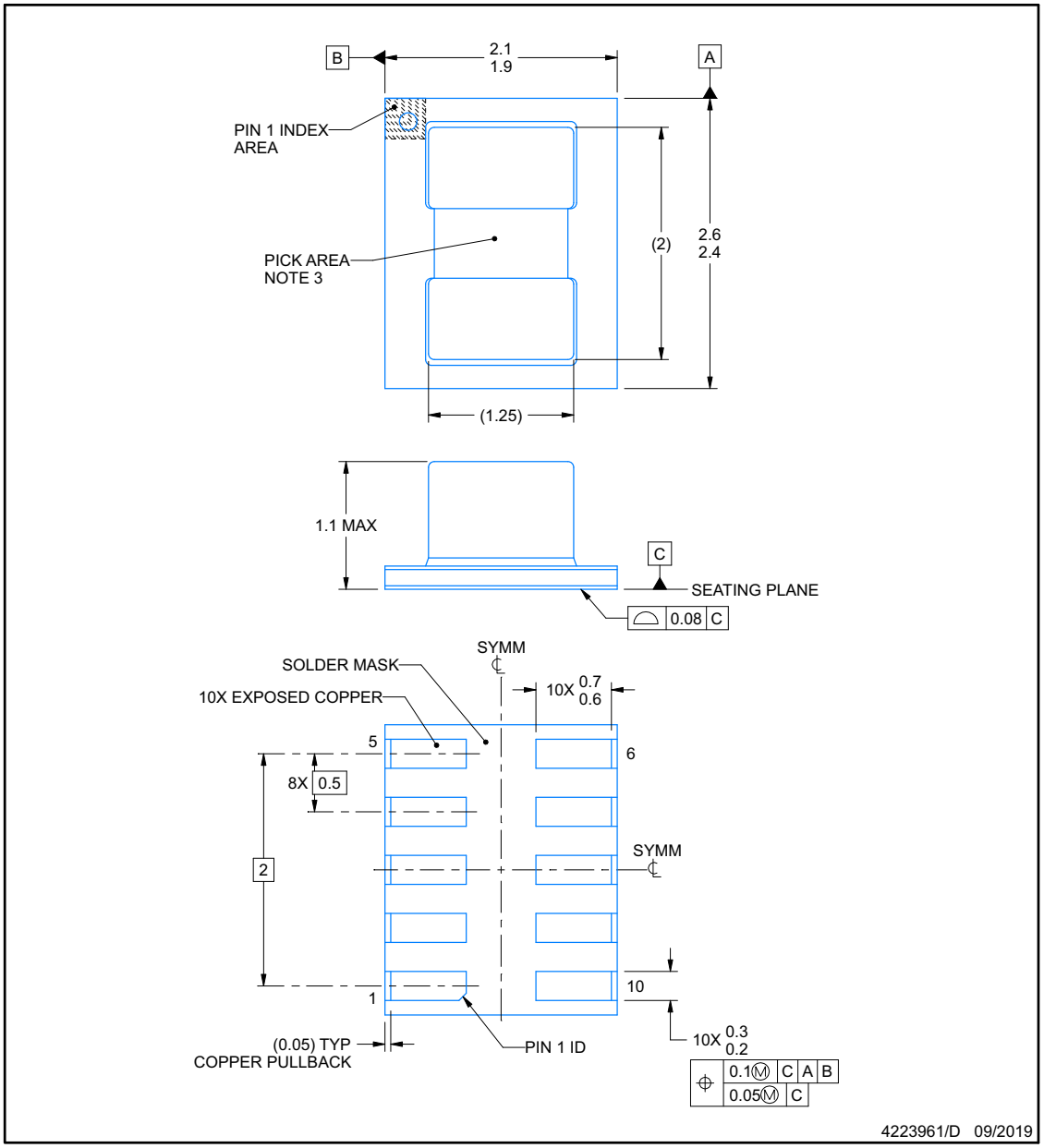


PACKAGE OUTLINE

SIL0010D

uSIP™ - 1.1 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 0.33 mm or smaller recommended.

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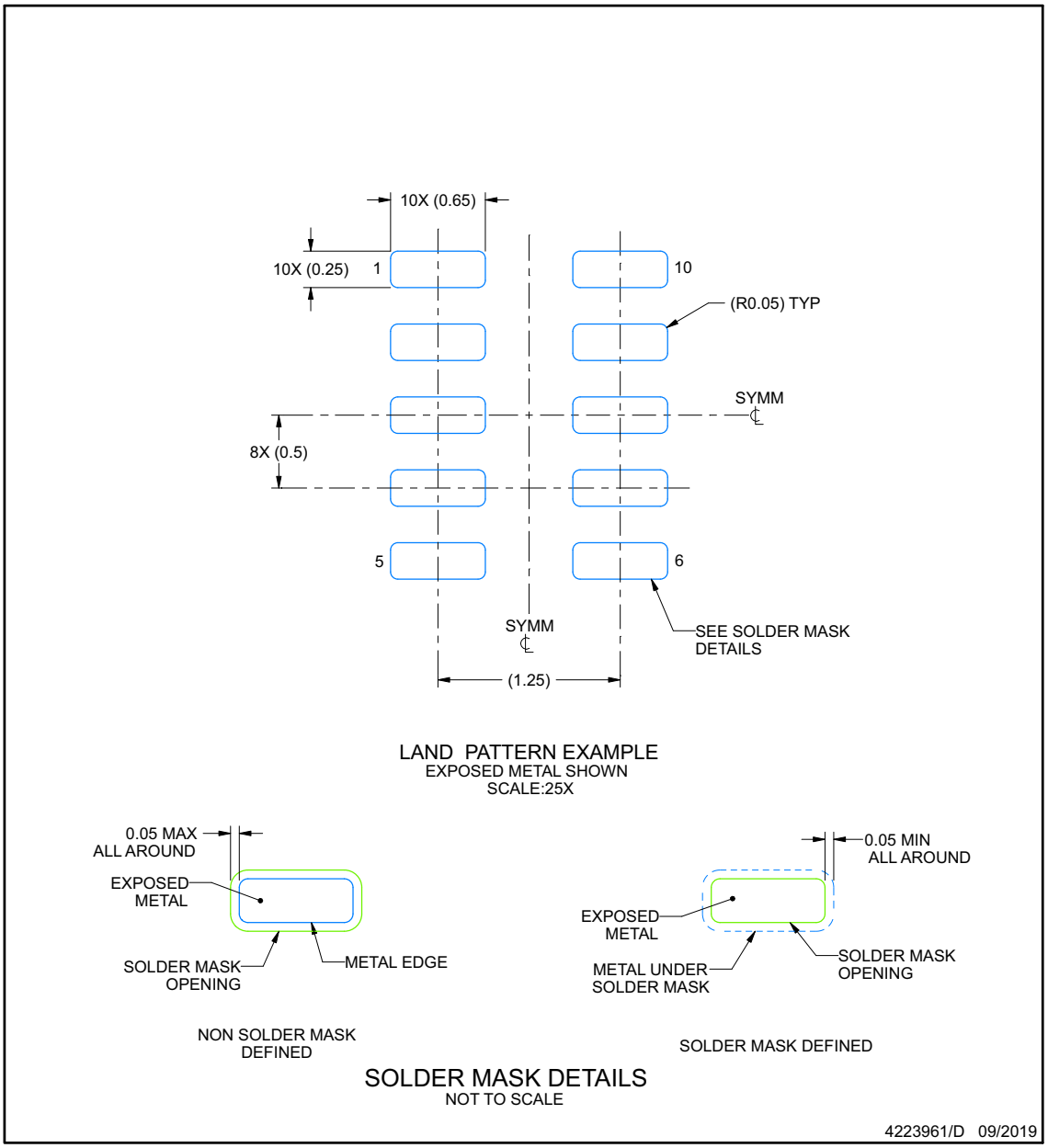
EXAMPLE BOARD LAYOUT

SIL0010D

uSIP™ - 1.1 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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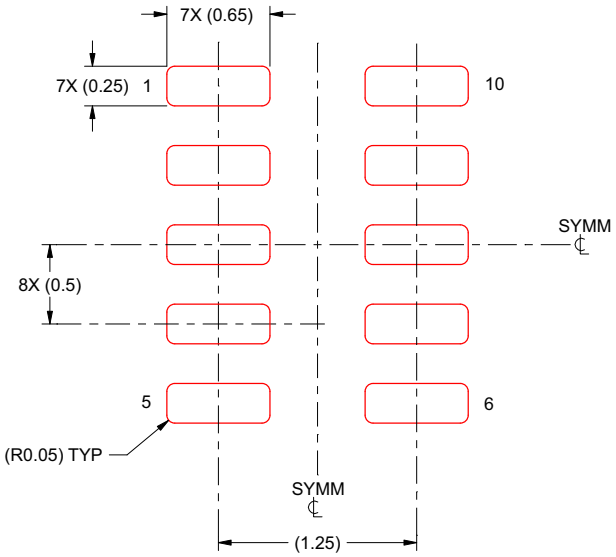
EXAMPLE STENCIL DESIGN

SIL0010D

uSIP™ - 1.1 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4223961/D 09/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM82821SILR	ACTIVE	uSiP	SIL	10	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	GA	Samples
TPSM82822SILR	ACTIVE	uSiP	SIL	10	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	G9	Samples
XPSM82821SILR	ACTIVE	uSiP	SIL	10	3000	Green (RoHS & no Sb/Br)	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	GAX	Samples
XPSM82822SILR	ACTIVE	uSiP	SIL	10	3000	Green (RoHS & no Sb/Br)	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	XX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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