TPS7A65-Q1 300-mA, 40-V, Low-Dropout Regulator With 25-µA Quiescent Current

1 Features

- Low Dropout Voltage
  - 300 mV at I_{OUT} = 150 mA
- 11-V to 40-V Wide Input Voltage Range With up to 45-V Transients
- 300-mA Maximum Output Current
- 25-µA (Typical) Ultralow Quiescent Current at Light Loads
- 3.3-V and 5-V Fixed Output Voltage With ±2% Tolerance
- Low-ESR Ceramic Output Stability Capacitor
- Integrated Fault Protection
  - Short-Circuit and Overcurrent Protection
  - Thermal Shutdown
- Low Input-Voltage Tracking
- Thermally Enhanced Power Package
  - 3-Pin TO-252 (KVU, DPAK)

2 Applications

- Qualified for Automotive Applications
- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

3 Description

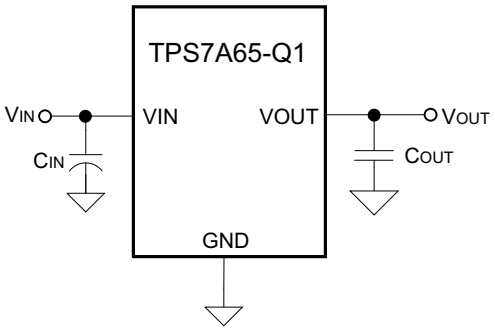
The TPS7A65-Q1 low-dropout linear voltage regulator is designed for low power consumption and quiescent current less than 25 µA in light-load applications. This device features integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, this device is well-suited in power supplies for various automotive applications.

Device Information(1)

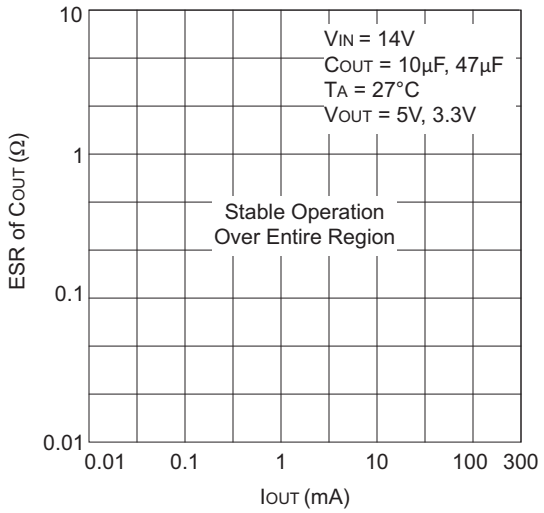
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A65-Q1	TO-252 (3)	6.60 mm × 6.10 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Schematic



Typical Regulator Stability



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2015) to Revision E — **Page**

- Changed 4 V to 11 V in *Input Voltage Range Features* bullet ... 1
- Changed V_{IN} parameter min specifications to 11 V from 5.3 V and 3.6 V ... 5
- Changed 4 V to 11 V in *Input voltage range* row in *Design Parameters* table ... 13
- Changed 4 V to 40 V in first sentence of *Power Supply Recommendations* section ... 15

Changes from Revision C (December 2011) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (November 2011) to Revision C — **Page**

- Deleted the TPS7A6533QKVURQ1 device ... 1
- Changed the Regulated Output Voltage (5.1). Added to Test Conditions "10mA to 300mA, V_{IN} = V_{OUT} + 1V to 16V" ... 5

Changes from Revision A (November 2011) to Revision B — **Page**

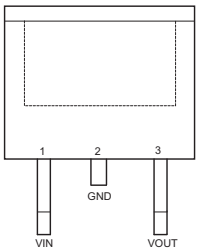
- Changed the θ_{JP} value in the Abs Max Table From: 12.7 To: 1.2°C/W ... 4

Changes from Original (May 2010) to Revision A — **Page**

- Removed all KKT information. ... 4

5 Pin Configuration and Functions

KVU Package
3-Pin TO-252
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	GND	I/O	Ground pin: This is signal ground pin of the IC.
3	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3 V or 5 V, as applicable) pin with a limitation on maximum output current. To achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and the GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(2)(3)		45	V
V_{OUT}	Regulated output		7	V
θ_{JP}	Thermal impedance junction to exposed pad		1.2	°C/W
T_A	Operating ambient temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute negative voltage on these pins not to go below –0.3 V.
(3) Absolute maximum voltage for duration less than 480 ms.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	11	40	V
V_{EN}	Enable pin voltage	4	40	V
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)			TPS7A65-Q1 KVU (TO-252) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K profile(2)	29.3	°C/W
		Low-K profile(3)	38.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter		3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter		8.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(3) The thermal data is based on JEDEC standard low-K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.

6.5 Electrical Characteristics

V_{IN} = 14 V, T_J = –40ºC to +150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN PIN)						
V_{IN}	Input voltage	Fixed 5-V output, I_{OUT} = 1 mA	11		40	V
		Fixed 3.3-V output, I_{OUT} = 1 mA	11		40	
$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2 V to 18 V, I_{OUT} = 0.01 mA to 0.75 mA		25	40	µA
$V_{IN-UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
$V_{IN(POWERUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
REGULATED OUTPUT VOLTAGE (VOUT PIN)						
V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3 V or 5 V as applicable), I_{OUT} = 10 mA, 10 mA to 300 mA, V_{IN} = V_{OUT} + 1 V to 16 V	–2%		2%	
$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 5 V			15	mV
		V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 3.3 V			20	
$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10 mA to 300 mA, V_{IN}= 14 V, V_{OUT} = 5 V			25	mV
		I_{OUT} = 10 mA to 300 mA, V_{IN} = 14 V, V_{OUT} = 3.3 V			35	
$V_{DROPOUT}$ (1)	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 250 mA			500	mV
		I_{OUT} = 150 mA			300	
R_{SW} (2)	Switch resistance	VIN to VOUT resistance			2	Ω
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
I_{CL}	Output current limit	V_{OUT} = 0 V (VOUT pin is shorted to ground)	350		1000	mA
PSRR (2)	Power-supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 100 Hz, V_{OUT} = 5 V, V_{OUT} = 3.3 V		60		dB
		$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 150 kHz, V_{OUT} = 5 V, V_{OUT} = 3.3 V		30		
TEMPERATURE						
$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
T_{HYST}	Thermal shutdown hysteresis			10		ºC

(1) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (3.3 V or 5 V) drops by 100 mV at specified loads.
(2) Specified by design; not tested.

6.6 Dissipation Ratings

JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
JEDEC Standard PCB - low K, JESD 51-3	3-pin KVU	3.24	38.6	1.68
JEDEC Standard PCB - high K, JESD 51-5	3-pin KVU	4.27	29.3	2.22

6.7 Typical Characteristics

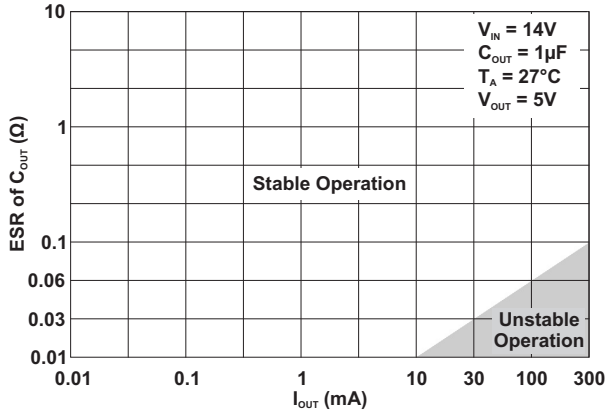


Figure 1. ESR vs Load Current

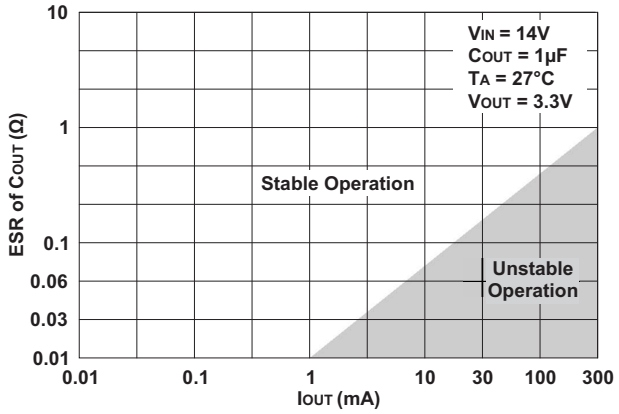


Figure 2. ESR vs Load Current

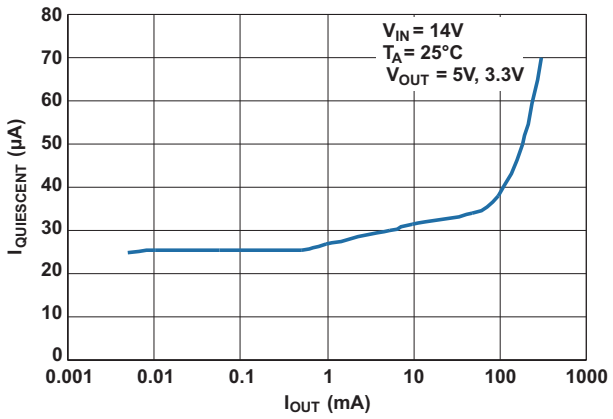


Figure 3. Quiescent Current vs Load Current

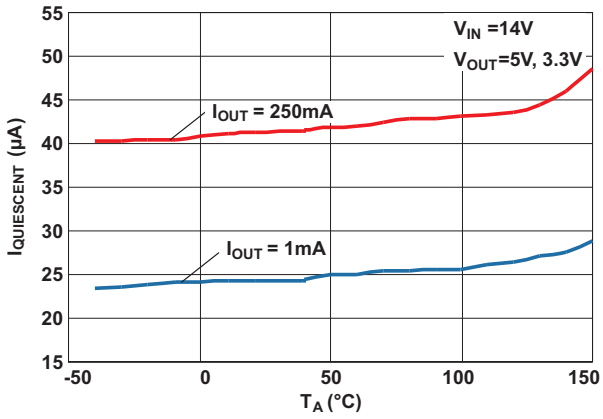


Figure 4. Quiescent Current vs Ambient Air Temperature

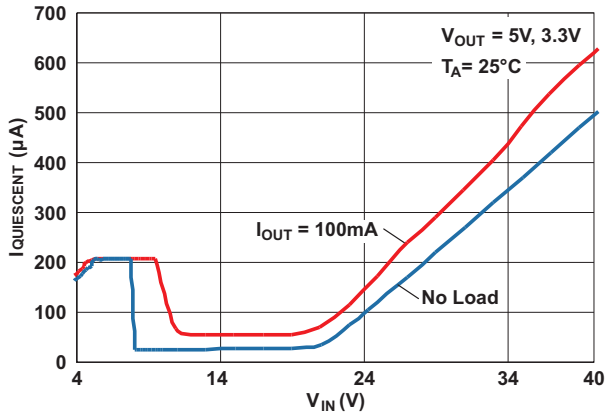


Figure 5. Quiescent Current vs Input Voltage

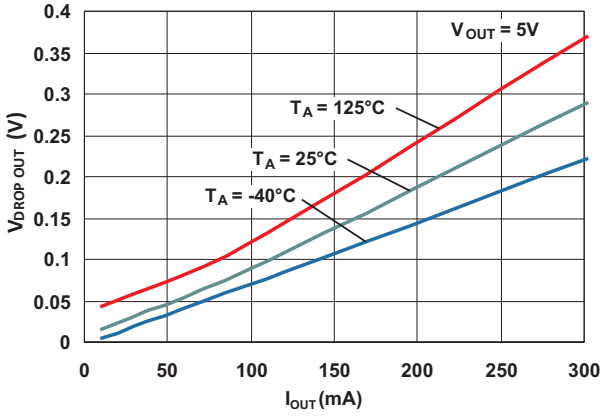


Figure 6. Dropout Voltage vs Load Current (1)

(1) Dropout voltage is measured when the output voltage drops by 100 mV from the regulated output voltage level. (For example, the drop out voltage for TPS7A6550 is measured when the output voltage drops down to 4.9 V from 5 V.)

Typical Characteristics (continued)

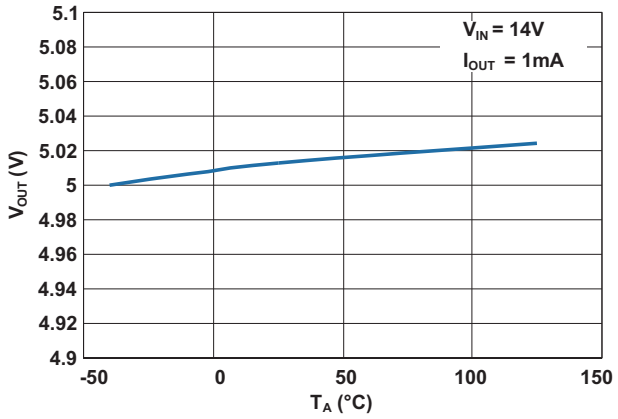


Figure 7. Output Voltage vs Ambient Air Temperature

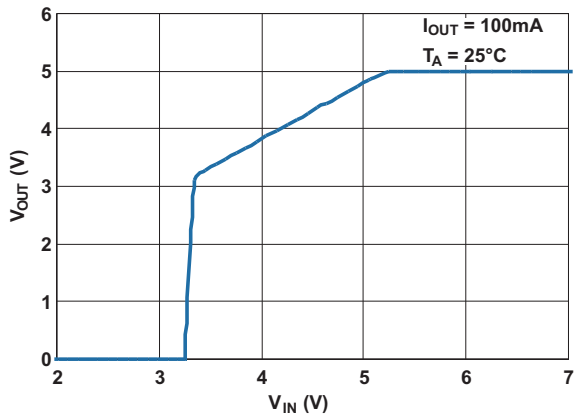


Figure 8. Output Voltage vs Input Voltage

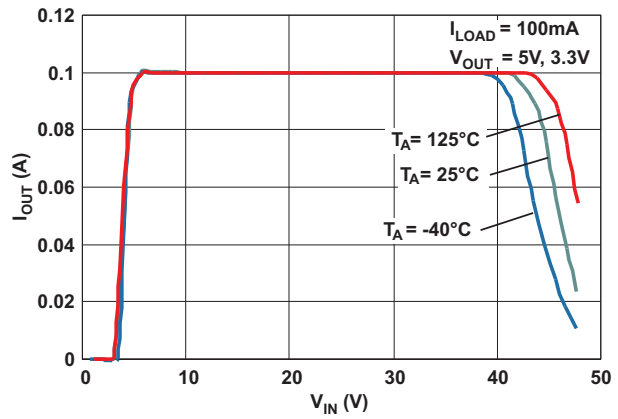


Figure 9. Output Current vs Input Voltage

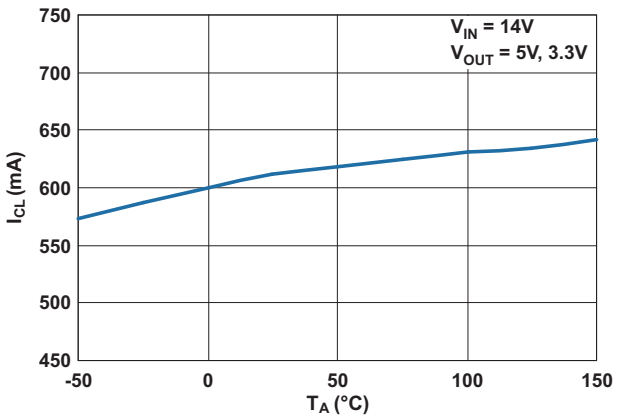


Figure 10. Output Current Limit vs Ambient Air Temperature

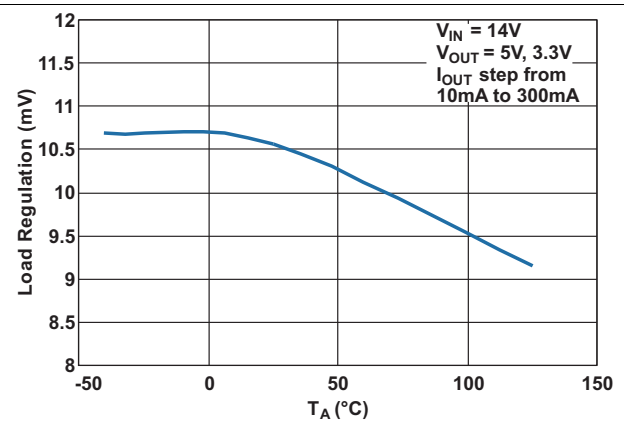


Figure 11. Load Regulation vs Ambient Air Temperature

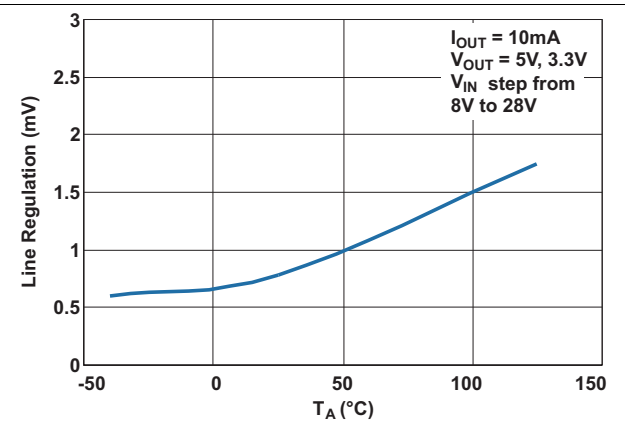


Figure 12. Line Regulation vs Ambient Air Temperature

Typical Characteristics (continued)

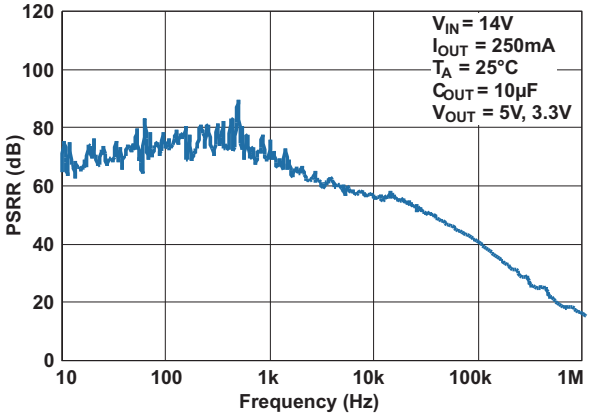


Figure 13. PSRR at Heavy Load Current

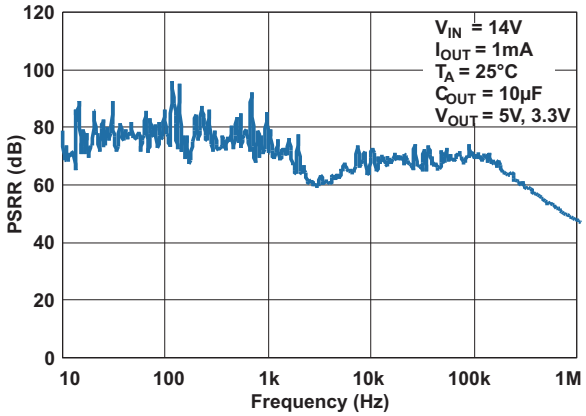


Figure 14. PSRR at Light Load Current

7 Detailed Description

7.1 Overview

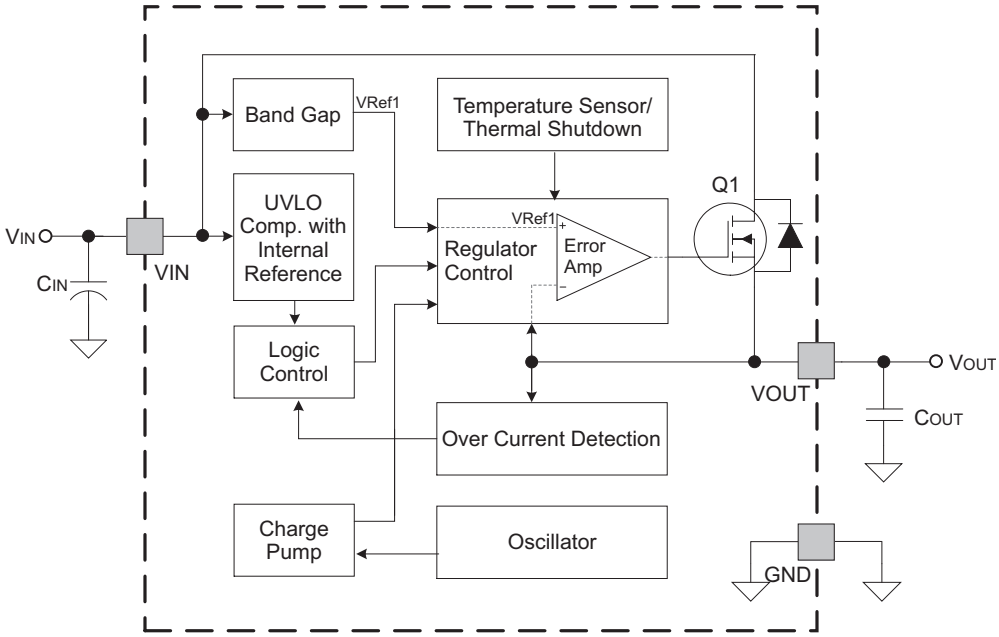
The TPS7A65-Q1 is a monolithic low-dropout linear voltage regulator designed for low-power consumption and quiescent current less than 25 µA in light-load applications. Because of an integrated fault protection, this device is well-suited in power supplies for various automotive applications.

This device is available in two fixed-output-voltage versions as follows:

- 5-V output version (TPS7A6550-Q1)
- 3.3-V output version (TPS7A6533-Q1)

See *Feature Description* for full descriptions of the features of the TPS7A65-Q1 voltage regulator.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Up

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{IN(POWERUP)}$) level, the output voltage begins to ramp up; see Figure 15.

Feature Description (continued)

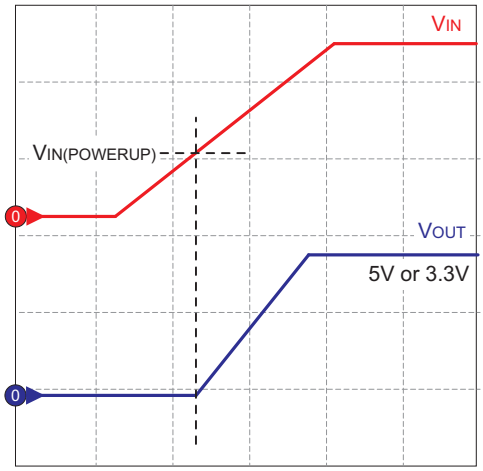


Figure 15. Power-Up Sequence

7.3.2 Charge-Pump Operation

This device has an internal charge pump that turns on or off depending on the input voltage and the output current. The charge pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge-pump switching thresholds are hysteretic. Figure 16 and Figure 17 show typical switching thresholds for the charge pump at light (I_{OUT} < approximately 2 mA) and heavy (I_{OUT} > approximately 2 mA) loads, respectively.

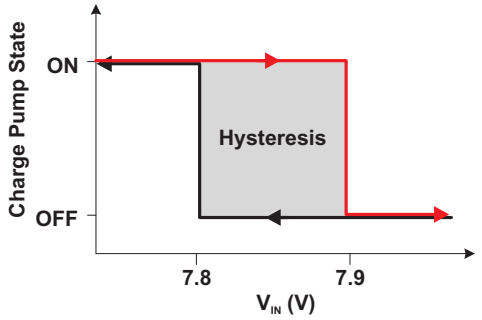


Figure 16. Charge-Pump Operation at Light Loads

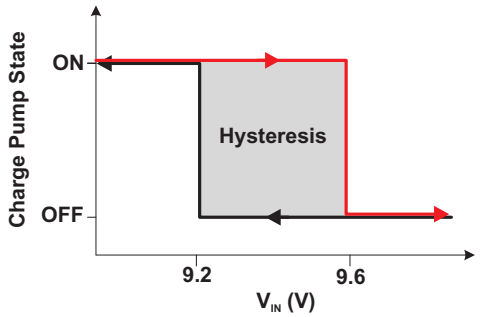


Figure 17. Charge-Pump Operation at Heavy Loads

Feature Description (continued)

7.3.3 Low-Power Mode

At light loads and high input voltages (V_{IN} > approximately 8 V such that charge pump is off) the device operates in the low-power mode and the quiescent current consumption decreases to 25 µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	CHARGE PUMP ON	CHARGE PUMP OFF
I_{OUT} < approximately 2 mA (light load)	250 µA	25 µA (low-power mode)
I_{OUT} > approximately 2 mA (heavy load)	280 µA	70 µA

7.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$) as shown in Figure 18. This ensures that the regulator does not latch into an unknown state during low input-voltage conditions. The regulator normally powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ threshold.

7.3.5 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}) as shown in Figure 18. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

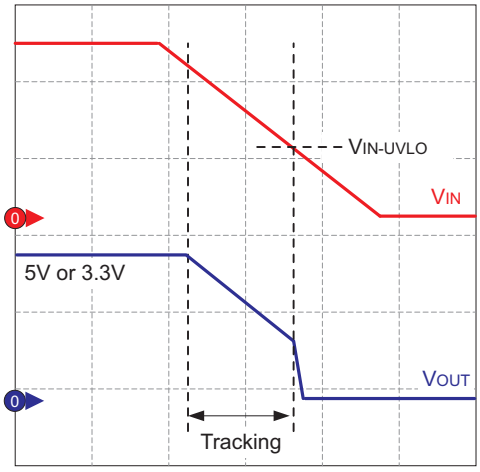


Figure 18. Undervoltage Shutdown and Low-Voltage Tracking

7.3.6 Integrated Fault Protection

This device features integrated fault protection to make them ideal for use in automotive applications. To keep the device in a safe area of operation during certain fault conditions, the device uses internal current limit protection and current limit foldback to limit the maximum output current. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, limiting current through the pass element to I_{CL} protects the device from excessive power dissipation.

7.3.7 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again. Figure 19 shows this.

Feature Description (continued)

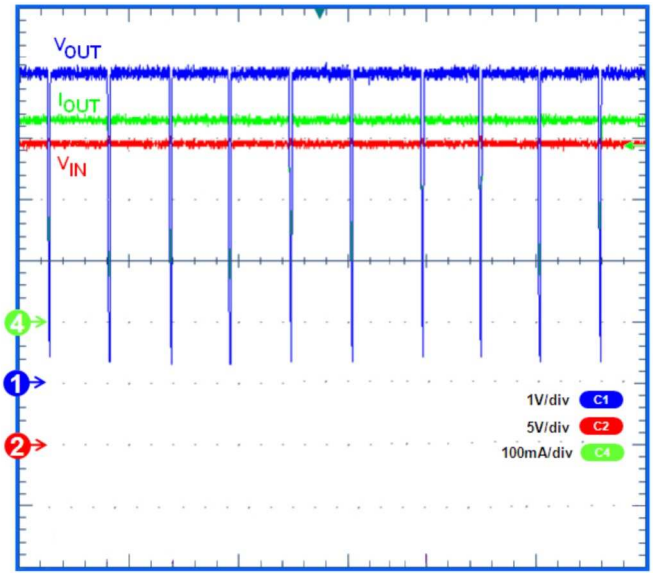


Figure 19. Thermal Cycling Waveform for TPS7A6550-Q1 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 4 V

The TPS7A65-Q1 device operates with input voltage above 4 V. The typical UVLO voltage is 3.16 V, the device can operate at input voltage lower than 4 V. But at input voltage below the actual UVLO, the device shuts down.

7.4.2 Operation With V_{IN} Larger Than 4 V

When V_{IN} is greater than 4 V, if the input voltage is higher than V_{OUT} plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A65-Q1 is a low-dropout linear voltage regulator designed for low power consumption and quiescent current less than 25 µA in light-load applications. This device features integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, this device is well-suited in power supplies for various automotive applications.

8.2 Typical Application

A typical application circuit for TPS7A65-Q1 is Figure 20. Depending on the end application, one may use different values of external components. An application may require a larger output capacitor during fast load steps to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. The user can additionally connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

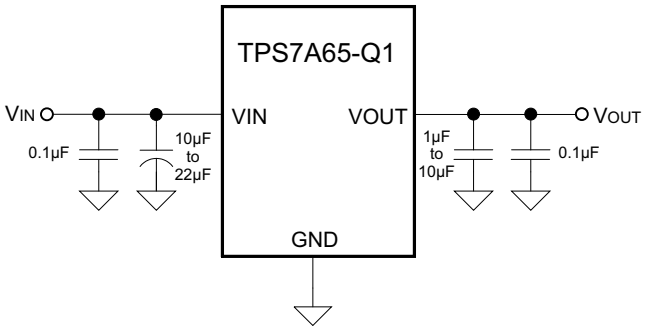


Figure 20. Typical Application Schematic

8.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	11 V to 40 V
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	1 µF to 10 µF

8.2.2 Detailed Design Procedure

When using the TPS7A6533-Q1, TPS7A6550-Q1, TI recommends adding a 10-µF to 22-µF capacitor to the input to keep the input voltage stable. TI also recommends adding a 1-µF to 10-µF low ESR ceramic capacitor to get a stable output.

8.2.3 Application Curve

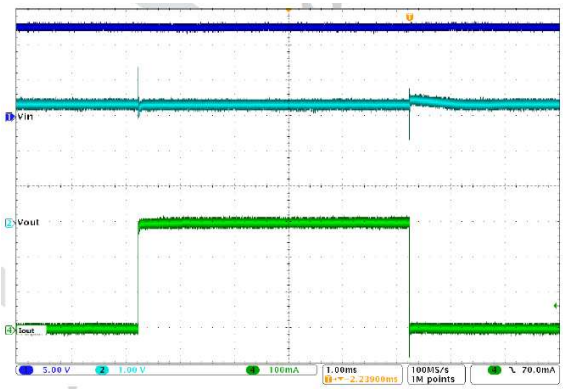


Figure 21. TPS7A6533-Q1 Load Transient Waveform

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 11 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A65-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10 μF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as large as possible and putting enough thermal vias on the thermal pad.

10.1.1 Power Dissipation and Thermal Considerations

Calculate the power dissipated in the device using Equation 1.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT)}) + I_{QUIESCENT} \times V_{IN}$$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage
- $I_{QUIESCENT}$ = quiescent current. (1)

$I_{QUIESCENT} << I_{OUT}$; therefore, ignore the term $I_{QUIESCENT} \times V_{IN}$ in Equation 1.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 2.

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-ambient air thermal impedance. (2)

Calculate the rise in junction temperature due to power dissipation using Equation 3.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), calculate the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate using Equation 4.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (4)$$

Example

If I_{OUT} = 100 mA, V_{OUT} = 5 V, V_{IN} = 14 V, $I_{QUIESCENT}$ = 250 µA and θ_{JA}= 30°C/W, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 27°C. For a maximum junction temperature of 150°C, maximum ambient air temperature at which the device can operate is 123°C.

For adequate heat dissipation, TI recommends soldering the power pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Figure 22 shows power derating curves for the TPS7A65-Q1 family of devices in the KVU (DPAK) package.

Layout Guidelines (continued)

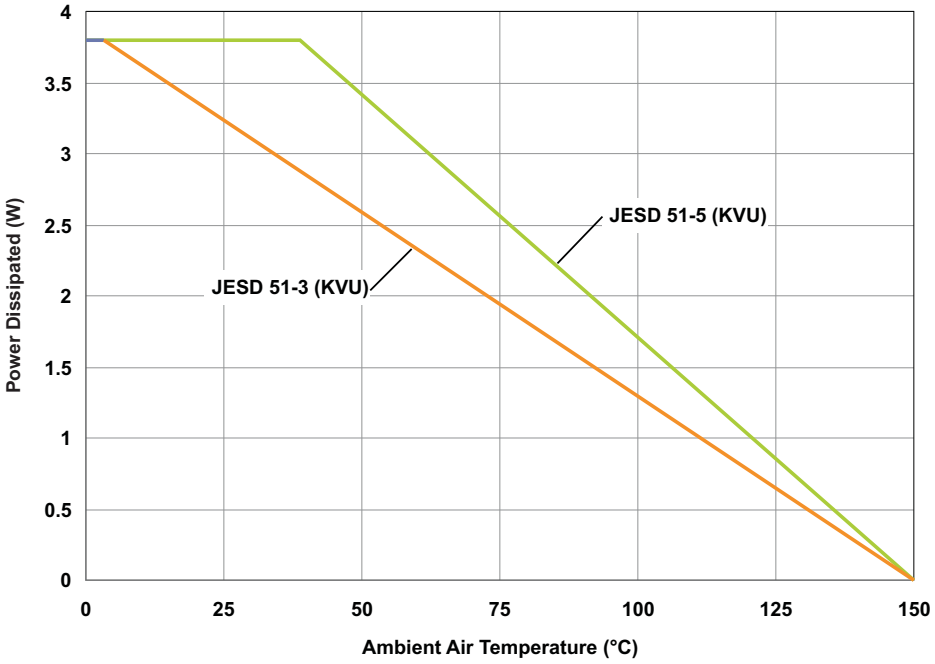


Figure 22. Power Derating Curves

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad. Figure 23 (a) and (b) show this. Further, a design can improve the heat-spreading capabilities of a PCB considerably by using a thicker ground plane and a thermal land pad with a larger surface area.

Layout Guidelines (continued)

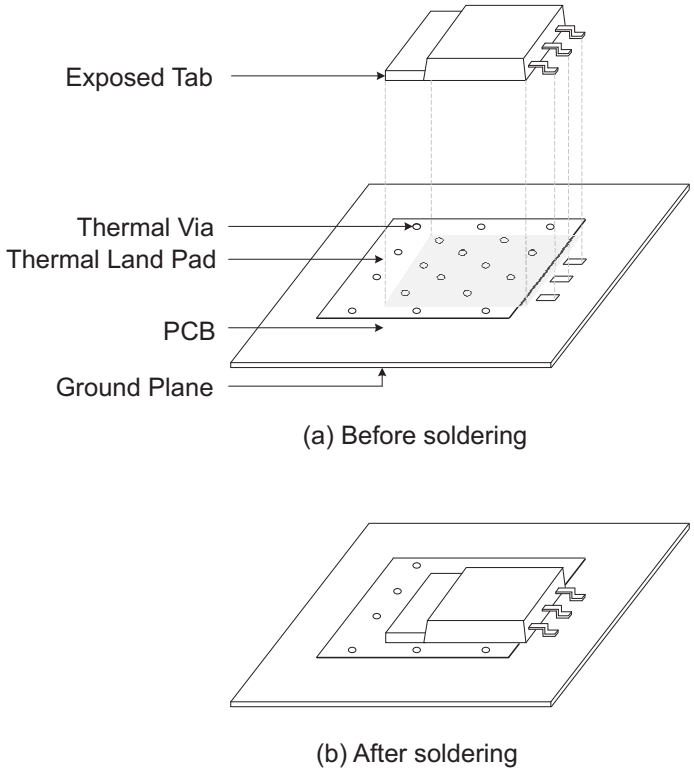


Figure 23. Using a Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Keeping other factors constant, the surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 24 shows the variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for the KVU package.

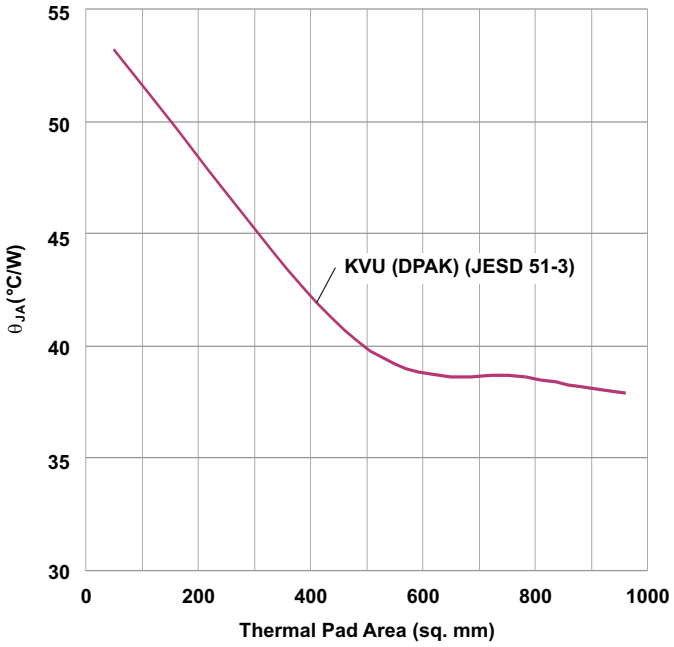


Figure 24. θ_{JA} vs Thermal Pad Area

10.2 Layout Example

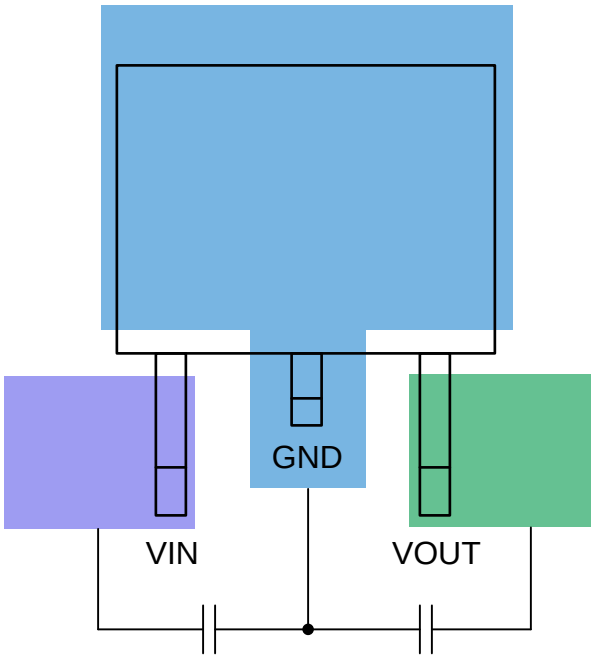


Figure 25. Layout Recommendation

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6533QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6533Q1	Samples
TPS7A6550QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6550Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

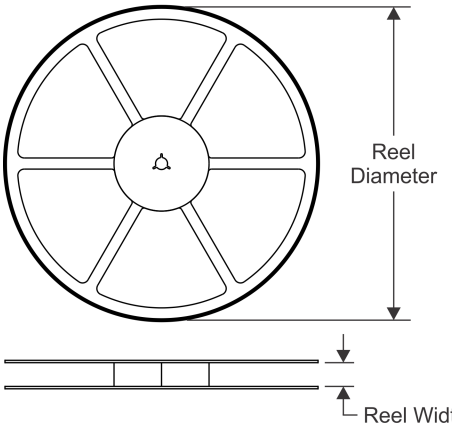
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

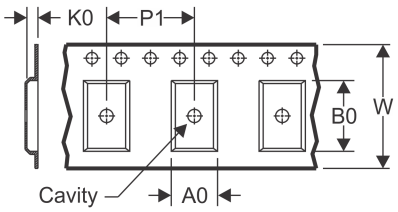
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

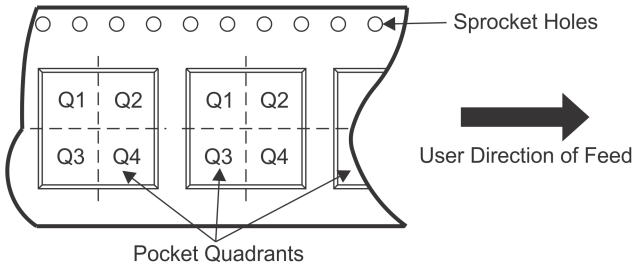


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

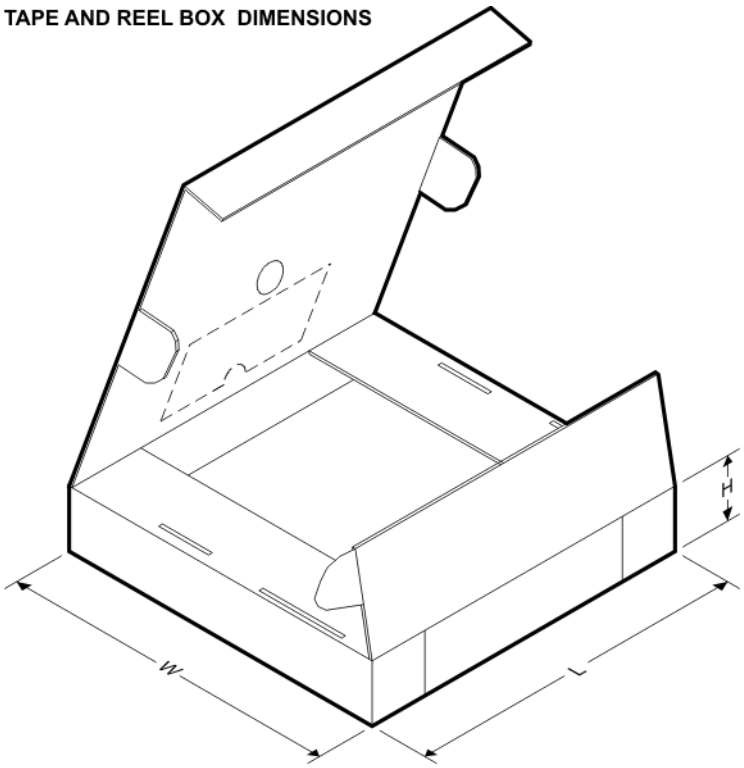
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



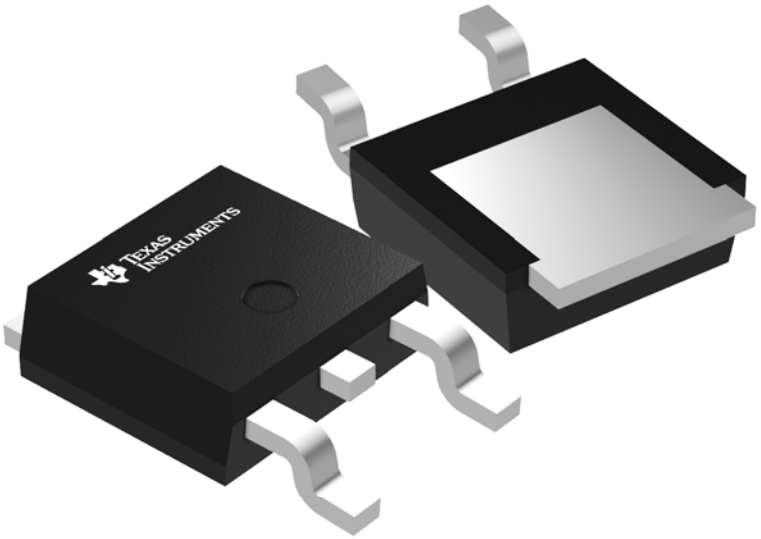
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



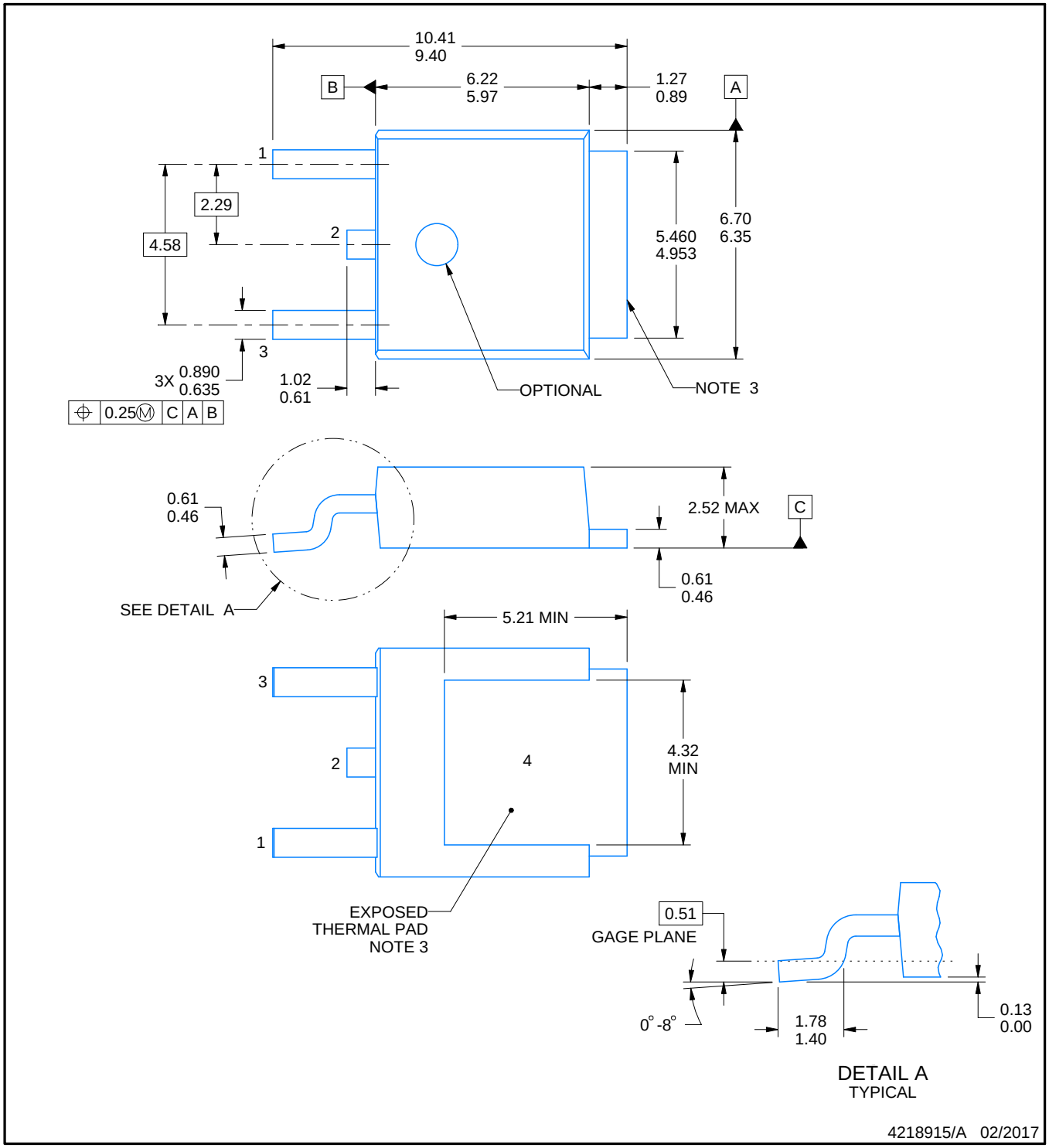
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

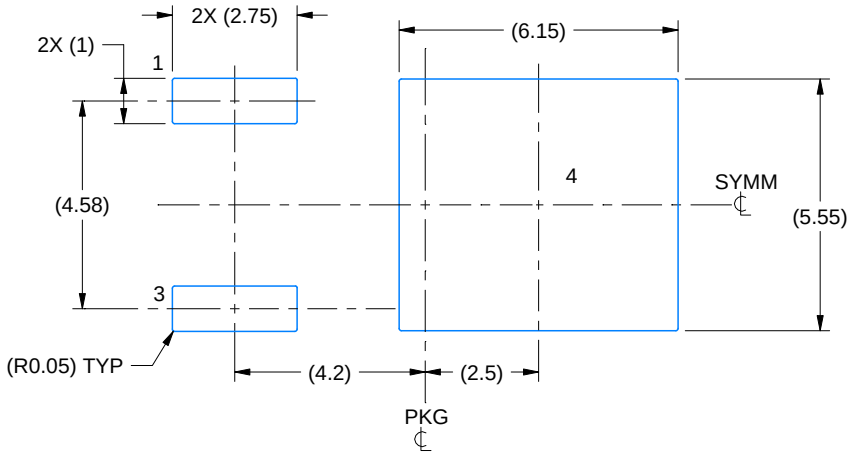
TO-252 - 2.52 mm max height

TO-252

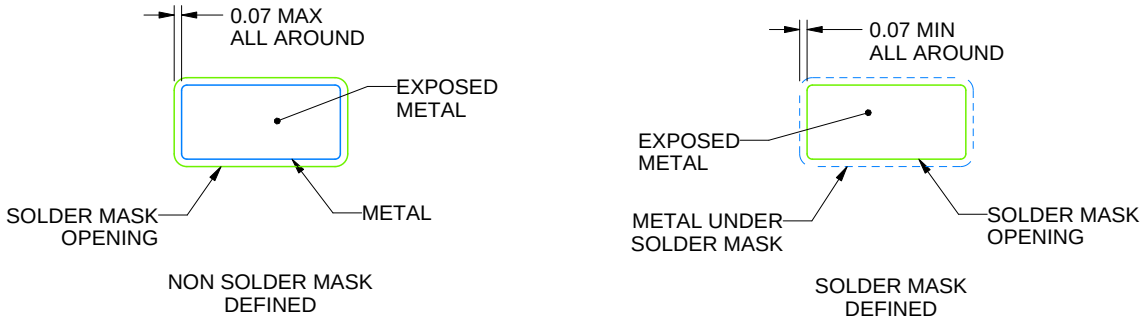


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

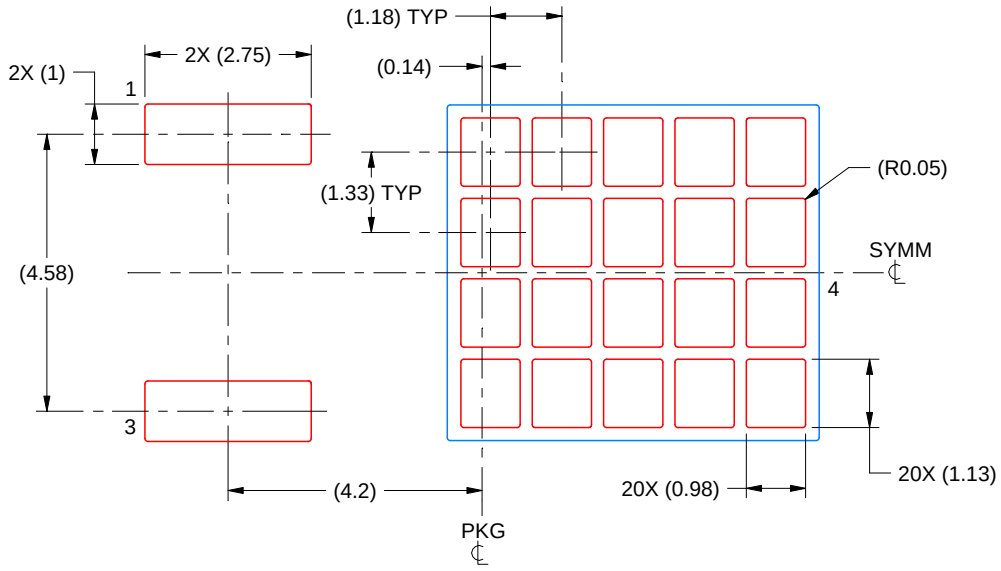
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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