SiT3921

Digitally Controlled Differential Oscillator (DCXO)

Preliminary

The Smart Timing Choice™

Features

- Factory programmable between 1 MHz and 220 MHz accurate to 6 decimal places
- Digital controlled pull range
- Widest pull range options: ±25, ±50, ±100, ±200, ±400, ±800, ±1600 PPM
- Superior pull range linearity of <= 1%, 10 times better than quartz
- < 1ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 5.0 mm x 3.2 mm and 7.0 mm x 5.0 mm Contact SiTime for 3.2 mm x 2.5 mm package
- For frequencies higher than 220 MHz, refer to SiT3922 datasheet

Applications

- Ideal for SONET, Video, Instrumentation, Satellite applications
- Telecom, networking, broadband

Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common DC and AC Characteristics						
Output Frequency Range	f	1	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power, supply voltage and load change
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	–	10	ms	
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
Pull Range	PR	±25, ±50, ±100, ±200, ±400, ±800, ±1600			PPM	See the last page for Absolute Pull Range, APR table
Linearity	Lin	–	0.2	1	%	
Frequency Change Polarity	–	Positive Slope			–	
1-year Aging		-2	–	+2	PPM	First year @ 25°C
10-year Aging		-5	–	+5	PPM	@ 85°C
Input Low Voltage	VIL	–	–	0.2xVdd	V	
Input Middle Voltage	VIM	0.4xVdd	–	0.6xVdd	V	
Input High Voltage	VIH	0.8xVdd	–	–	V	
Input High or Low Pulse Width	T_logic	500	–	–	ns	
Input Middle Pulse Width	T_middle	500	–	–	ns	
Input to Output Isolation					TBD	
Input Impedance	Zin	TBD	–	–	kΩ	Pin 1
Input Capacitance	Cin	–	–	TBD	pF	Pin 1
LVPECL, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
Maximum Output Current	I-driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 9
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 9
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 9
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	105	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.5	0.75	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

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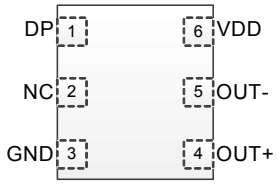
Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC, and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
Differential Output Voltage	VOD	200	350	500	mV	See Figure 12
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 12
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 12
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 12
Rise/Fall Time	Tr, Tf	360	495	600	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	105	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.5	0.75	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

Pin Description

Pin	Map	Functionality	
1	DP	Input	Digital programming pin
2	NC	NA	No connect
3	GND	Power	VDD power supply ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65V)	1,000+	–	years

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

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Default Startup Condition

The SiT3921 starts up at its factory programmed frequency and settings. The control register values are initialized all zeros, effectively setting the frequency to the middle of the control range.

Frequency Control Protocol Description

The device includes two DCXO registers; writing to these registers controls the output frequency. Data for each register is written to the device using a data frame.

Data Frame Format

Each frame consists of 40 bits. A frame has 3 parts:

- The header, 16 bit

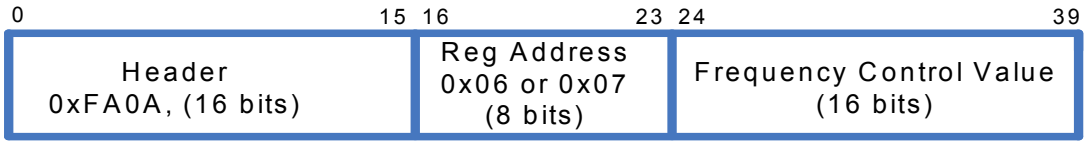
- Register address, 8 bit

- The data word (represented as 2's complement numbers), 16 bit.

Bits are sent MSB first.

Frames are sent LS word first in mode 2.

The header allows the devices to recognize that the master is initiating communication. The header includes the device address, which is factory programmable. The valid header is 0xFAIA, where "I" can be a hex digits from 0 to F. If not specified at the order time, it will be defaulted to zero. In this document in all examples and text, the device address is considered to be zero (default).



Frequency Control Mode 1

In this resolution mode, only one frame per frequency update is required, and the output frequency is updated at the end of each frame. The length of the frequency control data is 16 bits, and is written to the device as shown below:

Figure 1. Frequency Control Mode 1

Frequency Control Mode 2

In this mode, two frames per frequency update are required, and frequency is only updated at the end of the second frame. The frequency control value in this mode is 23 bits. This value is written to the device in two frames as follows:

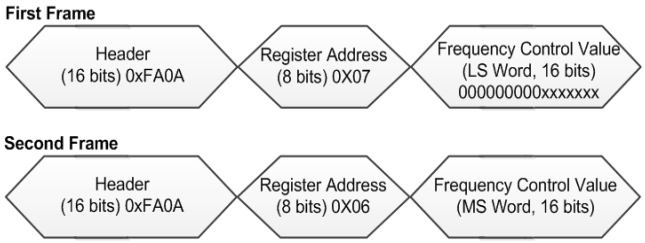


Figure 2. Frequency Control Mode 2

Resolution and Update Rate for Mode 1

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	25 K
±50	1.5	25 K
±100	3	25 K
±200	6	25 K
±400	12	25 K
±800	25	25 K
±1600	49	25 K

Resolution and Update Rate for Mode 2

Pull Range (PPM)	Step Resolution (ppb)	Max Update Rate (Updates Per Second)
±25	1	12.5 K
±50	1	12.5 K
±100	1	12.5 K
±200	1	12.5 K
±400	1	12.5 K
±800	1	12.5 K
±1600	1	12.5 K

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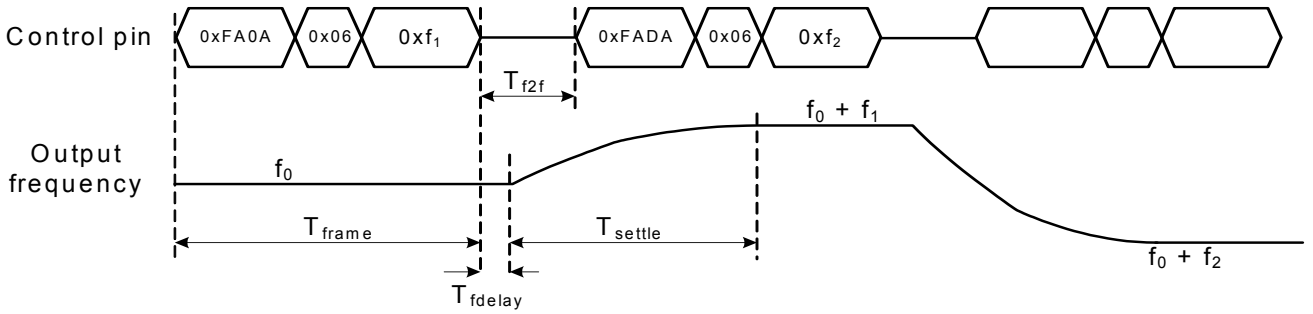

Figure 3. Mode 1 Frame Timing

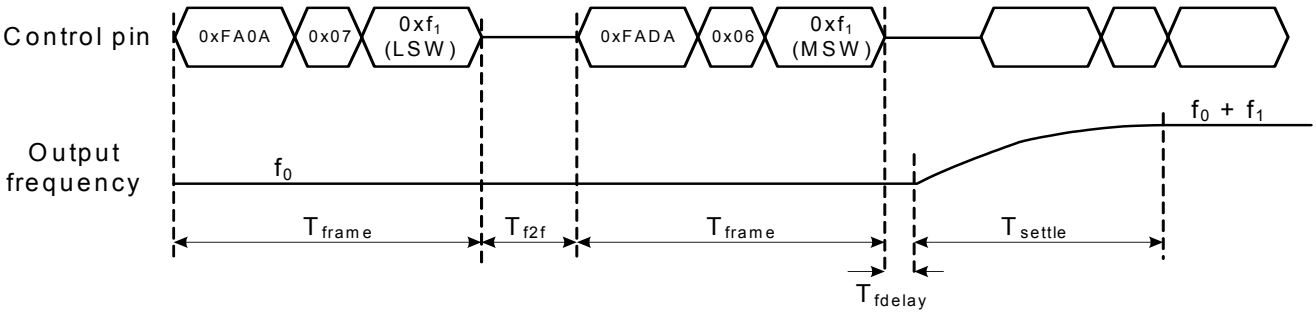

Figure 4. Mode 2 Frame Timing

Frame Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Frame Length	T_{frame}	40	—	µS
Frame to Frame Delay	T_{f2f}	2	—	µS
Frequency Settling Time	T_{settle}	—	30	µS
Frame to Frequency Delay	T_{fdelay}	—	8	µS

Calculating Pull Range PPM offset

The frequency control value must be encoded as a 2's complement number (16-bit in mode 1 and 23-bit in mode 2), representing the full scale range of the device. For example, for a +/-1600ppm device in mode 2, the 23-bit number represents the full +/-1600ppm range.

The upper 16 bits of the value are written to address 0x06. If the high-resolution register (address 0x07) is used, the other 7 bits are written to the lowest seven bits of address 0x07.

Here are the steps to calculate the frequency control value:

1. Find the scale factor (calculated for half of the pull range) from the tables below where PR is the Pull Range:

K (scale)Factor

Mode	K = Scale Factor
1	(2^15-1) / (PR*1.00135625)
2	(2^22-1) / (PR*1.00135625)

2. Enter the desired_PPM in equation below:
   Frequency control (decimal value) = round (desired_PPM * K).
3. For any frequency shifts (positive or negative PPM), convert the frequency control value to a 2's complement binary number.

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Two examples follow:

Example 1

This example shows how to shift the frequency by +245.6 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(245.6 * K) = 642954
23-bit value = 0x09CF8A

LS Word value = 0x000A (to be written to address 0x07)
MS Word value = 0x139F (to be written to address 0x06)
Write LS Word: 0xFA0A 07 000A (Frequency will not update)
Write MS Word: 0xFA0A 06 139F (Frequency updates after write)

Example 2

This example shows how to shift the frequency by -831.2 ppm in a device with ±1600 pull range using Mode 2 (23-bit):

Decimal value: round(abs(831.2 * K) = 2175989
23-bit abs binary value: 01000010011001111110101
23-bit 2's comp binary value: 1011110110011000 0001011
LS Word value = 0x 000B
MS Word value = 0x BD98
Write LS Word: 0xFA0A 07 000B (Frequency will not update)
Write MS Word: 0xFA0A 06 BD98 (Frequency updates after write)

Physical Interface

The SiTime DCMO uses a serial input interface to adjust the frequency control value. The interface uses a one-wire tri-level return-to-middle signaling format. *Figure 5* below shows the signal waveform of the interface.

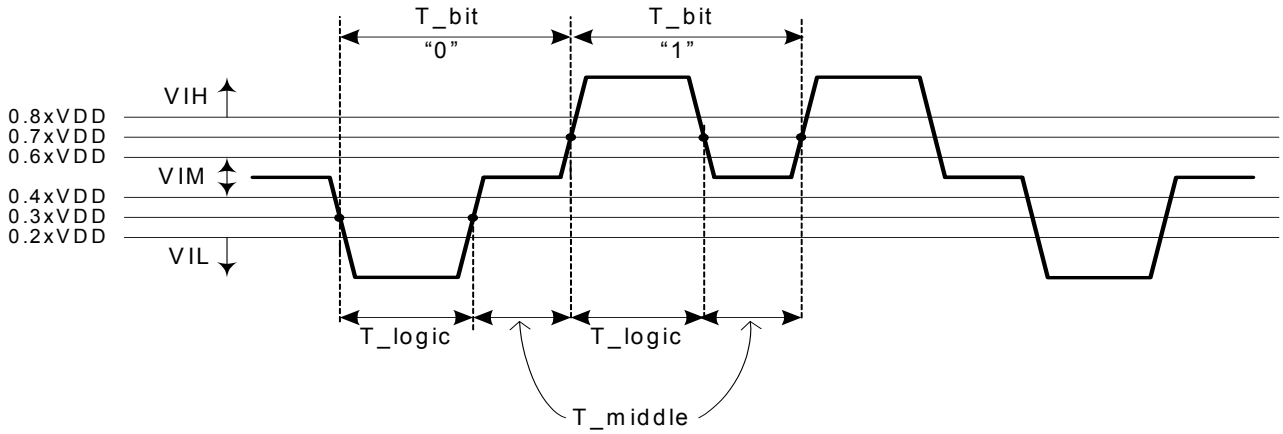

Figure 5. Serial 1-Wire Tri-Level Signaling

A logical bit "1" is defined by a high-logic followed by mid-logic. A logical bit "0" is defined by a low-logic followed by mid-logic. The voltage ranges and time durations corresponding to low-logic, high-, and mid-logic are illustrated in *Figure 5* and specified in electrical specification table.

The overall baud rate is computed as below:

$$baud\_rate = \frac{1}{T\_bit}$$

Figure 6 shows a simple circuit to generate tri-level circuit with a general purpose IO (GPIO) with tri-state capability. Most FPGAs and micro controllers/processors include such GPIOs. If the GPIO does not support tri-state output, two IO s may be used in combination with external tri-state buffer to generate the tri-level signal; an example of such buffer is the SN74LVC1G126. The waveform at the output of the tri-state buffer is shown in *Figure 7*. When the GPIO drives Low or High voltage, the rise/fall times are typically fast (sub-5ns range). When the output is set to Hi-Z, the output settles at middle voltage with a RC response. The time constant is determined based on the total capacitance on frequency control pin and the parallel resistance of the pull-up and pull-down resistors. The time constant in most practical situations will be less than 50ns; this necessitate choosing longer T_middle to allow the RC waveform to settle within 5% or so.

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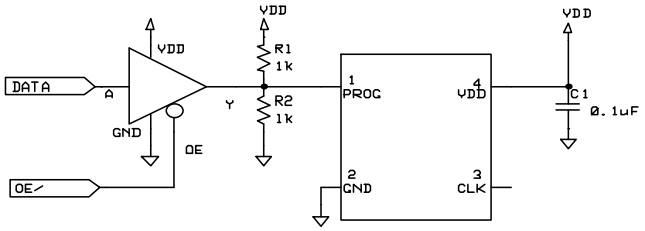

Figure 6. Circuit Diagram for Generating Tri-Level Signal with Tri-State Buffer

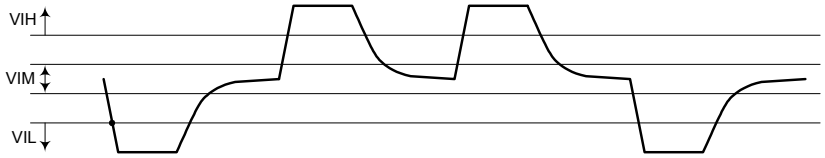

Figure 7. Tri-State Signal Generated with Tri-State Buffer

When using a tri-state buffer as shown above, care must be taken if the DATA and OE lines transition at the same time that there are no glitches. A glitch might occur, for example, if the OE line enables the output slightly before the data line has finished its logical transition. One way around this, albeit at the cost of some data overhead, is to use an extra OE cycle on every bit, as shown in *Figure 8*. Note that the diagram assumes an SN74LVC125, which has a low-true OE/ line (output is enabled when OE/ is low). For a high-true OE part, such as the SN74LVC126, the polarity of that signal would be reversed.

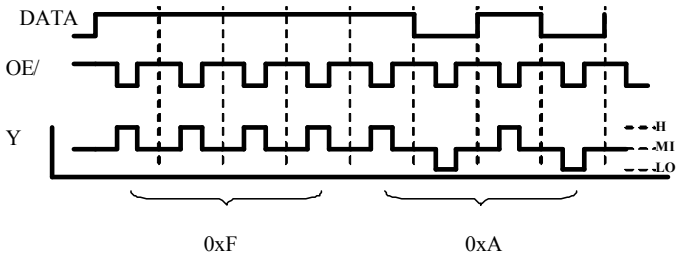

Figure 8. Signal Polarity

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Termination Diagrams

LVPECL:

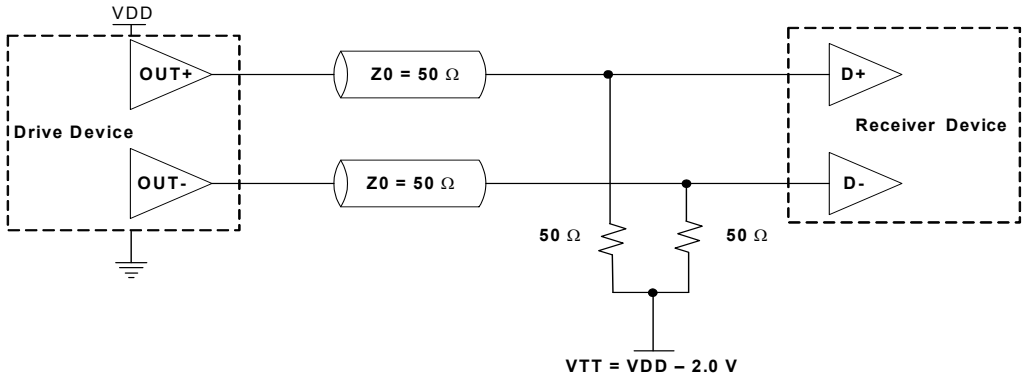

Figure 9. LVPECL Typical Termination

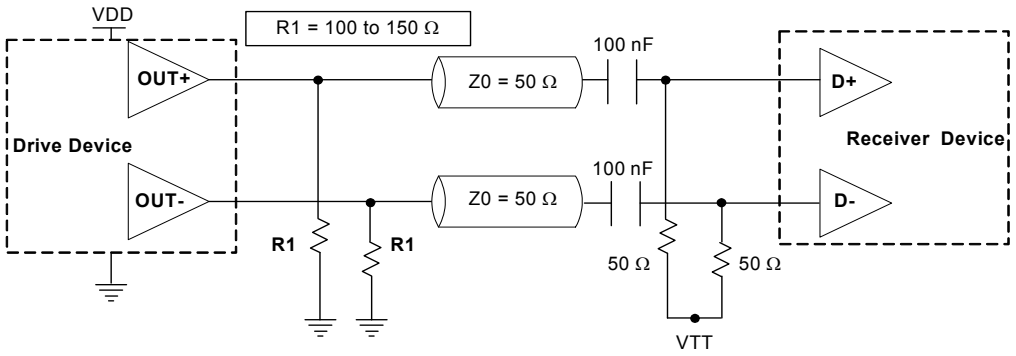

Figure 10. LVPECL AC Coupled Termination

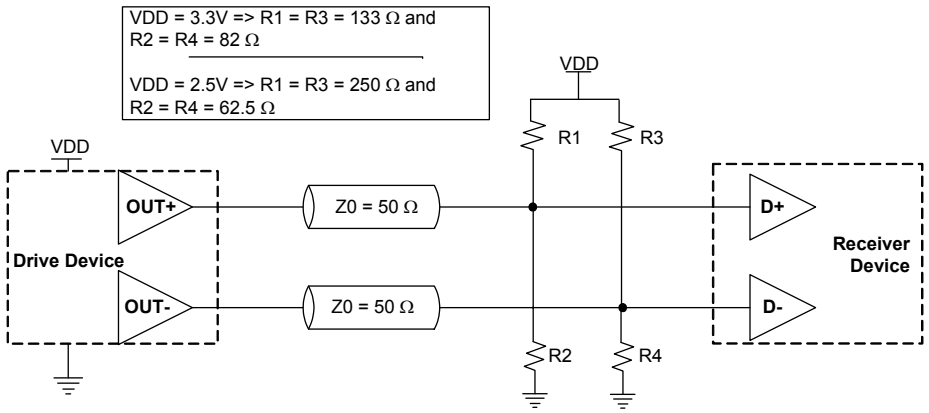

Figure 10. LVPECL with Thevenin Typical Termination

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LVDS:

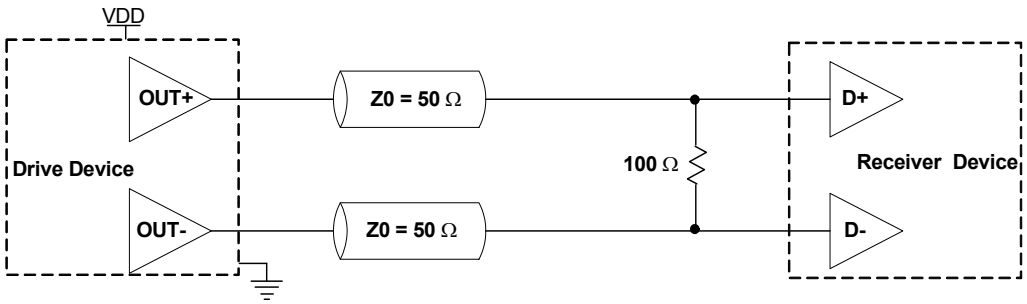

Figure 12. LVDS Single Termination (Load Terminated)

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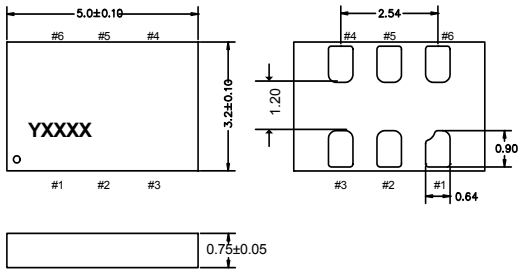
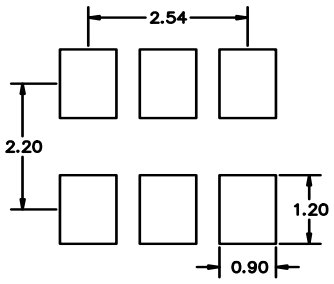
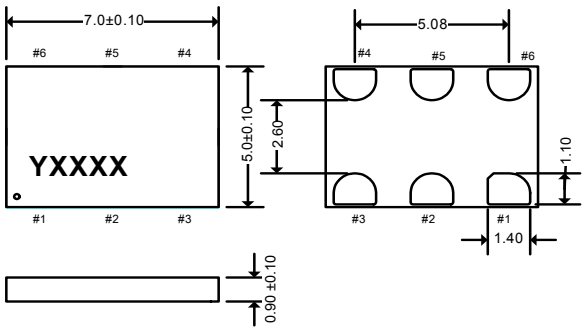
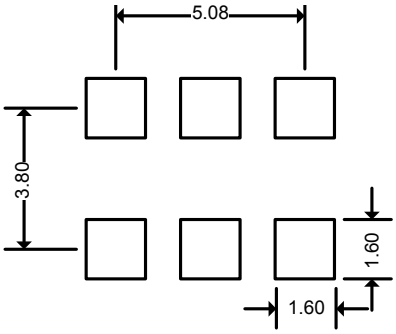
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.

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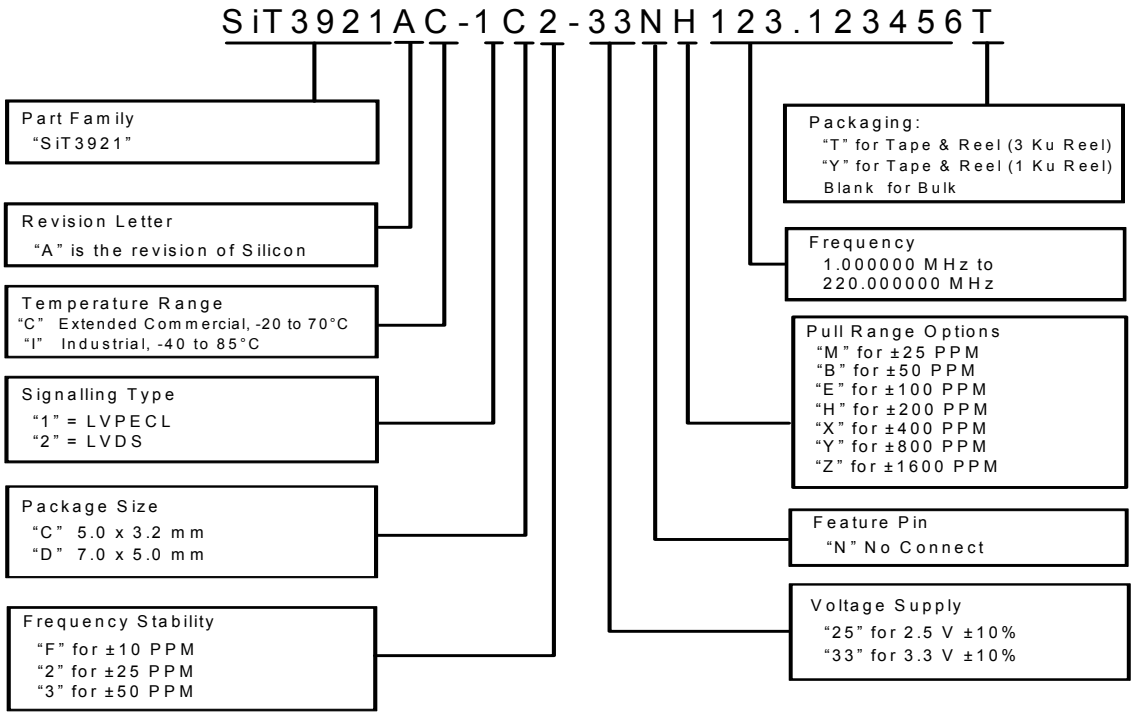
Ordering Information



APR Definition

Absolute pull range (APR) = Norminal pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

APR Table

Nominal Pull Range	Frequency Stability		
	± 10	± 25	±50
	APR (PPM)		
± 25	± 10	—	—
± 50	± 35	± 20	—
± 100	± 85	± 70	± 45
± 200	± 185	± 170	± 145
± 400	± 385	± 370	± 345
± 800	± 785	± 770	± 745
± 1600	± 1585	± 1570	± 1545

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