User's Manual

ISL78444EVAL1Z

User's Manual: Evaluation Board

Automotive

Rev.01.00 Oct 2018

ISL78444EVAL1Z

Evaluation Board

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1. Overview

The ISL78444EVAL1Z evaluation board is designed to provide a quick and comprehensive method for evaluating the ISL78444 100V 3A source, 4A sink half-bridge driver for driving the gates of two NMOS FETs in a half-bridge configuration. Two N-channel MOSFETs are included on the evaluation board to allow for the evaluation of a half-bridge driven load such as a DC motor or a synchronous switching regulator.

The ISL78444 family of FET drivers is offered in a 14 Ld HTSSOP package enhanced with a thermal EPAD. It operates from a supply voltage of 8V to 18V DC with the capability of driving a high-side N-channel FET in a 70V half-bridge configuration. A unique tri-level PWM input allows control of both the high-side and low-side gate drivers with a single input. The mid-level state has both high-side and low-side sink drivers active to disable both MOSFETs. This is beneficial for multiphase DC/DC converters that require phase dropping or to implement asynchronous operation in a synchronous DC/DC converter.

1.1 Key Features

- 3A source and 4A sink NMOS gate drivers
- Internal level shifter and bootstrap switch for gate driver on high-side FET
- Up to 70V high-side gate drive reference
- 8V to 18V bias supply operation
- Single PWM input for high-side and low-side gate driver with tri-level for turning off both drivers
- Single resistor adjustable dead time from 35ns to 400ns

1.2 Specifications

This board is optimized for the following operating conditions:

- V_{DD} supply = 8V to 18V
- V_{BRIDGE} supply input = 12V to 70V
- PWM switching frequency 10kHz to 1MHz
- Preset half-bridge dead time: 165ns with RDT = 10kΩ, (adaptive dead time + programmable dead time)
- Peak gate drive current: 3A source and 4A sink

1.3 Ordering Information

Part Number	Description
ISL78444EVAL1Z	ISL78444EVAL1Z evaluation board

1.4 Related Literature

For a full list of related documents, visit our website:

- ISL78424, ISL78434, ISL78444, ISL78224, ISL78226 product pages

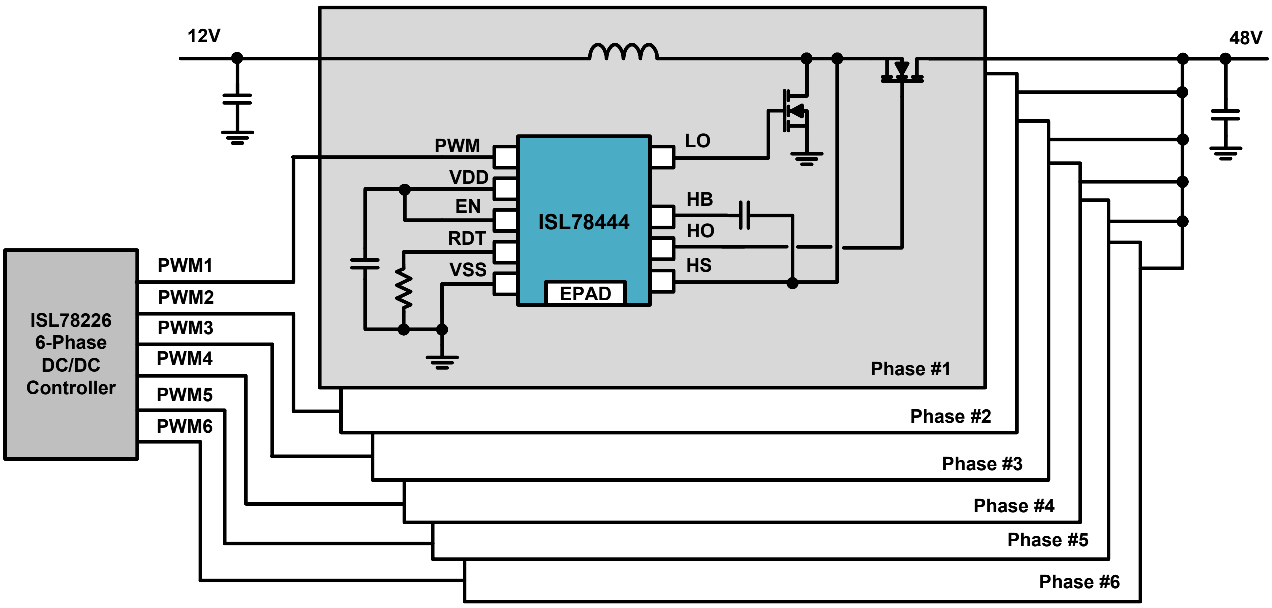

Figure 1. ISL78444 Typical Application Block Diagram

2. Functional Description

The ISL78444EVAL1Z is designed to provide a comprehensive and versatile platform for a user to evaluate the functionality and prototype an application of the ISL78444 FET drivers. This evaluation board provides an open loop type of application for either synchronous buck or boost applications where the output voltage is controlled through the duty cycle of the PWM pin.

2.1 Operating Range

The ISL784x4 FET drivers offer voltage ratings that are ideal for 48V automotive systems. The switching node (HS) can operate at voltages of up to 70V and can tolerate infrequent transient voltages up to 86V. The bootstrap (HB) node (supply to the high-side driver) can operate at voltages up to 86V and can handle infrequent transients up to 100V. The logic pins of the ISL78444 driver are tolerant up to maximum VDD of 18V. The gate drive of the high and low side drivers is provided by VDD.

2.2 Recommended Equipment

(1) 8V to 18V power supply with at least 2A source current capability.

(2) 0V to 70V power supply to bias the half bridge.

(3) 100kHz to 1MHz square wave generator with 0V to 5V logic levels output.

(4) Minimum 4-channel oscilloscope to verify PWM, HO, LO, and HS signals.

(5) Load such as DC motor, or electronic load (optional).

2.3 Quick Start Guide

(1) The programmable dead time of the HO and LO signal is set to 110ns with a 10kΩ resistor from the RDT pin to GND (note the ISL78444 also has an inherent adaptive dead time). To change the dead time, replace the resistor at R_{10} with the value corresponding to the desired dead time. See Figure 1.

(2) Ensure that the enable switch (SW_1) is set to the off position.

(3) Connect a power supply capable of 48V and 10A to VBAT_48V terminals {J_{19}(+) and J_{20}(-)}. Turn on supply to 48V.

(4) Connect 8V to 18V supply to VDD terminals on board {J_2(+) and J_3(-)}. Turn on supply to 12V.

(5) Connect a 0V to 5V (PWM pin capable of voltage up to VDD) <500kHz square wave signal to PWM BNC connector J_{13}.

(6) Toggle enable switch (SW_1) to the on position.

(7) Verify HO and LO outputs are switching. LO switches between GND and VDD (12V for this example) phase inverted from PWM. HO switches between GND and $V_{HB} + V_{BRIDGE}$ (48V in this example) in phase with PWM.

2.4 Dead Time Measurement

(1) Ensure that there is no bandwidth limitation on any of the channels of the oscilloscope and that they are set up to 5V/div.

(2) Connect a probe to the LO signal on J_1 (2-pin header, GND(-)) towards top of board, LO(+) signal towards bottom of board.

(3) Connect a probe to the HO signal on J_6 (2-pin header, GND(-)) towards top of board, HO(+) signal towards bottom of board.

(4) Connect a probe to the HS signal on J_5 (2-pin header, GND(-)) towards left of board, HS(+) signal towards right of board.

(5) Add math measurement to the scope and subtract the HO-HS signals.

(6) Dead time measurement t_{DTHL} = time from 50% level of (HO-HS) signal falling to 50% level of LO signal rising. With R_{DT} = 10kΩ, default configuration of board, the t_{DTHL} = 120ns (adaptive dead time (t_{ADTC}) + resistor programmed dead time (t_{DTHL})).

(7) Dead time measurement t_{DTLH} = time from 50% level of LO signal falling to 50% level of (HO-HS) signal rising. With R_{DT} = 10kΩ, default configuration of board, the t_{DTLH} = 120ns (adaptive dead time (t_{ADTC}) + resistor programmed dead time (t_{DTLH})).

3. PCB Layout Guidelines

For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to ground planes on other PCB layers. For best electrical performance, connect the VSS and AGND pins together through the EPAD to maintain a low impedance connection between the two pins.

When adjustable dead time is used, connect the resistor to the RDT pin and GND plane close to the IC to minimize ground noise from disrupting the timing performance.

Place the VDD decoupling capacitors and bootstrap capacitors close to the VDD-VSS and HB-HS pins, respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance.

(1) Keep power loops as short as possible by paralleling the source and return traces.

(2) Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, add series gate resistors on the bridge FETs to dampen the oscillations.

(3) Large power components (power FETs, electrolytic capacitors, power resistors, etc.) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.

(4) If you simulate your circuits, consider including parasitic components.

3.1 ISL78444EVAL1Z Evaluation Board

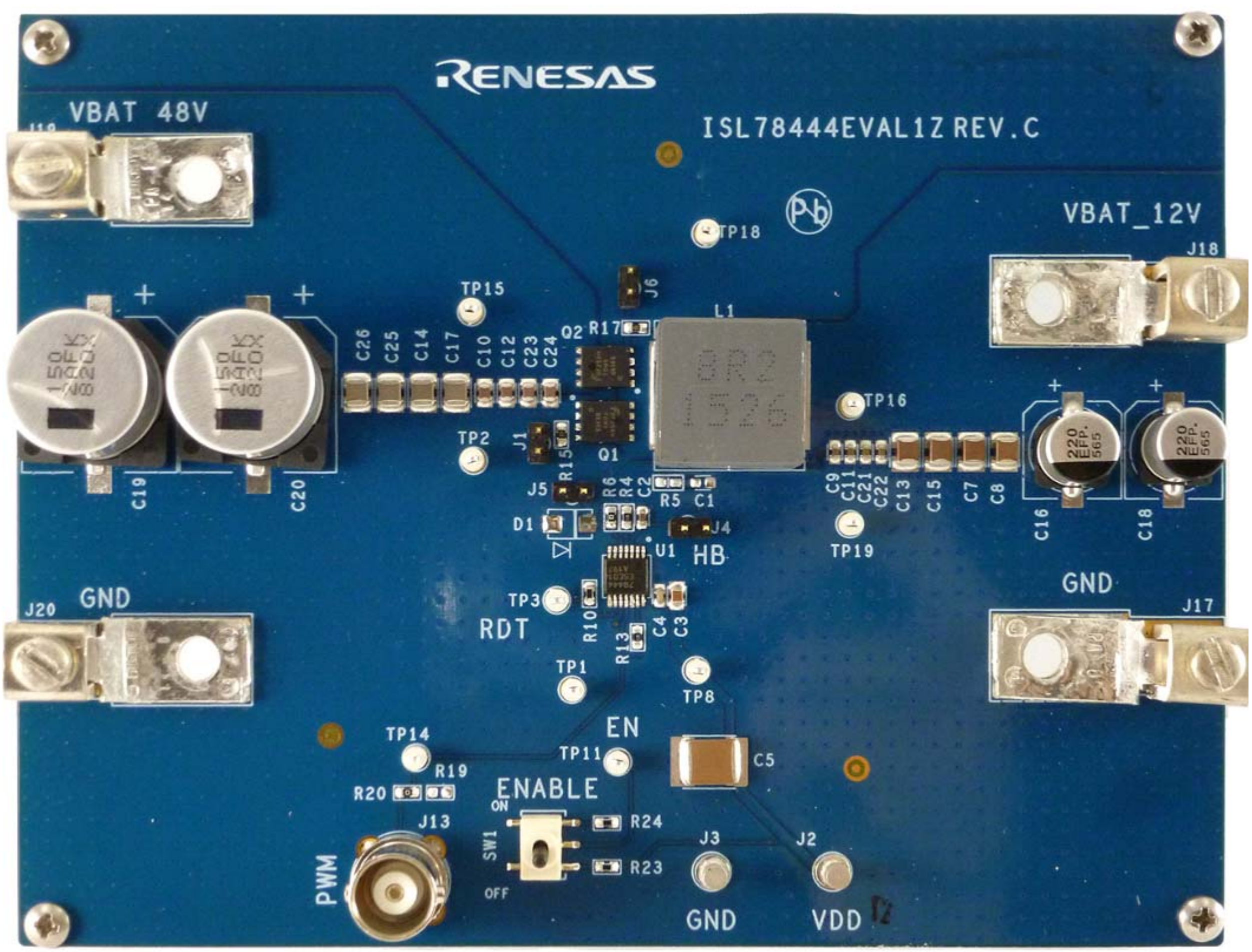

Figure 2. ISL78444EVAL1Z Evaluation Board (Top)

3.2 ISL78444EVAL1Z Circuit Schematic

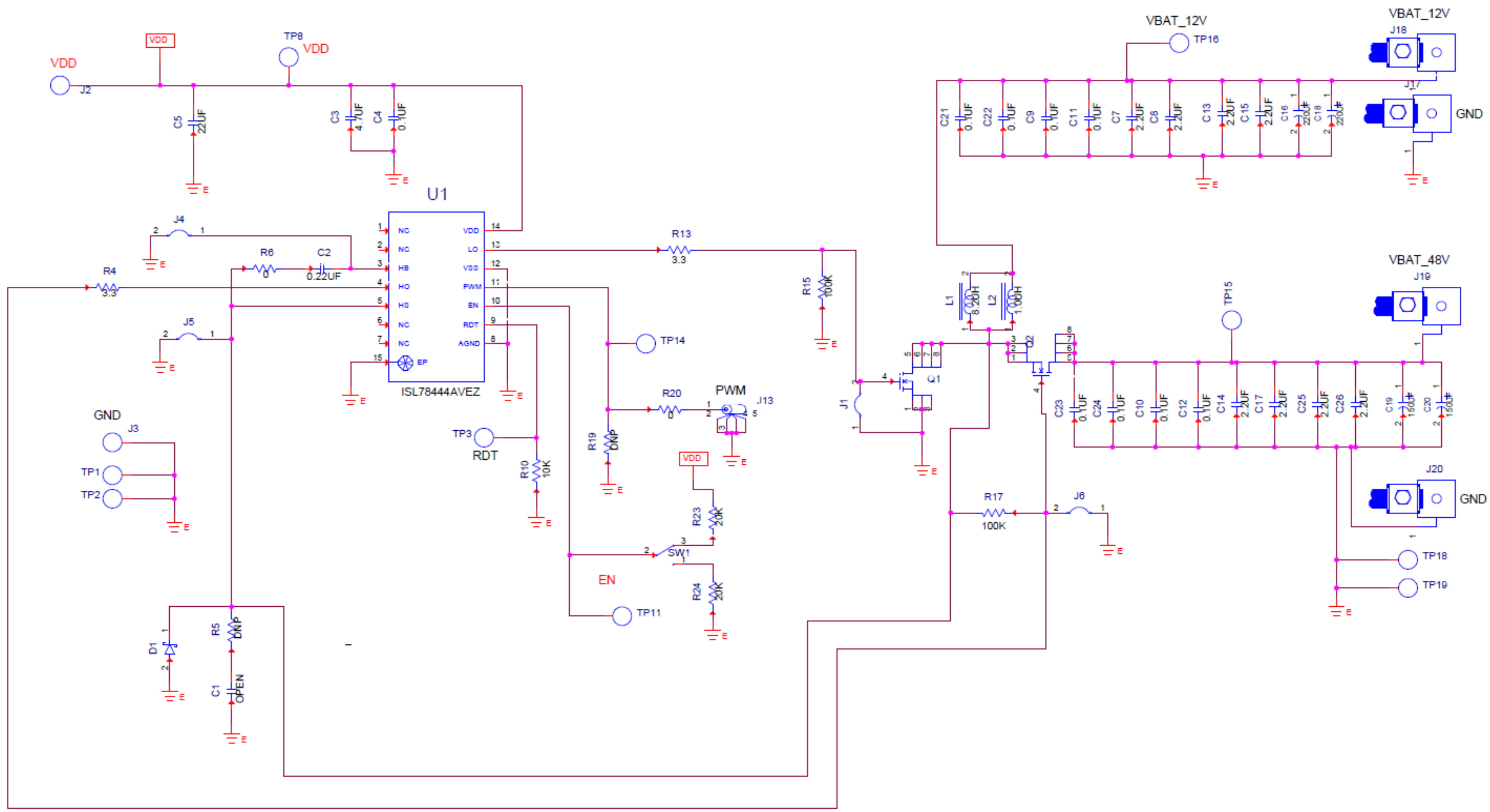

Figure 3. ISL78444EVAL1Z Schematic

3.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	U1	IC-4A, 86V, HALF-BRIDGE DRIVER, 14P, HTSSOP, ROHS	Renesas	ISL78444AVEZ
1	C5	CAPACITOR, SMD, 2220, 22µF, 25V, 20%, X7R, ROHS	TDK	C5750X7R1E226M
1	C3	CAP-AEC-Q200, SMD, 0805, 4.7µF, 35V, 10%, X7R, ROHS	TDK	CGA4J1X7R1V475K125AE
4	C10, C12, C23, C24	CAP-AEC-Q200, SMD, 0805, 0.1µF, 100V, 10%, X7R, ROHS	TDK	CGA4J2X7R2A104K125AA
2	C19, C20	CAP, SMD, 17X17, 150µF, 100V, 20%, ALUM.ELEC., ROHS	Panasonic	EEV-FK2A151M
4	C9, C11, C21, C22	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Yageo	CC0603KRX7R8BB104
1	C4	CAP, SMD, 0603, 0.1µF, 25V, +80 -20%, Y5V, ROHS	Murata	GRM39Y5V104Z025
1	C2	CAP, SMD, 0603, 0.22µF, 50V, 10%, X7R, ROHS	Murata	GCM188R71H224KA64D
4	C14, C17, C25, C26	CAP, SMD, 1210, 2.2µF, 100V, 10%, X7R, ROHS	Murata	GRM32ER72A225KA35L
4	C7, C8, C13, C15	CAP, SMD, 1210, 2.2µF, 50V, 10%, X7R, ROHS	TDK	C3225X7R1H225K
2	C16, C18	CAP, SMD, 8x10.2mm, 220µF, 20%, 25V, 80mΩ, ALUM.ELEC., ROHS	Panasonic	EEE-FP1E221AP
4	L1	COIL-INDUCTOR, AEC-Q200, SMD, 16.9x16.9, 8.2µH, 20%, 18A, ROHS	Bourns	SRP1770TA-8R2M
2	Q1, Q2	TRANSISTOR-MOS, N-CHANNEL, 8P, PWR56, 80V, 80A, ROHS	Fairchild	FDMS86368_F085
3	R6, R20	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
1	R10	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
2	R15, R17	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1003FT
2	R23, R24	RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2002FT
4	R4, R13	RES, SMD, 0603, 3.3Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3RQF3R3V
1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 3POS, ON-OFF-ON, ROHS	ITT Industries/ C&K Division	GT13MSCBE
2	J2, J3	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
2	J9, J13	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
10	TP1-3, TP8, TP11, TP14-TP16, TP18, TP19	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
4	J1, J4-J6	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	Berg/FCI	68000-236HLF
	D1, R5, R16, R19, C1	DNP		

3.4 Board Layout

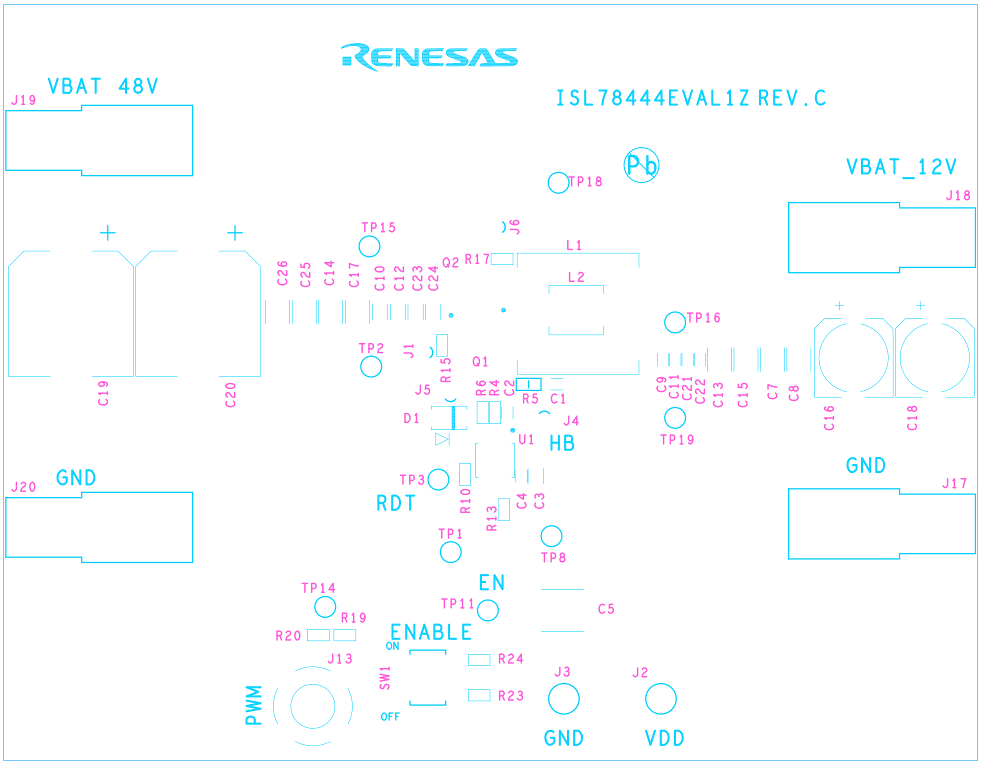

Figure 4. Silkscreen Top Layer

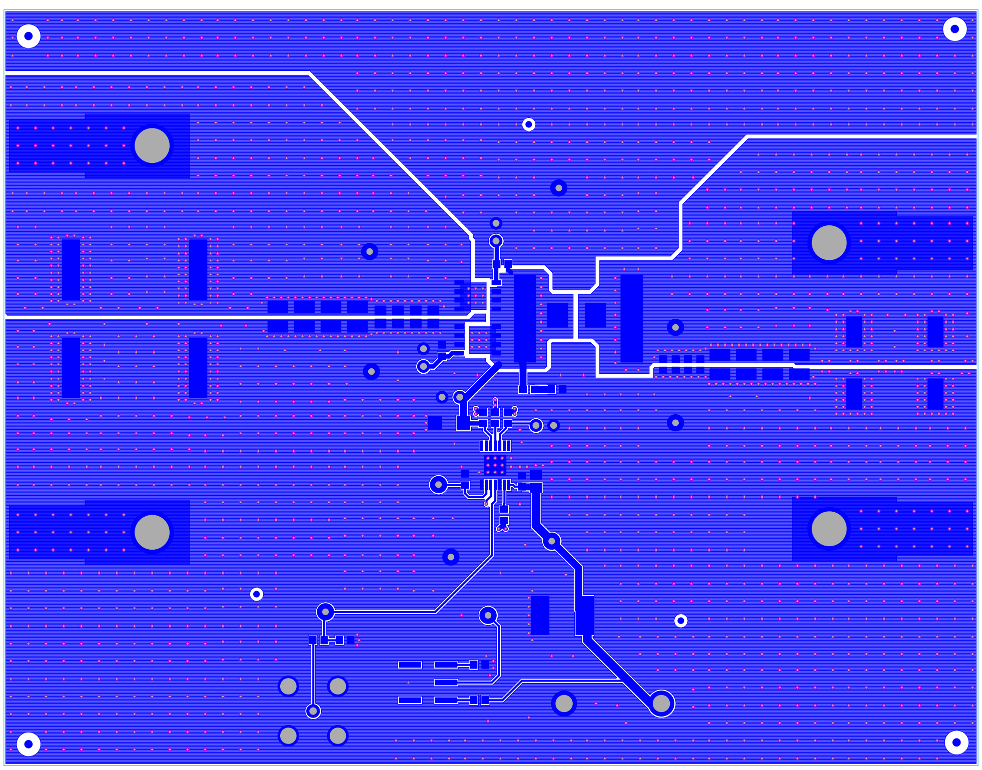

Figure 5. Layer 1

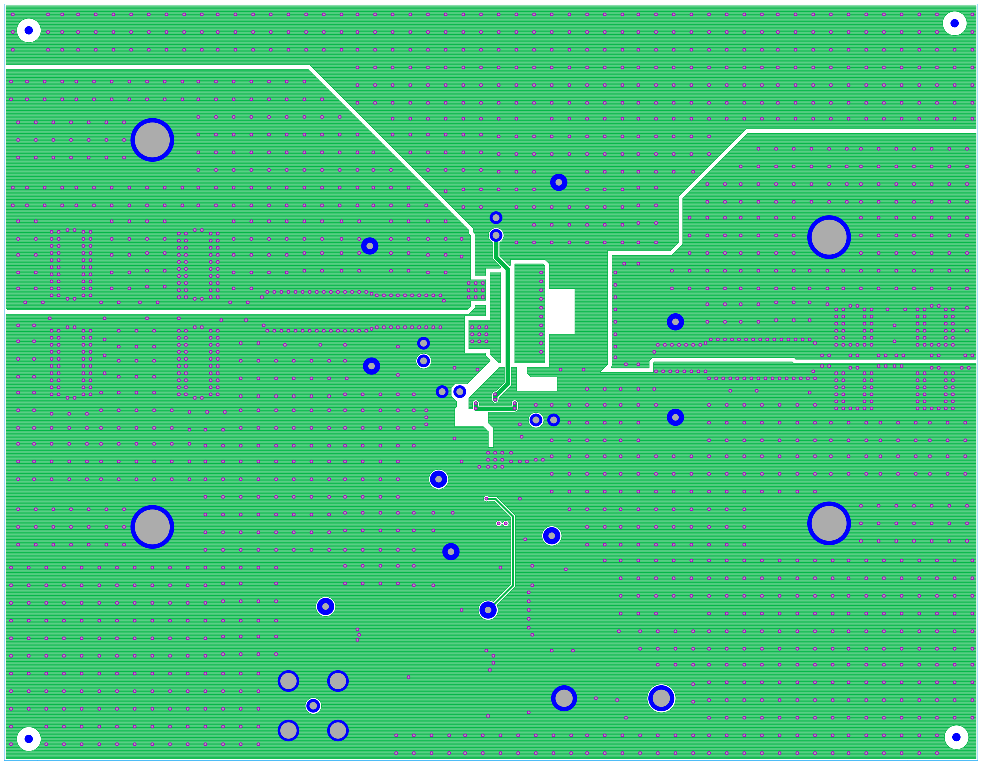

Figure 6. Layer 2

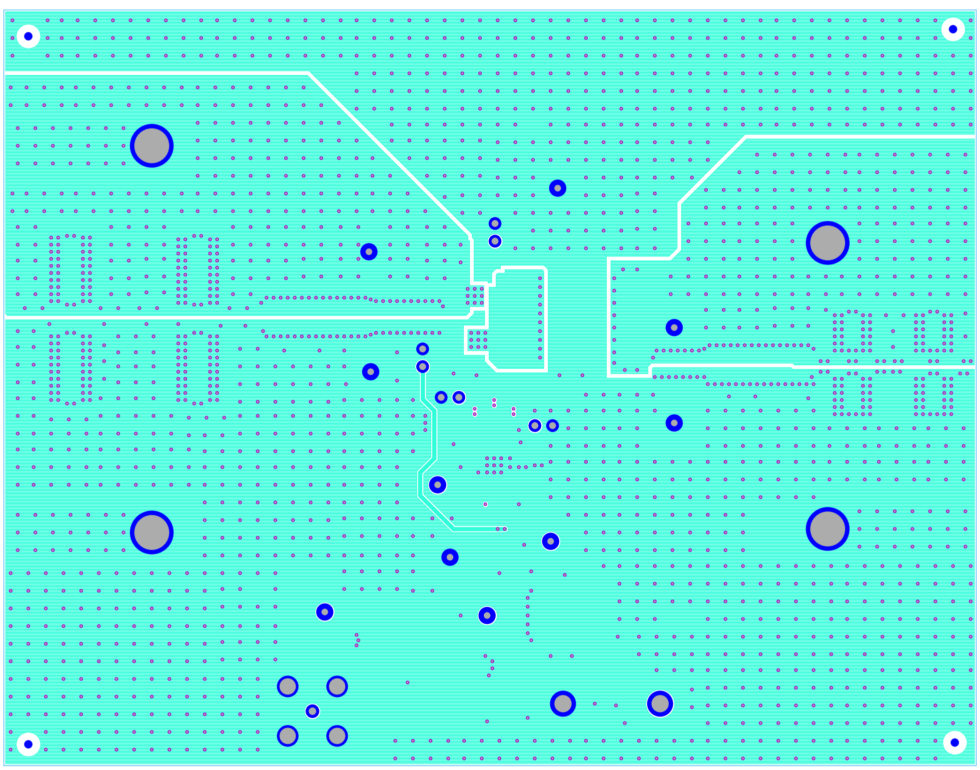

Figure 7. Layer 3

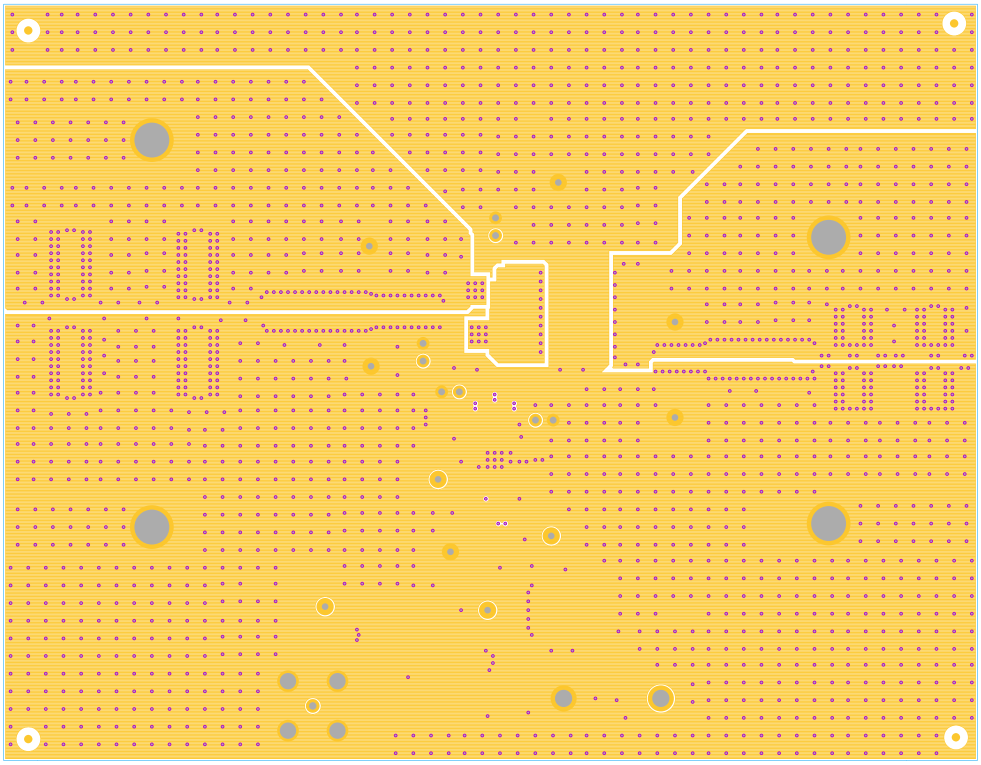

Figure 8. Layer 4

4. Typical Performance Curves

Unless noted: V_{DD} = 12V, V_{BRIDGE} = 48V, PWM = 100kHz square wave, 0V to 5V, 25% duty cycle, T_A = +25°C

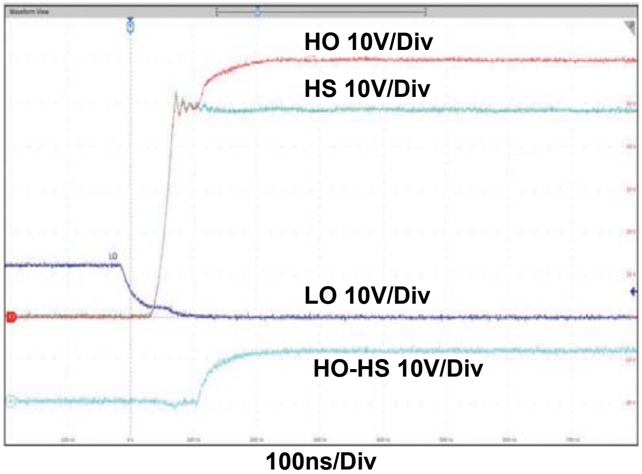

Figure 9. Dead Time LO Falling to HO Rising

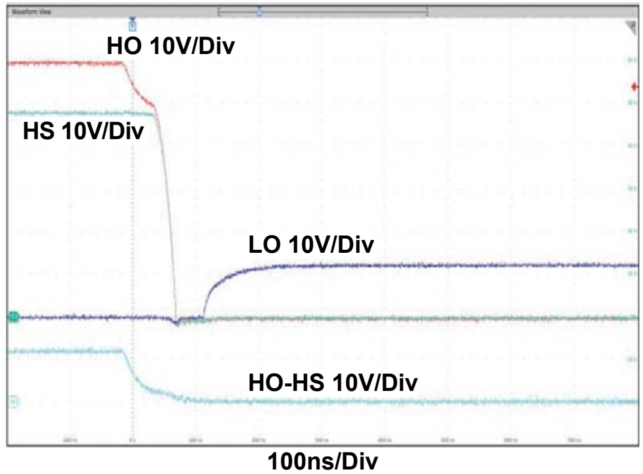

Figure 10. Dead Time HO Falling to LO Rising

5. Revision History

Rev.	Date	Description
01.00	October 23, 2018	Initial release

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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Colophon 7.2

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