

Si5341-D EVALUATION BOARD USER'S GUIDE

Description

The Si5341-D-EVB is used for evaluating the Si5341 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5341-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB Features

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5341 or up to 3 input clocks for synchronous clocking.
- Feedback clock input for optional zero delay mode.
- ClockBuilder[®] Pro (CBPro) GUI programmable V_{DD} supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable V_{DDO} supplies allow each of the 10 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of V_{DD} and all V_{DDO} supplies.
- Status LEDs for power supplies and control/status signals of Si5341.
- SMA connectors for input and output clocks.



Figure 1. Si5341-D Evaluation Board

1. Functional Block Diagram

Below is a functional block diagram of the Si5341-D-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See section "3. Quick Start" or section "8. Installing ClockBuilder Pro Desktop Software" for more information.

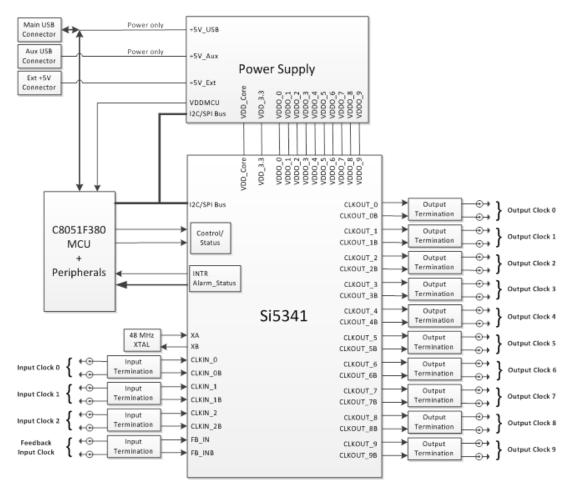


Figure 2. Si5341-D-EB Functional Block Diagram

2. Si5341-D-EVB Support Documentation and ClockBuilder Pro Software

All Si5341-D-EVB schematics, BOMs, User's Guides, and software can be found online at the following link: www.skyworksinc.com/support-ia

3. Quick Start

- 1. Install ClockBuilder Pro desktop software from www.skyworksinc.com/en/application-pages/clockbuilderpro-software.
- 2. Connect a USB cable from Si5341-D-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 1.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5341-D-EB.
- 6. For the Si5341 data sheet, go to www.skyworksinc.com/en/Products/Timing.

Si5341-D-EVB

4. Jumper Defaults

Location	Туре	l = Installed 0 = Open		Location	Туре	l = Installed 0 = Open
JP1	2 pin	0		JP23	2 pin	0
JP2	2 pin	I		JP24	2 pin	0
JP3	2 pin	0		JP25	2 pin	0
JP4	2 pin	I		JP26	2 pin	0
JP5	2 pin	I		JP27	2 pin	0
JP6	2 pin	I		JP28	2 pin	0
JP7	2 pin	I		JP29	2 pin	0
JP8	2 pin	I		JP30	2 pin	0
JP9	2 pin	0		JP31	2 pin	0
JP10	2 pin	I		JP32	2 pin	0
JP13	2 pin	0		JP33	2 pin	0
JP14	2 pin	I		JP34	2 pin	0
JP15	3 pin	1 to 2		JP35	2 pin	0
JP16	3 pin	1 to 2		JP36	2 pin	0
JP17	2 pin	0		JP38	3 pin	All Open
JP18	2 pin	0		JP39	2 pin	0
JP19	2 pin	0		JP40	2 pin	0
JP20	2 pin	0		JP41	2 pin	0
JP21	2 pin	0		J36	5 x 2 Hdr	All 5 installed
JP22	2 pin	0				
*Note: Refer to	the Si5341	-D-EB schematics for	the	functionality ass	ociated with ea	ich jumper.

Table 1. Si5341-D-EB Jumper Defaults

4 Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com Rev. 1.0 • Skyworks Proprietary Information • Products and Product Information are Subject to Change Without Notice • December 2, 2021

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

Table 2. Si5341-D-EB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5341 +3.3 V, and Si5341 V_{DD} supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

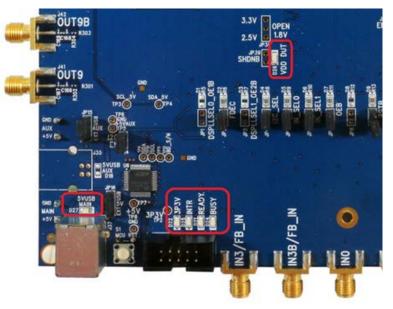


Figure 3. Status LEDs

6. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5341-D-EB has eight SMA connectors (IN0/IN0B–IN2/IN3B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5341 data sheet.

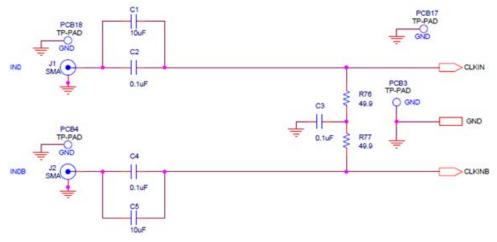


Figure 4. Input Clock Termination Circuit

7. Clock Output Circuits (OUTx/OUTxB)

Each of the twenty output drivers (10 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5341-D-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5341-D-EB and provide locations on the PCB for optional dc/ac terminations by the end user.

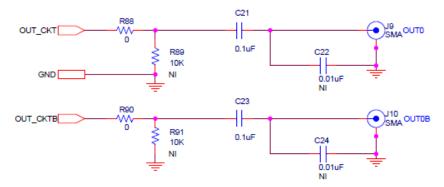


Figure 5. Output Clock Termination Circuit

8. Installing ClockBuilder Pro Desktop Software

To install the CBOPro software on any Windows 7 (or above) PC:

Go to www.skyworksinc.com/en/application-pages/clockbuilder-pro-software and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Please follow the instructions as indicated.

9. Using the Si5341-D-EVB

9.1. Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the evaluation board with a USB cable as shown below.

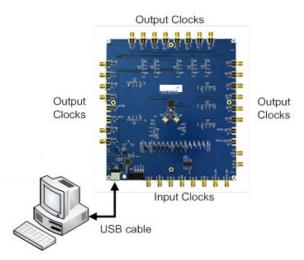


Figure 6. EVB Connection Diagram

9.2. Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5341-D-EB schematic for details.

The Si5341-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

Figure 7 shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

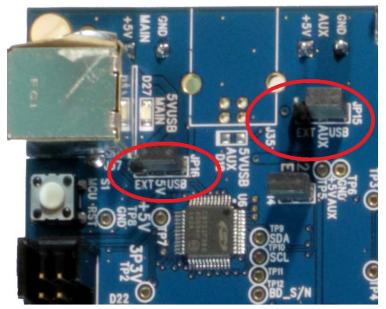


Figure 7. JP15-JP16 Standard Jumper Shunt Installation

Errata Note:Some early versions of the 64-pin Si534x-EBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the right hand side as read and viewed in Figure 7.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, reconfigure the EB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
 - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
 - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

9.3. Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install **two** main applications:

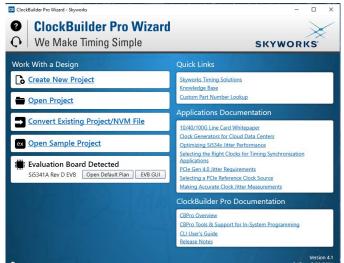


Figure 8. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

fo DUT SPI DUT	IT Settings Editor DUT F	Register Editor Re	gulators All Vol	tages GPIC) Status Registers	+ Control Registers
		Voltage	Current	Power		Soft Reset and Cal
VDD 1	1.80V	v	A	W	Read	SOFT_RST
VDDA 3	3.30V	v	A	w	Read	Hard Reset, Sync. & Pi
VDDO0	1.80V 🔽 💽	1.804 V	0 mA	0 mW	Bead	HARD_RST
VDDO1 1	1.80V 🔽 On	1.788 V	0 mA	0 mW	Read	SYNC
	1.80V 🖬 On	1.796 V	0 mA	0 mW	Read	PDN: 0
	1.80V 🔽 On	1.799 V	0 mA	0 mW	Read	
	1.80V 🖬 On	1.804 V	0 mA	0 mW		Frequency Ad
					Read	FINC
_	1.80V 💽 On	1.795 V	0 mA	0 mW	Read	FDEC
VDDO6 1	1.80V 📘 On	1.786 V	0 mA	0 mW	Read	
VDDO7 1	1.80V 📱 On	1.801 V	0 mA	0 mW	Read	
VDDO8 1	1.80V 📱 💽	1.791 V	0 mA	0 mW	Read	
VDDO9 1	1.80V 📱 On	1.796 V	0 mA	0 mW	Read	
						_
ltered 📘 Auto		t Marker Ch	ar Copy to	Clipboard	Pause	
tered 💽 Auto nestamp Source	e Message			Clipboard		
Itered Auto mestamp Source :32:31.363 EVB	e Message Pausing 70 msec	for voltage MUX I	old	Clipboard		
tered Auto mestamp Source 32:31.363 EVB 32:31.442 EVB	Pausing 70 msec Starting Read_AD	for voltage MUX F	old 0)	Clipboard		•
Auto nestamp Source 32:31.363 EVB :32:31.442 EVB :32:31.452 EVB	Pausing 70 msec Starting Read_AD Finished Read_AD	for voltage MUX H C(num_samples= C(num_samples=	old 0) 10) => 380.2			*
Auto nestamp Source 32:31.363 EVB :32:31.442 EVB :32:31.452 EVB :32:31.452 EVB	Pausing 70 msec Starting Read_AD Finished Read_AD Finished Measure	for voltage MUX I C(num_samples=)C(num_samples= v_Voltage(channel=	old 0) 10) => 380.2 :VDD_8_PIN) =>			•
tered Auto mestamp Source 32:31.363 EV8 32:31.442 EV8 32:31.452 EV8	Pausing 70 msec Starting Read_AD Finished Read_AD Finished Measure Starting Read_DU	for voltage MUX H C(num_samples= C(num_samples=	old 0) 10) => 380.2 :VDD_8_PIN) => x090E)			•

Figure 9. Application #2: EVB GUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5341)
- Control the EVB's regulators
- Monitor voltage, current, power on the EVB

9.4. Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5341-D-EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Skyworks-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

9.5. Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows. Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking on this icon on your PC's desktop.



Figure 10. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

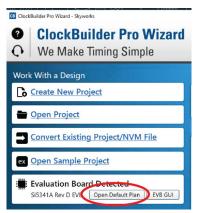


Figure 11. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

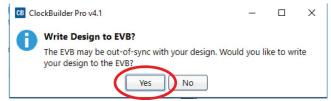
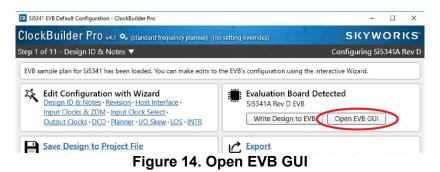


Figure 12. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5341 device mounted on your EVB. This ensures the device is completely reconfigured per the Skyworks default plan for the DUT type mounted on the EVB.

Writing Si5341 Design	to EVB
Address 0x026D	
Figure	e 13. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.



The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Skyworks, as shown below.

Si5	341A Rev D I	EVB - ClockBuilder Pro)					
e H	lelp				-			
nfo	DUT SPI	DUT Settings Editor	DUT Register Edi	tor Regulators	All Voltages	GPIO	Status Regis	ters
			Volta	ge Currer	nt Power	r		
	VDD	0 1.80V 📳	On	- v	A N	N [Read	
	VDD/	A 3.30V	On	- v	A N	N [Read	
	VDDO	0 2.50V 📱	On 1.804	4 V 0	mA 0ı	mW 🗌	Read	
	VDDO.	1 2.50V 🔽	On 1.78	3 V 0	mA 0ı	mW 🗌	Read	
	VDDO	2 2.50V 🔽	On 1.79	5 V 0	mA 0ı	mW 🗌	Read	
	VDDO3	3 2.50V 🔽	On 1.799	9 V 0	mA 0ı	mW 🗌	Read	
	VDDO4	4 2.50V 🔽	On 1.804	4 V 0	mA 0ı	mW 🗌	Read	
	VDDO:	5 2.50V 🔽	On 1.79	5 V 0	mA 0ı	mW 🗌	Read	
	VDDO	5 2.50V 🔽	On 1.78	5 V 0	mA 0ı	mW 🗌	Read	
	VDDO	7 2.50V 🔽	On 1.80	I V 0	mA 0ı	mW 🗌	Read	
	VDDO	3 2.50V 🔽	On 1.79	I V 0	mA 0ı	mW 🗌	Read	
	VDDO	9 2.50V 🔽	On 1.79	5 V 0	mA 0ı	mW 🗌	Read	
All	Output [– Select Voltage	То	tal 0	mA 0	w	Read All	
5	Supplies _	- Power On Po	ower Off	Compare Desig	in Estimates to	Measur	ements	

Figure 15. EVB GUI Window

9.5.1. Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

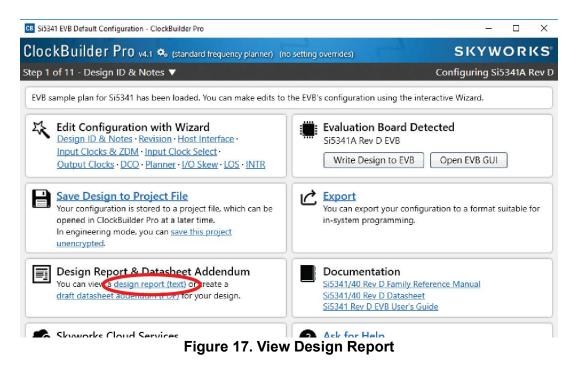
You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Skyworks-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":



Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.



Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

B Si5341 Design Repo	m		_)
Design Report					
** Engineering P	lode Design Repo	rt **			
Overview					
Part:	Si5341A Rev	D			
Design ID:	5341EVB2				
Created By:		r Pro v4.1 [2021-09-22]			
Timestamp:	2021-11-12	11:36:01 GMT-05:00			
Design Rule Chec					
Errors:	-				
- No errors					
Warnings:					
- No warnings					
Device Grade					
Maximum Output F					
Frequency Synthe		ional			
Frequency Plan G Minimum Base OPM		14*			
Base Outpu	ut Clock	Supported Frequency Synthesis Modes			
OPN Grade Frequ	ency Range	(Typical Jitter)			
S15341A* 100 H	to 1.028 GHz	Integer (< 100 fs) and fractional (< 150 fs)			
	iz to 350 MHz	" Tabaara aala (c. 200 fa)			
S153410 100 F		Integer only (< 100 fs)			
* Based on your	calculated free	uency plan, a Si5341A grade device is			
required for you	ur design. See t	he datasheet Ordering Guide for more			
information.	0				
Design					
Host Interface:	oply: VDD (Core)				
SPI Mode: 4-W					
		19d / 0x74 to 0x77 (selected via A0/A1 pins)			
Inputs:					
VAYE 16 MHz					
Crystal IN0: Unused	mode				
IN1: Unused					
IN2: Unused					
FB_IN: Unused					
Outputs:					
5070. 161.132 Fashlas					
OUT1: 672.164	1, LVDS 2.5 V				
	i, LVDS 2.5 V				
OUT2: 168.041					
Enabled	i, LVDS 2.5 V				
Copy to Clipboard	Save Repo	t Ask for Help		Clo	se

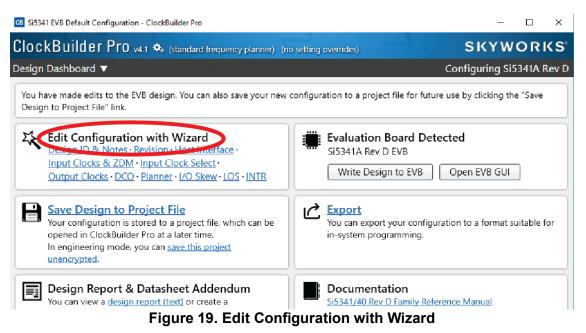
Figure 18. Design Report Window

9.5.2. Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

9.6. Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

	er Pro v4.1 🍫 (standard frequency planner) (no setting overrides)	SKYWOR
<u>ep 1 of 11 - De</u>	esign ID & Notes	Configuring Si5341A
Design ID The device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/r	evision identifier.
Design ID:	5341EVB2 (optional; max 8 characters)	
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN	ID7.
Padding Mode:	WILL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pad character).	ded with 0x00 bytes (aka NULL
	 Space Padded ff you do not enter the full 8 characters, the remaining bytes of DESIGN_JDx will be pad character). 	ded with 0x20 bytes (space
Design Notes		
Enter anything you	u want here. The text is stored in your project file and included in design reports and custom p ord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet addendu
Enter anything you		art number datasheet addendu
Enter anything you		art number datasheet addendu
Enter anything you		art number datasheet addendu
Enter anything you		art number datasheet addendu
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Figure 20. Design Wizard

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

Writing Si5341 Design to EVB						
Address 0x026D						

Figure 21. Writing Design Status

9.7. Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

CB ClockBuilder Pro Wizard - Skyworks	- 🗆 X
ClockBuilder Pro WizardQWe Make Timing Simple	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
🖶 Open Project	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation 10/40/100G Line Card Whitepaper
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance
Si5341A Rev D EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements
	ClockBuilder Pro Documentation
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes
¢,	Version 4.1 Built on 9/22/2021

Figure 22. Open Design Project File

Si5341-D-EVB

CB Open CBPro Project File X ↑ _ « Jui_Tharwal → User_Guide_Images_Rebranding → Si5341 v ひ Search Si5341 p New folder 822 -2 Organize 🔻 Date modified Size Nam Type A Quick access Bi5341-RevD-5341EVB2-Project 11/12/2021 11:39 ... Skyworks Timing ... 10 KB Desktop Documents Downloads Pictures _2 E:\ COGSWORTH_FW-{ Keysight_250ct21 Si5340 Si5341 This PC

Locate your CBPro design file.design file in the Windows file browser.

Figure 23. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:

CB Clo	ockBuilder Pro v4.1	-		×
A	Write Design to EVB?			
	The EVB may be out-of-sync with your design. Woul your design to the EVB?	d you li	ke to wr	ite

Figure 24. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

9.8. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

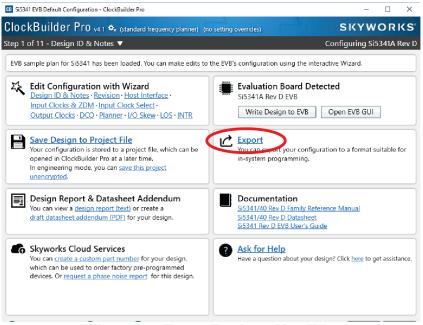


Figure 25. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

CB Si5341 Export			
Register File	Settings File	Multi-Project Register/Settings	
This expor your desig address is data fields Please refe and how to	n/configuratio two-bytes wid er to the Si538	he registers that need to be written to t n. Each line in the file is an address, data de and the data is a single byte. A com 8x/4x Family Reference Manual for infoi a contained within this export. Note the f ornifiguration.	pair in hexadecimal format. The ma separates the address and rmation on register addressing
If check header about t Include Certain registe normal	will be prefixe the design, too pre- and post control registers. This ensures operation after host system is	der stional header will be included at the top d by the # character. The header will con 1, and a timestamp. write control register writes ers must be written before and after writi the device is stable during configuration rt the download is complete. You can tur managing this process already. rour selection is not saved to prefs)	tain some basic information ing the volatile configuration n download and resumes
		Preview Export Save to File	

Figure 26. Export Settings

10. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5341 using Clock-Builder Pro on the Si5341-D-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5341 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

11. Si5341-D-EVB Schematic and Bill of Materials (BOM)

The Si5341-D-EVB Schematic and Bill of Materials (BOM) can be found online at

www.skyworksinc.com/support-ia

Please be aware that the Si5341-D-EB schematic is in **OrCad Capture** *hierarchical format* and not in a typical "flat" schematic format.

SKYWORKS

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro



C

Portfolio www.skyworksinc.com/ia/timing

www.skyworksinc.com/CBPro



Quality www.skyworksinc.com/quality



Support & Resources www.skyworksinc.com/support

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