BROADCOM®

Data Sheet

APDS-9160-003

Digital Proximity and ALS Sensor in Small Aperture

Description

The Broadcom® APDS-9160-003 is an integrated ALS and proximity detector with IR LED in an optical module.

The APDS-9160 provides digital ALS and IR sensing, an IR LED, and a complete proximity sensing (PS) system in a single 8-pin package that is suitable to be used under a small aperture of the devices' cover windows. The proximity detection feature operates well from bright sunlight to dark rooms. The APDS-9160 is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions.

The APDS-9160 has a wide dynamic range. Current is programmable in 8 different steps. The number of LED pulses can be configured by using the pulse step, and the LED modulation frequency can be set from 60 kHz to 100 kHz in 5 steps. PS resolution can be varied from 8 bits to 11 bits, and the measurement rate is from 6.25 ms to 400 ms. To offset unwanted reflected light from the cover glass, a PS intelligent cancellation level register allows for an on-chip subtraction of the ADC count caused by the unwanted reflected light from PS ADC output.

Both the PS and ALS function independently allowing for maximum flexibility in application.

Applications

- Cell phone backlight control
- Cell phone touch-screen disable
- Automatic Speakerphone enable
- Digital camera eye sensor

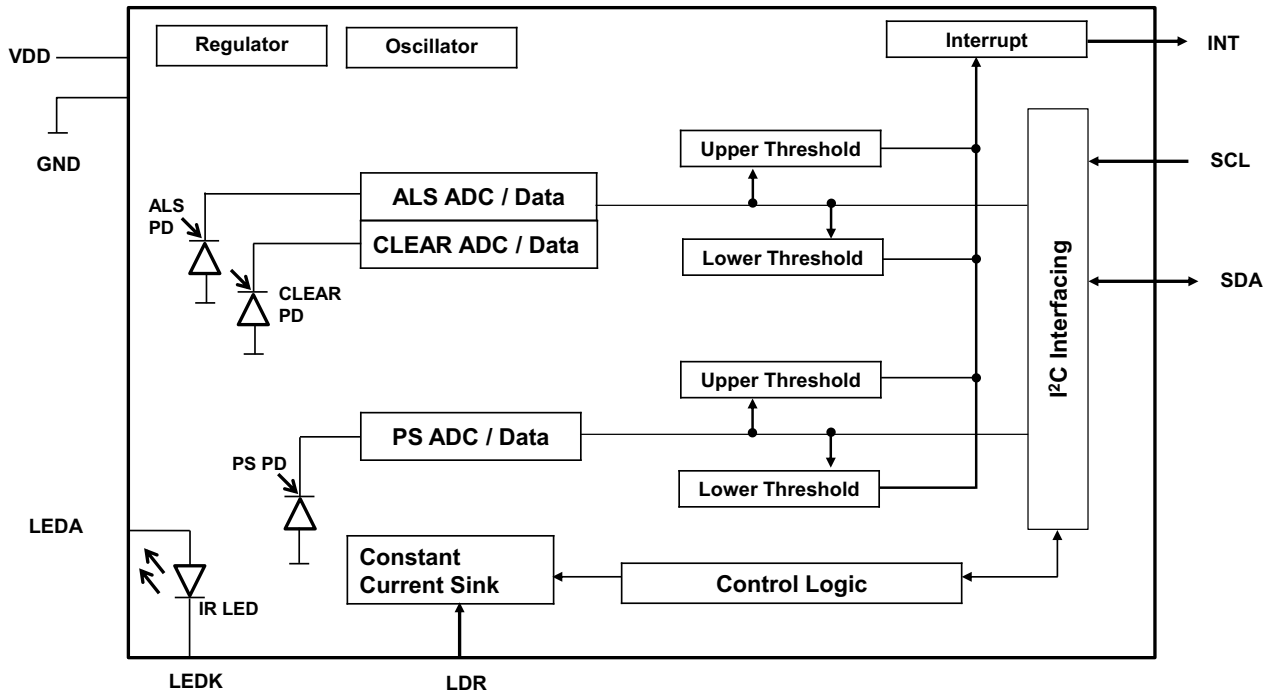
Features

- Ambient Light Sensing (ALS)
  - Light output proportional to light intensity
  - Uses optical coating technology to emulate human eye spectral response
  - Works well under different light source conditions
  - High sensitivity in low lux condition. Ideally suited for operations behind darkened glass
  - 50 Hz/60 Hz light flicker immunity
  - Fluorescent light flicker immunity
  - Programmable interrupt function with upper, lower thresholds and persists function
  - Programmable LS integration time
  - Programmable LS gain setting
  - Up to 20-bit resolution
- Proximity detection (PS)
  - 100K lux sunlight suppression
  - Up to 11-bit resolution
  - Programmable interrupt function with upper and lower thresholds and persists function
  - Programmable gain setting
- Supply voltage 1.7V to 3.6V
- Power management
  - Low active current
  - Low standby current
- I^2C interface compatible
  - Up to 400 kHz (I^2C fast-mode)
- Small package L 2.55 mm × W 2.05 mm × H 1.00mm

Ordering Information

Part Number	Packaging	Quantity
APDS-9160-003	Tape and Reel	10,000 per reel

Functional Block Diagram



I/O Pins Configuration

Pin	Name	Type	Description
1	GND	Ground	Power supply ground. All voltages are referenced to GND
2	INT	O	Interrupt. Open drain
3	LDR	I	LED driver for proximity emitter – up to 125 mA, open drain
4	LEDK	O	LED cathode, connect to LDR pin in most systems to use internal LED driver circuit
5	LEDA	I	LED supply voltage
6	VDD	Supply	Power supply voltage
7	SDA	I/O	Serial data I/O for I^2C
8	SCL	I	I^2C serial clock input terminal. Clock signal for I^2C serial data

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Conditions
Power Supply Voltage[a]	V_{DD}	—	3.63	V	
Digital Voltage Range		–0.5	3.63	V	
Storage Temperature Range	Tstg	–40	100	°C	

a. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Ambient Temperature	T_A	–40	—	85	°C
Supply Voltage	V_{DD}	1.7	—	3.6	V
LED Supply Voltage	V_{LED}	2.5	—	4.6	V

Operating Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
SCL, SDA Input High Voltage	V_{IH}	1.5	—	V_{DD}	V	
SCL, SDA Input Low Voltage	V_{IL}	0	—	0.4	V	
INT, SDA Output Low voltage	V_{OL}	0	—	0.4	V	
Leakage Current, SDA, SCL, INT Pins	I_{LEAK}	–5	—	5	µA	

ALS Characteristics

V_{DD} = 2.8 V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current (ALS only)	I_{DD_ALS}	—	50	70	µA	Active mode
		—	1	2	µA	Standby mode
Peak Wavelength	λ_P	—	550	—	nm	
Min Integration Time	$T_{intmin1}$	—	3.125	—	ms	
	$T_{intmin2}$	—	50	—	ms	With 50/60 Hz rejection
Max Integration Time	T_{intmax}	—	400	—	ms	With 50/60 Hz rejection
Output Resolution	RES_{ALS}	13	18	20	bit	Programmable
ADC Count Value		800	1000	1200	counts	λ = 525 nm, 50 ms, Gain=3×, Ee=72 µW/cm^2
Dark Count Value		0	—	3	counts	Gain = 64×, 50 ms, Ee = 0

IR LED Characteristics

T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Wavelength	λ_P	—	940	—	nm	I_F = 20 mA
Spectrum Width, Half Power	$\Delta\lambda$	—	50	—	nm	I_F = 20 mA
Optical Rise Time	T_R	—	20	—	ns	I_F = 100 mA
Optical Fall Time	T_F	—	20	—	ns	I_F = 100 mA

PS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Min.	Typ.	Max.	Units	Test Conditions
Supply Current (wthout LED Current)	—	99	—	µA	Active mode, 32 pulse, 60 kHz, 150 mA, Gain = 1x, 100-ms wait time
Supply Current (PS + LED only)	—	499	—	µA	Active mode, V_{LED} = 3V, 32 pulse, 60 kHz, 150 mA, Gain = 1x, 100-ms wait time
Full Scale ADC Count Value	—	—	2047	counts	11 bit
PS Resolution	8	—	11	bit	
IR LED Pulse Count	1	—	255	pulses	
Proximity LED Drive	10	—	200	mA	Sink current at 600 mV, LDR Pin
Frequency of PS LED Pulses (Programmable)	60	—	100	kHz	
Duty Ratio of PS LED Pulses	50%	—	—		
PS ADC Count Value (no object)	10	120	200	counts	Dedicated duo power supply, V_{LED} = 3V, LED driving 32 pulses, 150 mA, 60 kHz, 10-bit, Gain = 1x (0.7-mm thickness clear glass, 0.3-mm air gap) and no reflective object above the module
PS Reflectivity ADC Count Value (30 mm distance object)	150	225	300	counts	Dedicated duo power supply, V_{LED} = 3V, reflecting object – 73 mm × 83 mm Kodak 18% grey card, 30-mm distance, LED driving 32 pulses, 150 mA, 60 kHz, 10-bit, Gain = 1x (0.7-mm thickness clear glass, 0.3-mm air gap)

Figure 1: Spectral Response

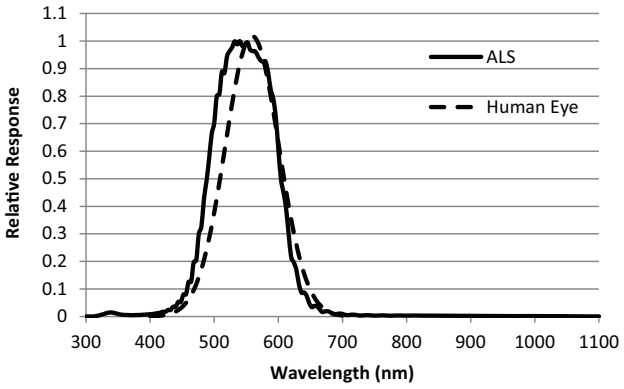


Figure 2: ALS Sensor LUX vs Meter LUX Using White Light

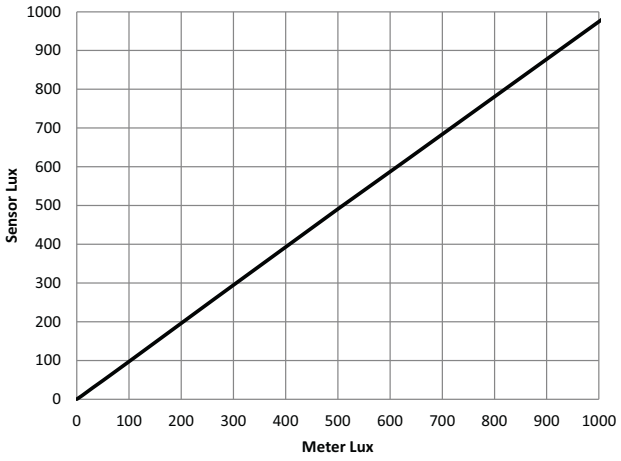


Figure 3: Normalized IDD vs. Temperature

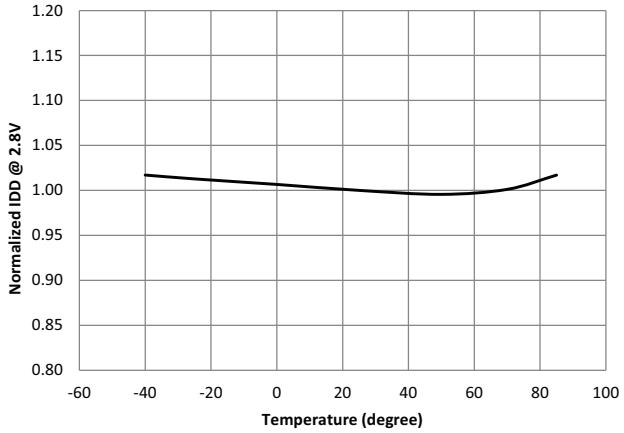


Figure 4: Normalized IDD vs. VDD

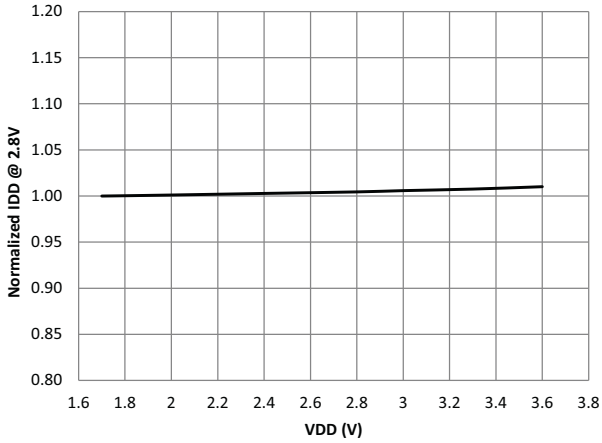
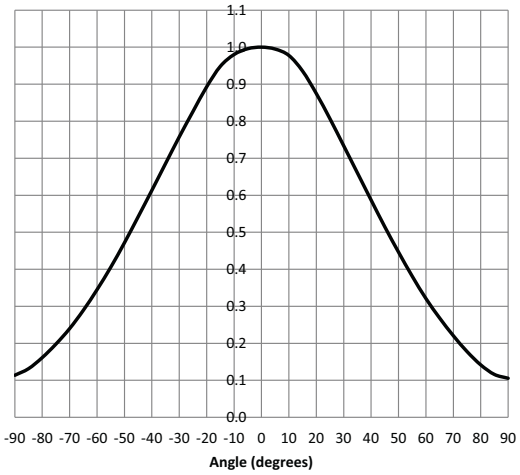


Figure 5: Normalized PD Responsitivity vs Angular Displacement (Perpendicular Axis)



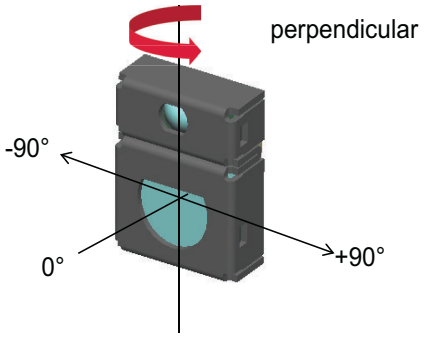
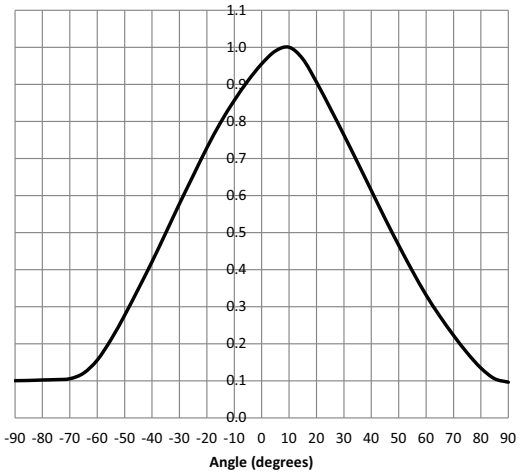
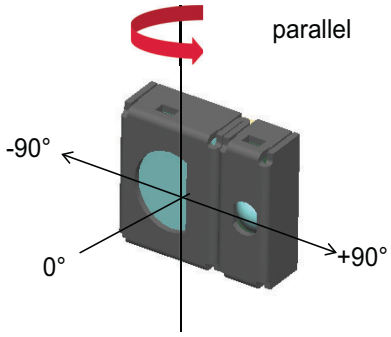


Figure 6: Normalized PD Responsitivity vs Angular Displacement (Parallel Axis)





ALS Gain and Resolution Settings

Gain	Resolution (bits)	Integration Time, itime (ms)	Min Lux	Max Lux	Resolution (lux/count)
1x	16	25	3.272	214412	3.272
	17	50	1.639	214813	1.639
	18	**100 (default)**	**0.819**	**214614**	**0.819**
	19	200	0.409	214557	0.409
	20	400	0.204	214331	0.204
3x (default)	16	25	1.077	70551	1.077
	17	50	0.538	70530	0.538
	18	**100 (default)**	**0.269**	**70531**	**0.269**
	19	200	0.135	70576	0.135
	20	400	0.067	70530	0.067
6x	16	25	0.525	34377	0.525
	17	50	0.263	34416	0.263
	18	**100 (default)**	**0.131**	**34373**	**0.131**
	19	200	0.066	34371	0.066
	20	400	0.033	34418	0.033
18x	16	25	0.169	11046	0.169
	17	50	0.084	11058	0.084
	18	**100 (default)**	**0.042**	**11055**	**0.042**
	19	200	0.021	11045	0.021
	20	400	0.011	11045	0.011
64x	16	25	0.049	3239	0.049
	17	50	0.025	3231	0.025
	18	**100 (default)**	**0.012**	**3233**	**0.012**
	19	200	0.006	3238	0.006
	20	400	0.003	3238	0.003

Principles of Operation for Light Sensor and Proximity Sensor

System State Machine

Start Up after Power-On or Software Reset

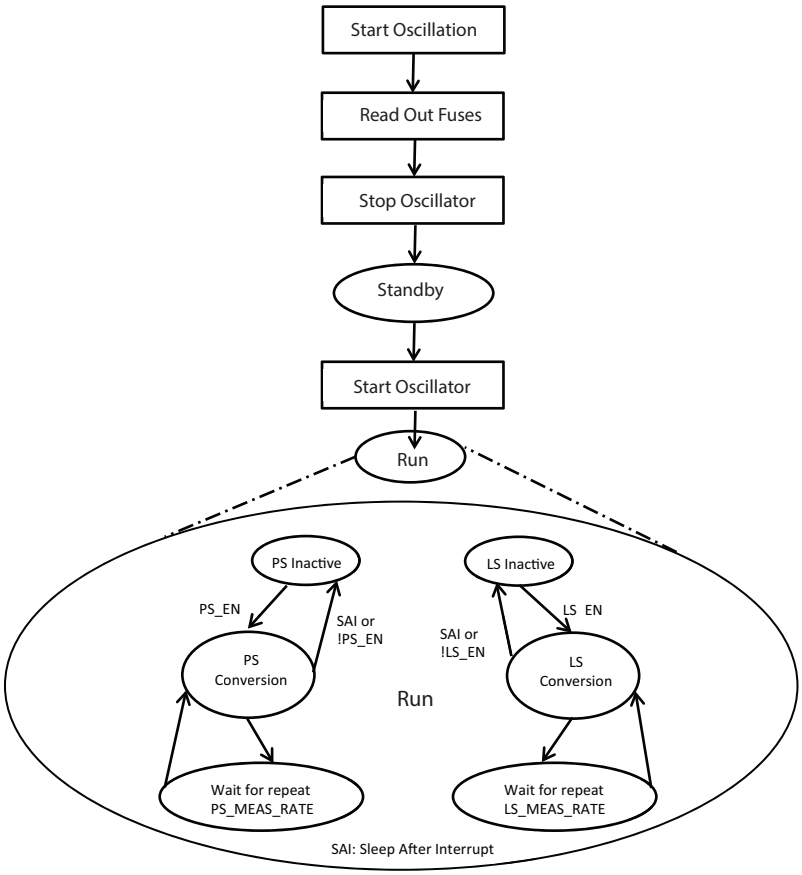
The main state machine is set to "Start State" during power-on or software reset. As soon as the reset is released, the internal oscillator starts. The programmed I^2C address and the trim values are read from the internal non-volatile memory (NVM) trimming data block. APDS-9160-003 (Ambient Light Sensor, ALS) enters into Standby Mode as soon as the Idle State is reached.

If any of the sensor operation modes becomes activated through an I^2C command (LS_EN bit is set to 1 and the sensor mode is selected with the respective bit in the MAIN_CTRL register), the internal support blocks are immediately powered on. Once the voltages and currents are settled (typical after 500 µs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates.

When the user resets the LS_EN bit (or PS_EN bit) to 0, a running conversion is completed and the relevant ADCs move to Standby Mode thereafter. The support blocks only move to Standby Mode if all Sensors are Inactive. If any of the sensors is programmed to sleep after interrupt with the according bit in the MAIN_CTRL register, the relevant ADCs move to Standby Mode after the interrupt condition occurred. Also the sensor's Enable bit LS_EN or PS_EN will be reset after following read out of Main Status register.

The deactivation of either LS or PS in the MAIN_CTRL register does not clear the related status bit in the MAIN_STATUS register. They are always reset upon activation of the respective sensor.

Figure 7: State Diagram



Ambient Light Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It can function as either threshold triggered (ALS_VAR_MODE = 0) or variance trigged (ALS_VAR_MODE = 1).

The threshold interrupt is enabled with ALS_INT_EN = 1 and ALS_VAR_MODE = 0. The interrupt is set when the respective *_DATA register of the selected interrupt source channel is above the upper or below the lower threshold configured in the ALS_THRES_UP and ALS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+LS_PERSIST).

The variance interrupt is enabled with ALS_INT_EN = 1 and ALS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold for a specified number of consecutive measurements (1+ALS_PERSIST).

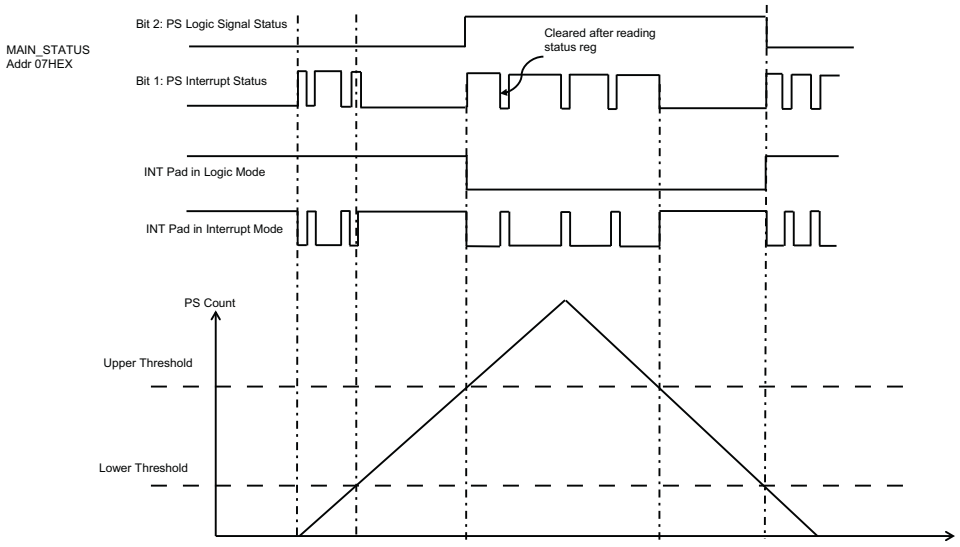
Proximity Sensor Interrupt

APDS-9160-003 generates independent PS interrupt signals. The interrupt is configured by the bit in the INT_CFG register. It is threshold triggered.

The interrupt is enabled with PS_INT_EN = 1. The interrupt is set when the PS_DATA register content is above the upper or below the lower threshold configured in the PS_THRES_UP and PS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+PS_PERSIST).

The ps_logic signal (PS_LOGIC_STAT bit in the MAIN_STATUS register) is set to 0 if the PS data is below the lower PS threshold, and it is set to 1 if the PS data is above the upper PS threshold.

Figure 8: Proximity Sensor Interrupt Behavior



Interrupt

The APDS-9160-003 generates independent ALS and PS interrupt signals. Interrupts will be triggered if upper or lower threshold values are crossed. It is possible to deactivate a sensor after an interrupt event occurred. Therefore a bit for the respective sensor has to be set in the MAIN_CTRL register (SAI_PS and SAI_ALS). This feature is independently available for ALS and PS.

In combination with the PS_PERSIST or ALS_PERSIST setting, up to 16 conversions will be performed before the interrupt is set.

For ALS an interrupt can also be triggered if the output count variation of consecutive conversions has exceeded a defined limit.

The PS Logic Output Mode has priority over any other interrupt signal. If selected (PS_LOGIC_MODE=1), no LS interrupt can be signaled at the INT pad.

The ALS and PS interrupt signals as well as *ps_logic_mode* are active low at the INT pad. A cleared ALS *interrupt status* or PS *interrupt status* flag will also clear the interrupt signal on the INT pad.

Optical Design Considerations

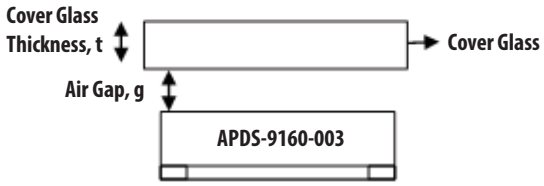
The APDS-9160-003 simplifies the optical system design by eliminating the need for light pipes and optical barrier with specially designed apertures and package shielding which will reduce crosstalk when placed in the final system. The module package design has been optimized for minimum package foot print and short distance proximity of 70 mm typical. The spacing between the cover glass surface and package top surface is critical to controlling the crosstalk. With some simple mechanical design implementations, the APDS-9160-003 will perform well in the end equipment system.

APDS-9160-003 Module Optimized design parameters:

- Window thickness, t ≤ 0.7 mm
- Air gap, g ≤ 0.3 mm
- Cover glass IR transmittance ≥ 80%

The APDS-9160-003 is available in a narrow width and low profile package that contains optics that provides optical gain on both the IR LED and the sensor side of the package. The device has a package Z height of 1.00 mm and will support an air gap of ≤ 0.3 mm between the cover glass and the package. The assumption of the optical system level design is that the cover glass surface above the module is ≤ 0.3 mm.

Figure 9: Optical Design Considerations



I²C Protocol

IInterface and control of the APDS-9160-003 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x53 hex using a 7-bit addressing protocol. (Contact the factory for other addressing options.)

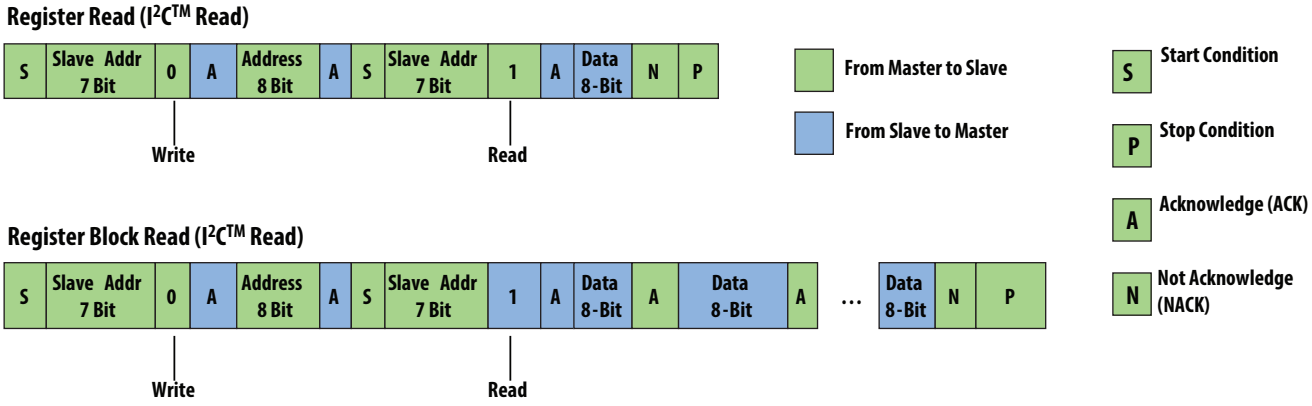
I²C Register Read

The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device does not roll over and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on ALS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the APDS-9160-003 returns NACK until the I²C operation is ended.

Read operations must follow this timing diagram.



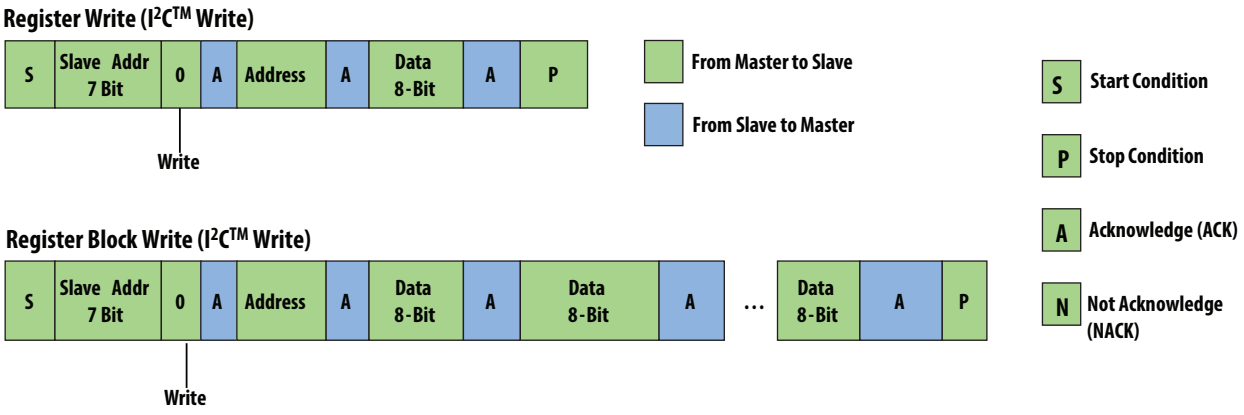
I²C Register Write

The APDS-9160-003 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bit, the register is not skipped. Data written to read-only bit is ignored.

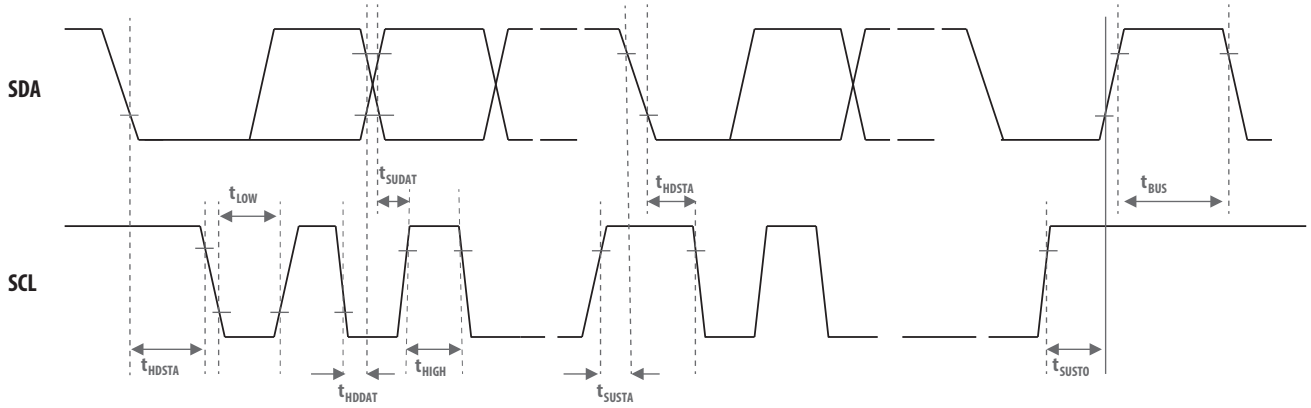
If the last valid address of the APDS-9160-003 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9160-003 does not roll over. The APDS-9160-003 returns NACK for every following byte sent by the master until the I²C operation is ended.

If a write access is started on an address belonging to a non-writeable register, the APDS-9160-003 returns NACK until the I²C operation is ended.

Write operations must follow this timing.



I²C Interface – Bus Timing



Bus Timing Characteristics

Parameter	Symbol	Standard Mode	Fast Mode	Units
Maximum SCL Clock Frequency	f_{SCL}	100	400	kHz
Minimum START Condition Hold Time Relative to SCL Edge	t_{DSTA}	4	—	µs
Minimum SCL Clock Low Width	t_{LOW}	4.7	—	µs
Minimum SCL Clock High Width	t_{HIGH}	4	—	µs
Minimum START Condition Setup Time Relative to SCL Edge	t_{SUSTA}	4.7	—	µs
Minimum Data Hold Time on SDA Relative to SCL Edge	t_{HDDAT}	0	—	µs
Minimum Data Setup Time on SDA Relative to SCL Edge	t_{SUDAT}	0.1	0.1	µs
Minimum STOP Condition Setup Time on SCL	t_{SUSTO}	4	—	µs
Minimum Bus Free Time between Stop Condition and Start Condition	t_{BUS}	4.7	—	µs

Register Set

The APDS-9160-003 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	Operation mode control, SW reset	00HEX
01HEX	RW	PS_LED	PS LED settings	33HEX
02HEX	RW	PS_PULSES	Number of LED pulses	08HEX
03HEX	RW	PS_MEAS_RATE	PS measurement rate in active mode	05HEX
04HEX	RW	ALS_MEAS_RATE	ALS measurement rate and resolution setting	22HEX
05HEX	RW	ALS_GAIN	ALS analog gain range	01HEX
06HEX	RW	PART_ID	Part number ID	03HEX
07HEX	R	MAIN_STATUS	Power-on status, interrupt status, data status	20HEX
08HEX	R	PS_DATA_0	PS measurement data – LSB	00HEX
09HEX	R	PS_DATA_1	PS measurement data – MSB and overflow	00HEX
0AHEX	R	LS_CLEAR_DATA_0	LS CLEAR ADC measurement data – LSB	00HEX
0BHEX	R	LS_CLEAR_DATA_1	LS CLEAR ADC measurement data	00HEX
0CHEX	R	LS_CLEAR_DATA_2	LS CLEAR ADC measurement data – MSB	00HEX
0DHEX	R	ALS_DATA_0	ALS ADC measurement data – LSB	00HEX
0EHEX	R	ALS_DATA_1	ALS ADC measurement data	00HEX
0FHEX	R	ALS_DATA_2	ALS ADC measurement data – MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PST	Interrupt persist setting	00HEX
1BHEX	RW	PS_ THRES _UP_0	PS Interrupt upper threshold, LSB	FFHEX
1CHEX	RW	PS_ THRES _UP_1	PS Interrupt upper threshold, MSB	07HEX
1DHEX	RW	PS_ THRES _LOW_0	PS Interrupt lower threshold, LSB	00HEX
1EHEX	RW	PS_ THRES _LOW_1	PS Interrupt lower threshold, MSB	00HEX
1FHEX	RW	PS_ CAN_DIG_0	PS intelligent cancellation level setting, LSB	00HEX
20HEX	RW	PS_ CAN_DIG_1	PS intelligent cancellation level setting, MSB	00HEX
21HEX	RW	PS_CAN_ANA_DURATION	PS analog cancellation pulse duration	00HEX
22HEX	RW	PS_CAN_ANA_CURRENT	PS analog cancellation (current)	00HEX
23HEX	RW	PS_ AV_HYST	PS averaging and hysteresis control	00HEX
24HEX	RW	ALS_THRES_UP_0	ALS interrupt upper threshold, LSB	FFHEX
25HEX	RW	ALS_THRES_UP_1	ALS interrupt upper threshold	FFHEX
26HEX	RW	ALS_THRES_UP_2	ALS interrupt upper threshold, MSB	0FHEX
27HEX	RW	ALS_THRES_LOW_0	ALS interrupt lower threshold, LSB	00HEX
28HEX	RW	ALS_THRES_LOW_1	ALS interrupt lower threshold	00HEX
29HEX	RW	ALS_THRES_LOW_2	ALS interrupt lower threshold, MSB	00HEX
2AHEX	RW	ALS_THRES_VAR	ALS interrupt variance threshold	00HEX

MAIN_CTRL

Default Value: 00HEX

Address: 00HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	SAI_PS	SAI_ALS	SW_RESET	0	0	ALS_EN	PS_EN

Field	Bit	Description
SAI_PS	6	Sleep after interrupt for Proximity Sensor (SAI_PS). When this bit is set, the ALS returns to standby (PS_EN is cleared when the measurement is finished and MAIN_STATUS is read) once an interrupt occurs. This bit reacts on PS interrupt status bit in the MAIN_STATUS register.
SAI_ALS	5	Sleep after interrupt for Light Sensor (SAI_ALS). When this bit is set, the ALS returns to standby (ALS_EN is cleared when the measurement is finished and MAIN_STATUS is read) once an interrupt occurs. This bit reacts on ALS interrupt status bit in the MAIN_STATUS register.
SW_RESET	4	1: Reset will be triggered. If bit is set to 1, a software reset will be triggered. When SW_RESET bit is set, the device has to send an ACK and the RESET shall be executed when the stop bit is sent.
ALS_EN	1	0: Ambient Light Sensor inactive **(default)**. 1: Ambient Light Sensor active.
PS_EN	0	0: Proximity Sensor inactive **(default).** 1: Proximity Sensor active.

PS_LED

Default Value: 33HEX

Address: 01HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	LED PULSE MODULATION FREQUENCY			0	LED CURRENT		

Field	Bit	Description
LED PULSE MODULATION FREQUENCY	6:4	000: Reserved. 001: Reserved. 010: Reserved. 011: LED pulse frequency = 60 kHz **(default)**. 100: LED pulse frequency = 70 kHz. 101: LED pulse frequency = 80 kHz. 110: LED pulse frequency = 90 kHz. 111: LED pulse frequency = 100 kHz.
LED CURRENT	2:0	000: LED pulsed current level = 10 mA. 001: LED pulsed current level = 25 mA. 010: LED pulsed current level = 50 mA. 011: LED pulsed current level = 100 mA **(default)**. 100: LED pulsed current level = 150 mA. 101: LED pulsed current level = 175 mA. 110: LED pulsed current level = 200 mA. 111: LED pulsed current level = 200 mA.

Writing to this register resets PS state machine and starts new measurements.

PS_PULSES

Default Value: 08HEX

Address: 02HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS NUMBER OF LED PULSES							

Field	Bit	Description
PS PULSES	7:0	00000000: 0 pulses (no light emission) …. …. 00001000: 8 pulses **(default)** …. …. 00100000: 32 pulses …. …. 11111111: 255 pulses.

Writing to this register resets PS state machine and starts new measurements.

PS_MEAS_RATE

Default Value: 05HEX

Address: 03HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS GAIN		0	PS RESOLUTION		PS MEASUREMENT RATE		

Field	Bit	Description
PS GAIN	7:6	00: 1x **(default)**. 01: 2x 10: 4x 11: 8x
PS RESOLUTION/BIT WIDTH	4:3	00: 8 bit (**default)**. 01: 9 bit. 10: 10 bit. 11: 11 bit.
PS MEASUREMENT RATE	2:0	000: Reserved. 001: 6.25 ms. 010: 12.5 ms. 011: 25 ms. 100: 50 ms. 101: 100 ms **(default)**. 110: 200 ms. 111: 400 ms.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets PS state machine and starts new measurements.

ALS_MEAS_RATE

Default Value: 22HEX

Address: 04HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	ALS RESOLUTION BT WIDTH			0	ALS MEASUREMENT RATE		

Field	Bit	Description
ALS RESOLUTION/BIT WIDTH	6:4	000: 20 bit – 400 ms 001: 19 bit – 200 ms 010: 18 bit – 100 ms **(default)** 011: 17 bit – 50 ms 100: 16 bit – 25 ms 101: 13 bit – 3.125 ms 110: Reserved 111: Reserved
ALS MEASUREMENT RATE	2:0	000: 25 ms 001: 50 ms 010: 100 ms **(default)** 011: 200 ms 100: 500 ms 101: 1000 ms 110: 2000 ms 111: 2000 ms

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets ALS state machine and starts new measurements.

ALS_GAIN

Default Value: 01HEX

Address: 05HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	ALS GAIN RANGE		

Field	Bit	Description
ALS GAIN RANGE	2:0	000: Gain 1 001: Gain 3 **(default)** 010: Gain 6 011: Gain 18 100: Gain 54

Writing to this register resets LS state machine and starts new measurements.

PART_ID

Default Value: 03HEX

Address: 06HEX

B7	B6	B5	B4	B3	B2	B1	B0
Part ID							

Field	Bit	Description
PART ID	7:0	Part number ID.

MAIN_STATUS

Default Value: 20HEX

Address: 07HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	POWER ON STATUS	ALS INTERRUPT STATUS	ALS DATA STATUS	PS LOGIC SIGNAL STATUS	PS INTERRUPT STATUS	PS DATA STATUS

Field	Bit	Description
POWER ON STATUS	5	1 : Part went through a power-up event, either because the part was turned on or because there was power supply voltage disturbance. (default at first register read). All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
ALS INTERRUPT STATUS	4	0 : Interrupt condition has not occurred **(default).** 1 : Interrupt condition has occured (cleared after read).
ALS DATA STATUS	3	0 : Old data, already read **(default).** 1: New data, not yet read (cleared after read).
PS LOGIC SIGNAL STATUS	2	0 : Object is far **(default).** 1 : Object is near
PS INTERRUPT STATUS	1	0 : Interrupt condition has not occurred **(default)**. 1 : Interrupt condition has occurred (cleared after read).
PS DATA STATUS	0	0 : Old data, already read **(default)**. 1 : New data, not yet read (cleared after read).

PS_DATA

Default Value: 00HEX, 00HEX

Address: 08HEX, 09HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_DATA_0							
0	0	0	PS_AMBIENT_ LIGHT_ OVERFLOW	PS_DATA_ OVERFLOW	PS_DATA_1		

If an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, both registers PS_DATA_0 and PS_DATA_1 are locked until the I^2C read operation is completed or the specified address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual PS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

The PS conversion result is always written LSB-aligned into the PS_DATA registers, regardless of the conversion resolution selected in the PS_MEAS_RATE register. PS_DATA_1 is filled with 0 for resolutions lower than 11 bit. If the PS data is outside of the measurable range, the Overflow flag (PS_DATA_1, Bit [3]) is set in any resolution mode.

PS_DATA is automatically corrected by the value of the PS cancellation register (PS_CAN).

PS_DATA = PS_MEAS – PS_CAN

PS_MEAS is the internal raw value obtained from the PS ADC. If PS_MEAS is already full-scale, then the value of PS_DATA is set to its maximum value without subtracting the PS cancellation value.

PS_AMBIENT_LIGHT_OVERFLOW is set when strong ambient light is seen by proximity sensor. This bit will be set if ambient light is above 300K lux sunlight

Reg 08HEX	7:0	PS measurement least significant data byte, bit 0 is the LSB of the data word.
Reg 09HEX	4	0: Valid PS data **(default)**. 1: Strong ambient light.
	3	0: Valid PS data (**default).** 1: Overflow of PS data.
	2:0	PS measurement most significant data byte, bit 2 is the MSB in 11-bit mode.

LS_CLEAR_DATA

Default Value: 00HEX, 00HEX, 00HEX

Address: 0AHEX, 0BHEX, 0CHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_CLEAR_DATA_0							
LS_CLEAR_DATA_1							
0	0	0	0	LS_CLEAR_DATA_2			

CLEAR channel digital output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

The channel out is already compensated internally: LS_CLEAR_DATA = LS_CLEAR_{int} – COMP

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual *_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 0AHEX	7:0	CLEAR PD data least significant data byte
Reg 0BHEX	7:0	CLEAR PD data intervening data byte
Reg 0CHEX	3:0	CLEAR PD data most significant data byte

ALS_DATA

Default Value: 00HEX, 00HEX, 00HEX

Address: 0DHEX, 0EHEX, 0FHEX

B7	B6	B5	B4	B3	B2	B1	B0
ALS_DATA_0							
ALS_DATA_1							
0	0	0	0	ALS_DATA_2			

ALS channel digital output data (unsigned integer, 13 bit to 20 bit, LSB aligned).

The channel out is already compensated internally: ALS_DATA = ALSint - COMP

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual *_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 0DHEX	7:0	ALS data least significant data byte
Reg 0EHEX	7:0	ALS data intervening data byte
Reg 0FHEX	3:0	ALS data most significant data byte

INT_CFG

Default Value: 10HEX

Address: 19HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	ALS_INT_SEL		ALS_VAR_ MODE	ALS_INT_EN	PS_LOGIC_ MODE	PS_INT_EN

Field	Bit	Description
ALS_INT_SEL	5:4	00: Clear channel. 01: ALS channel **(default)**.
ALS_VAR_MODE	3	0: ALS threshold interrupt mode **(default)**. 1: ALS variation interrupt mode.
ALS_INT_EN	2	0: ALS interrupt disabled **(default).** 1: ALS interrupt enabled.
PS_LOGIC_MODE	1	0: Normal interrupt disabled **(default).** After interrupt event, INT pad maintains active level until MAIN_STATUS register is read **(default)**. 1: PS logic output mode. INT pad is updated after every measurement and maintains output state between measurements.
PS_INT_EN	0	0: PS interrupt disabled **(default)**. 1: PS interrupt enabled.

INT_PST

Default Value: 00HEX

Address: 1AHEX

B7	B6	B5	B4	B3	B2	B1	B0
ALS_PERSIST				PS_PERSIST			

FIELD	BIT	DESCRIPTION
ALS_PERSIST	7:4	0000: Every ALS value out of threshold range **(default)** asserts an interrupt. 0001: 2 consecutive ALS values out of threshold range assert an interrupt. … 1111: 16 consecutive ALS values out of threshold range assert an interrupt.
PS_PERSIST	3:0	0000: Every PS value out of threshold range (**default)** asserts an interrupt. 0001: 2 consecutive PS values out of threshold range assert an interrupt. … 1111: 16 consecutive PS values out of threshold range assert an interrupt.

PS_THRES_UP

Default Value: FFHEX, 07HEX

Address: 1BHEX, 1CHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_UP_0							
0	0	0	0	0	PS_THRES_UP_1		

PS_THRES_UP sets the upper threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_UP against measured data in the PS_DATA registers. It generates an interrupt event if PS_DATA exceeds the upper threshold level.

The data format for PS_THRES_UP must match that of the PS_DATA registers.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1BHEX	7:0	PS upper interrupt threshold value, LSB.
Reg 1CHEX	2:0	PS upper interrupt threshold value, MSB.

PS_THRES_LOW

Default Value: 00HEX, 00HEX

Address: 1DHEX, 1EHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_LOW_0							
0	0	0	0	0	PS_THRES_LOW_1		

PS_THRES_LOW sets the lower threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_LOW against measured data in the PS_DATA registers. It generates an interrupt event if PS_DATA is lower than the lower threshold level.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1DHEX	7:0	PS lower interrupt threshold value, LSB.
Reg 1EHEX	2:0	PS lower interrupt threshold value, MSB.

PS_CAN_DIG

Default Value: 00HEX, 00HEX

Address: 1FHEX, 20HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_CAN_DIG_0							
0	0	0	0	0	PS_CAN_DIG_1		

The PS cancellation level is expected to be written by the MCU during system startup. The digital value is subtracted from the measured PS data before the data is transferred to the PS_DATA registers and evaluated by the Interrupt Controller.

The data format for PS_CAN_DIG must match to the data format of PS_DATA.

For resolution below 11 bit, the data LSB aligned.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1FHEX	7:0	PS digital cancellation level, LSB.
Reg 20HEX	2:0	PS digital cancellation level, MSB.

PS_CAN_ANA_DURATION

Default Value: 00HEX

Address: 21HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	PS_CAN_ANA_DURATION						

This value determines the cancellation pulse duration in each of PWM pulse. The cancellation current is applied during the integration phase of the PS measurement. The duration is programmed in half clock cycles. A duration programming of 0 or 1 will not generate any PS cancellation pulse. Depending of the PWM frequency the duration programming is limited.

Writing to these registers resets the PS state machine and starts new measurements.

Field	Bit	Description
PS_CAN_ANA_DURATION	6:0	PS analog cancellation pulse duration

PS_CAN_ANA_CURRENT

Default Value: 00HEX, 00HEX

Address: 22HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	PS_CAN_ANA_COARSE_ CURRENT		PS_CAN_ANA_FINE_CURRENT			

These values determine the current used for crosstalk cancellation. The PS_CAN_ANA_DURATION needs to be more than 1 to make the current affective.

The coarse value defines the cancellation current in steps of 60nA. (60nA, 120nA, 180nA, 240nA).

The fine value adjusts the cancellation current in steps of approximately 2.4nA.

Writing to these registers resets the PS state machine and starts new measurements.

Field	Bit	Description
PS_CAN_ANA_COARSE_CURRENT	5:4	Coarse PS cancellation current
PS_CAN_ANA_FINE_CURRENT	3:0	Fine PS cancellation current

PS_AV_HYST

Default Value: 00HEX

Address: 23HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	PS_AVG_EN	PS_HYS_WIDTH					

The PS raw data, that are scaled based on the resolution setting, are subtracted with the digital crosstalk cancellation value.

If the PS_AVG_EN is set to 1, the PS averaging filter gets activated. The hysteresis calculation follows the averaging block. If the hysteresis width is set to 0 the function is deactivated. The hysteresis width is programmable up to a count value of 63.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 23HEX	6	Enable PS digital data filtering
	5:0	PS hysteresis width (set to zero to disable hysteresis)

ALS_THRES_UP

Default Value: FFHEX, FFHEX, 0FHEX

Address: 24HEX, 25HEX, 26HEX

B7	B6	B5	B4	B3	B2	B1	B0
ALS_THRES_UP_0							
ALS_THRES_UP_1							
0	0	0	0	ALS_THRES_UP_2			

ALS_THRES_UP sets the upper threshold value for the ALS interrupt. The interrupt controller compares the value in ALS_THRES_UP against measured data in the ALS_DATA registers of the selected ALS interrupt channel. It generates an interrupt event if ALS_DATA exceeds the threshold level.

The data format for ALS_THRES_UP must match that of the ALS_DATA registers.

Writing to these registers resets the ALS state machine and starts new measurements.

Reg 24HEX	7:0	ALS upper interrupt threshold value, LSB
Reg 25HEX	7:0	ALS upper interrupt threshold value, intervening byte
Reg 26HEX	3:0	ALS upper interrupt threshold value, MSB

ALS_THRES_LOW

Default Value: 00HEX, 00HEX, 00HEX

Address: 27EX, 28HEX, 29HEX

B7	B6	B5	B4	B3	B2	B1	B0
ALS_THRES_LOW_0							
ALS_THRES_LOW_1							
0	0	0	0	ALS_THRES_LOW_2			

ALS_THRES_LOW sets the lower threshold value for the ALS interrupt. The interrupt controller compares the value in ALS_THRES_LOW against measured data in the ALS_DATA registers of the selected ALS interrupt channel. It generates an interrupt event if ALS_DATA exceeds the threshold level.

The data format for ALS_THRES_LOW must match that of the ALS_DATA registers.

Writing to these registers resets the ALS state machine and starts new measurements.

Reg 27HEX	7:0	ALS lower interrupt threshold value, LSB
Reg 28HEX	7:0	ALS lower interrupt threshold value, intervening byte
Reg 29HEX	3:0	ALS lower interrupt threshold value, MSB

ALS_THRES_VAR

Default Value: 00HEX

Address: 2AHEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	ALS_THRES_VAR		

Writing to these registers resets the ALS state machine and starts new measurements.

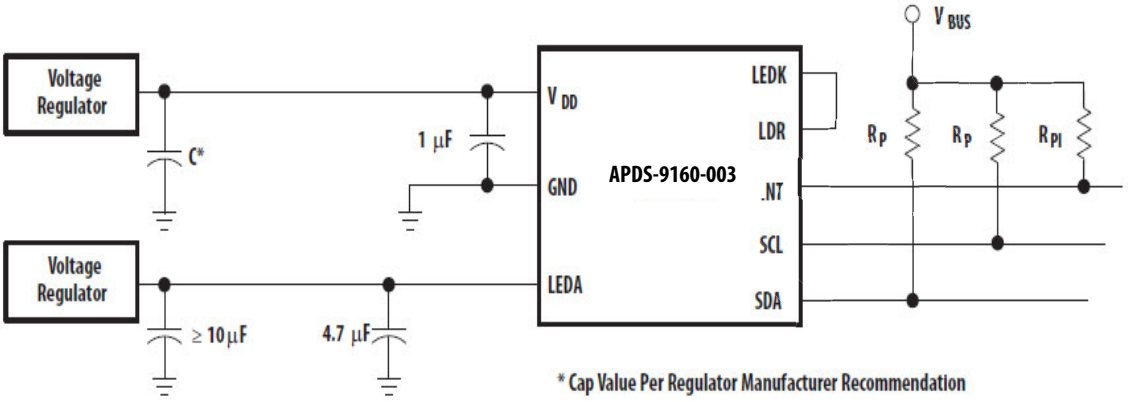
FIELD	BIT	DESCRIPTION
ALS_THRES_VAR	2:0	000: New ALS_DATA varies by **8 counts** compared to previous result. 001: New ALS_DATA varies by **16 counts** compared to previous result. 010: New ALS_DATA varies by **32 counts** compared to previous result. 011: New ALS_DATA varies by **64 counts** compared to previous result. 100: New ALS_DATA varies by **128 counts** compared to previous result. 101: New ALS_DATA varies by **256 counts** compared to previous result. 110: New ALS_DATA varies by **512 counts** compared to previous result. 111: New ALS_DATA varies by **1024 counts** compared to previous result.

Application Information: Hardware

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current. Therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

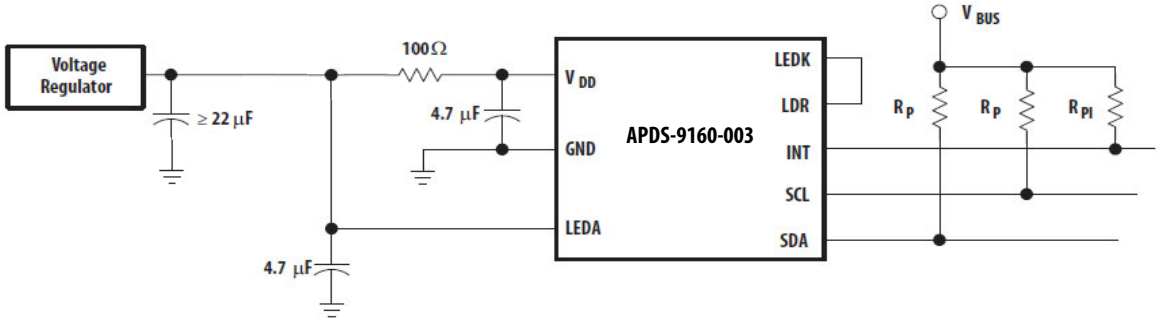
The first recommendation is to use two power supplies: one for the device VDD and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the VDD pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1-µF low-ESR decoupling capacitor as close as possible to the VDD pin and 4.7 µF at the LEDA pin, and at least 10 µF of bulk capacitance to supply the 125-mA current surge.

Figure 10: Proximity Sensing Using Separate Power Supplies



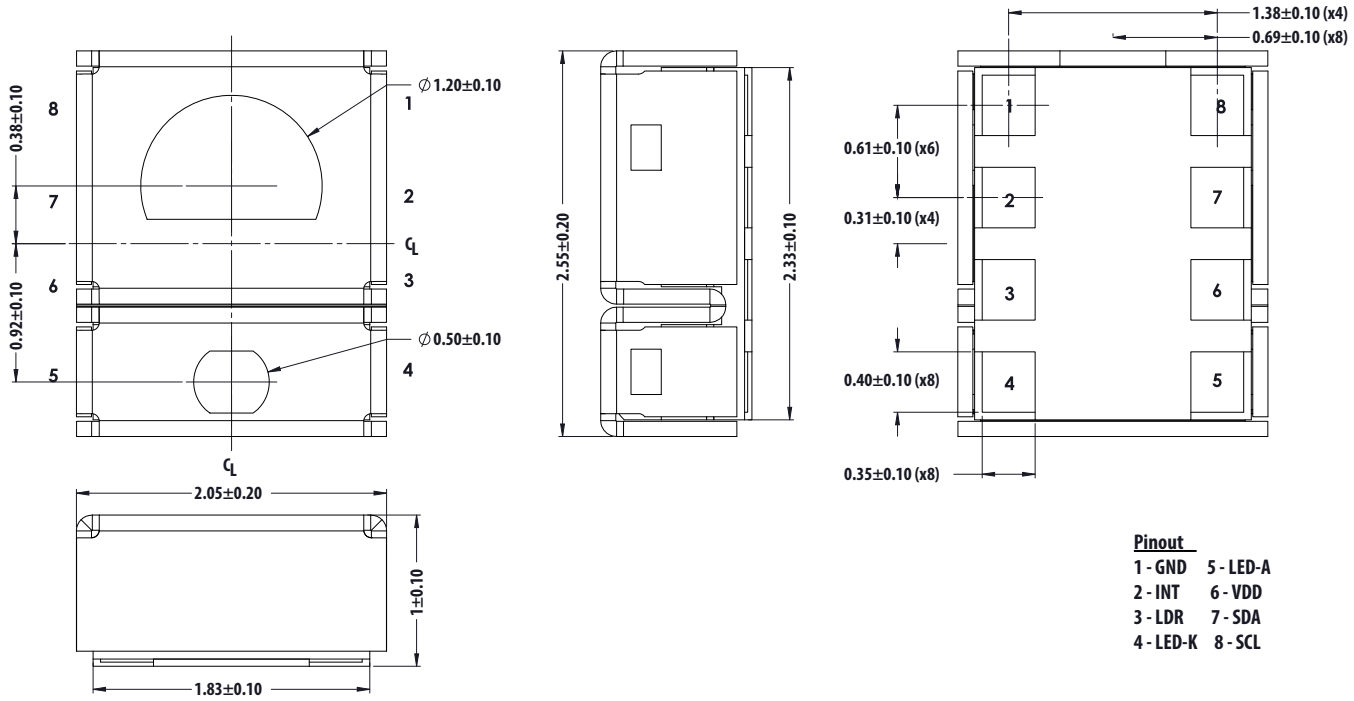
If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 100Ω resistor in series with the VDD supply line and a 4.7-µF ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

Figure 11: Proximity Sensing Using a Single Power Supply



VBUS in the preceding figures refers to the I^2C bus voltage. The I^2C signals and the interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (RP) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. A 10-kΩ pull-up resistor (RPI) can be used for the interrupt line.

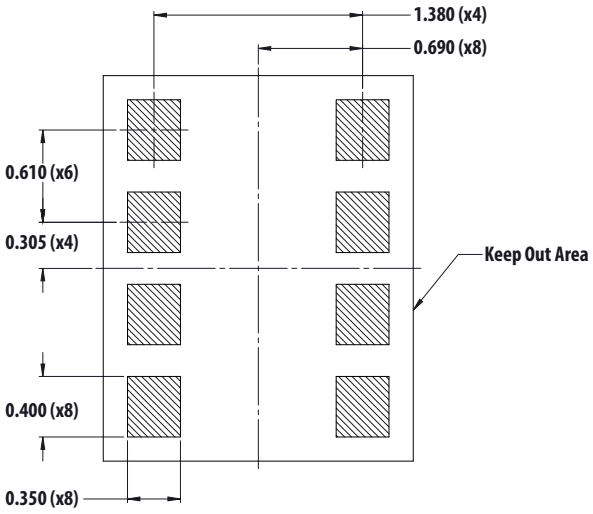
Package Outline Dimensions



NOTE: All linear dimensions are in mm.

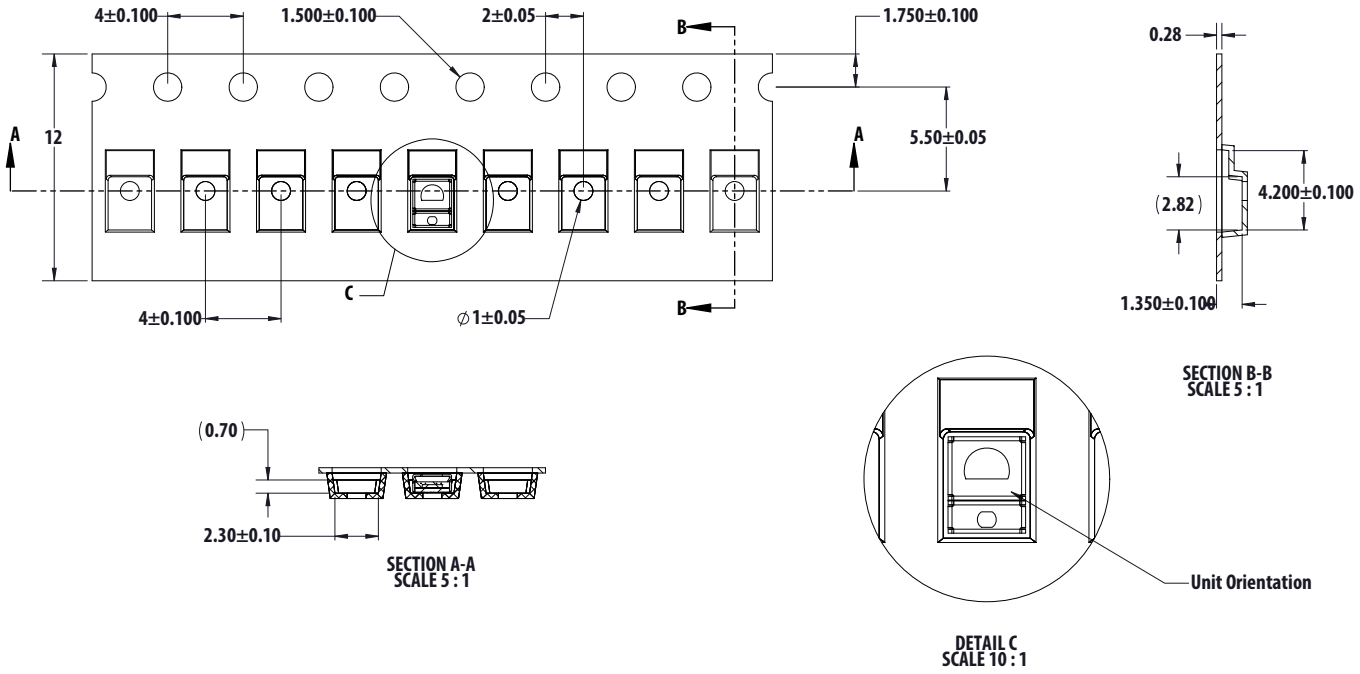
PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are as follows.



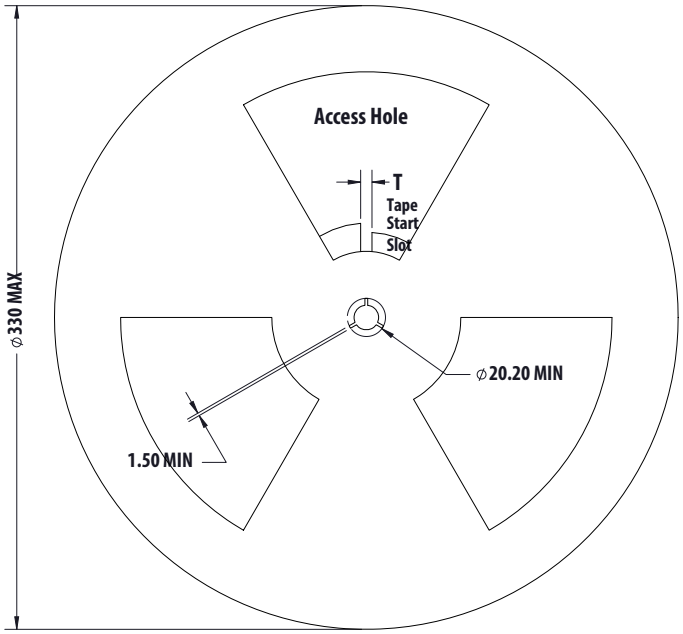
NOTE: All linear dimensions are in mm.

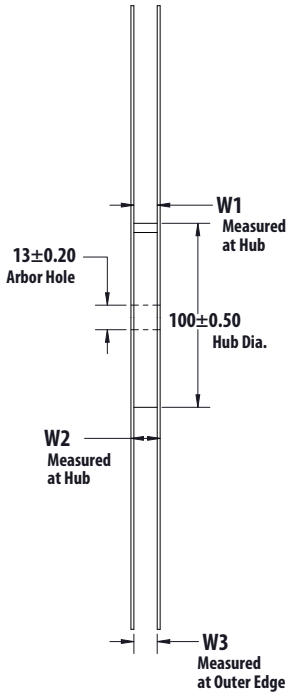
Tape Dimensions



NOTE: All linear dimensions are in mm.

Reel Dimensions



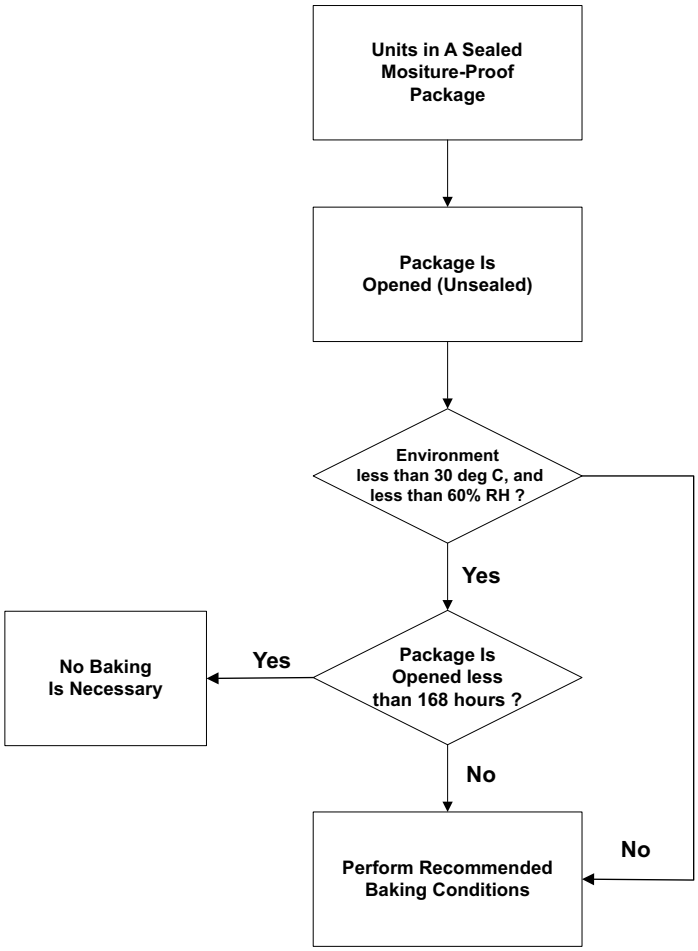


Tape Width	T	W1	W2	W3
12mm	4 ± 0.50	12.4 + 0.2 – 0.0	18.4 Max.	11.9 Min. 15.4 Max.

NOTE: All linear dimensions are in mm.

Moisture Proof Packaging

All APDS-9160 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

Package	Temperature	Time
In Reel	60°C	48 hours
In Bulk	100°C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

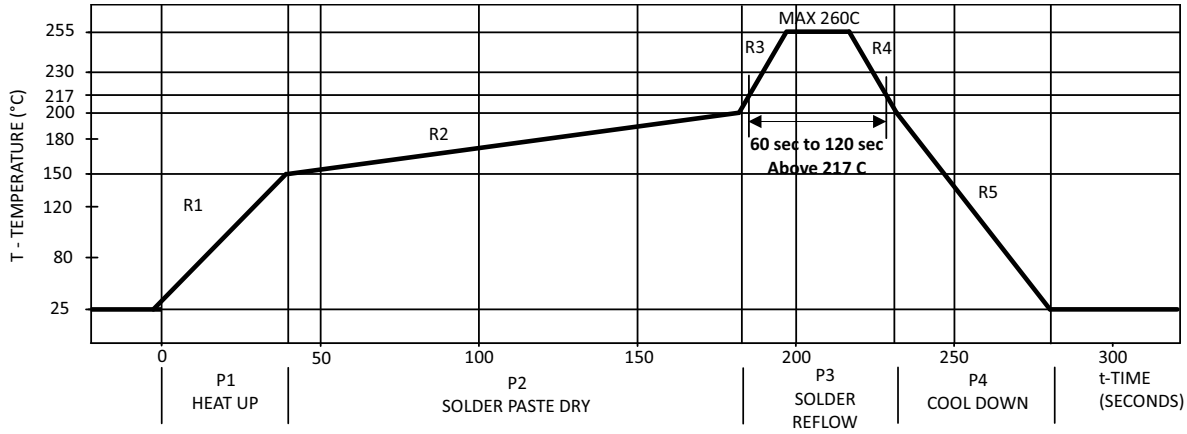
Recommended Storage Conditions

Measurement	Values
Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	∆T	Maximum ∆T/∆time or Duration
Heat Up	P1, R1	25°C to 150°C	3 °C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s –6°C/s
Cool Down	P4, R5	200 °C to 25 °C	–6°C/s
Time Maintained above Liquidus Point , 217°C		> 217°C	60s to 120s
Peak Temperature		260°C	—
Time within 5°C of actual Peak Temperature		> 255°C	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8 minutes

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different T/ time temperature change rates or duration. The T/ time rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100s to 180s) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60s and 120s. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

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