

High bandwidth (20 MHz for gain ≥ 4) micro-power (820 μA) rail-to-rail 5 V op amps

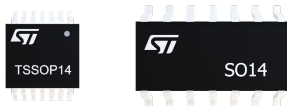
TSV991



TSV992



TSV994



Features

- Low input offset voltage: 1.5 mV max. (A grade)
- Rail-to-rail input and output
- Wide bandwidth 20 MHz
- Stable for gain ≥ 4 or ≤ -3
- Low power consumption: 820 μA typ.
- High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- Low input bias current, 1 pA typ.
- ESD internal protection ≥ 5 kV

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning and active filtering
- Medical instrumentation
- Automotive applications

Maturity status link

[TSV991, TSV992, TSV994, TSV991A, TSV992A, TSV994A](#)

Related products

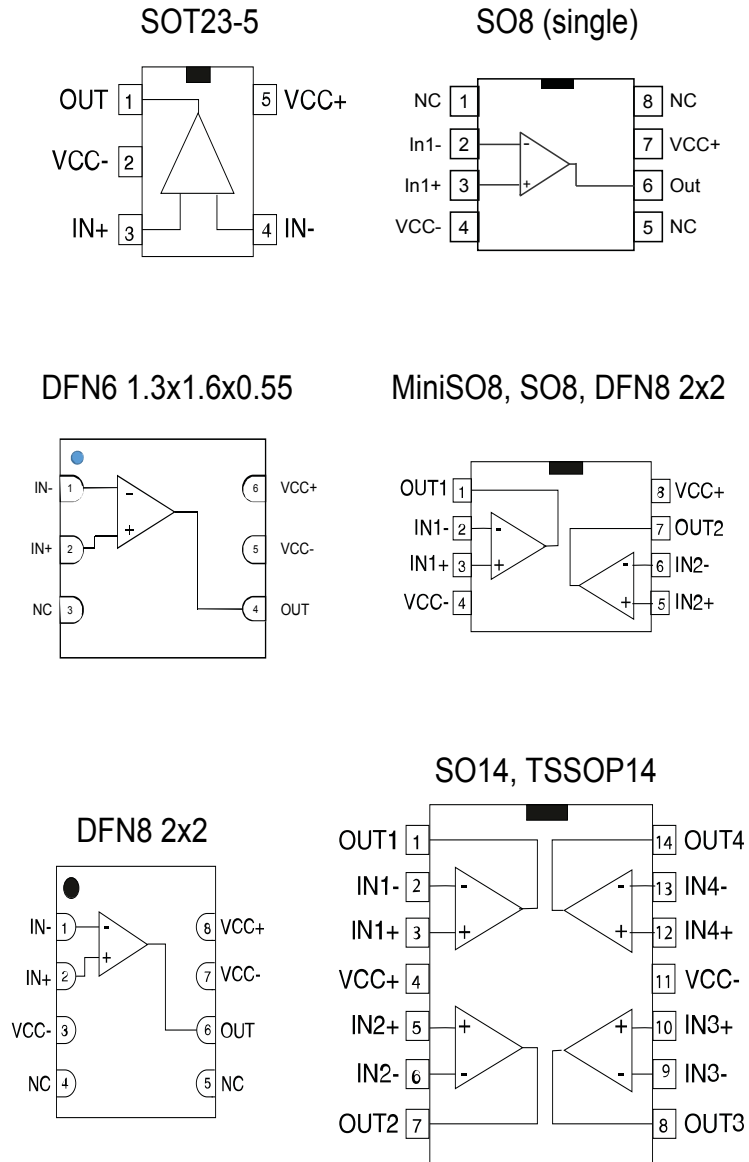
See TSV771 , TSV772	For 20 MHz unity-gain stable amplifiers
See TSV911 , TSV912 , TSV914 , TSV911A , TSV912A , TSV914A	For 8 MHz unity-gain stable amplifiers

Description

The TSV99x and TSV99xA family of single, dual, and quad operational amplifiers offers low voltage operation and rail-to-rail input and output. These devices feature an excellent speed/power consumption ratio, offering a 20 MHz gain-bandwidth, stable for gains above 4 (100 pF capacitive load), while consuming only 1.1 mA maximum at 5 V. They also feature an ultra-low input bias current. These characteristics make the TSV99x family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering. These characteristics make the TSV99x, TSV99xA family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

1 Package pin connections

Figure 1. Pin connection (top view)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit	
V_{CC}	Supply voltage ⁽¹⁾	6	V	
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$		
V_{in}	Input voltage ⁽³⁾	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$		
I_{in}	Input current ⁽⁴⁾	10	mA	
T_{stg}	Storage temperature	-65 to 150	°C	
T_j	Maximum junction temperature	150		
R_{thja}	Thermal resistance junction to ambient ^{(5) (6)}	DFN8 2x2	57	°C/W
		DFN6 1.3x1.6x0.55	230	
		SOT23-5	250	
		SO8	125	
		MiniSO8	190	
		SO14	103	
R_{thjc}	Thermal resistance junction to case	TSSOP14	100	
		SOT23-5	81	
		SO8	40	
		MiniSO8	39	
		SO14	31	
ESD	CDM: charged device model ⁽⁹⁾	TSSOP14	32	
		SOT23-5, SO8, MiniSO8, DFN8 2x2	1500	
		DFN6 1.3x1.6x0.55	1500	
		TSSOP14	750	
		SO14	500	
ESD	HBM: human body model ⁽⁷⁾	5	kV	
	MM: machine model ⁽⁸⁾	400	V	
ESD	CDM: charged device model ⁽⁹⁾	SOT23-5, SO8, MiniSO8, DFN8 2x2		1500
		DFN6 1.3x1.6x0.55		1500
		TSSOP14		750
		SO14		500
	Latch-up immunity	200	mA	

1. Value is with respect to the V_{CC-} pin.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC} - V_{IN}$ must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: 200 pF charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus packages are charged together to the specified voltage and then discharged directly to the ground.



Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{op}	Operating free air temperature range	-40 to 125	°C

3 Electrical characteristics

Note: In the electrical characteristic tables below, all parameter limits at temperatures other than 25 °C are guaranteed by correlation.

Table 3. Electrical characteristics at $V_{CC+} = 2.5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV99x	$T_{op} = 25\text{ °C}$		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage, TSV99xA	$T_{op} = 25\text{ °C}$			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/\text{°C}$
I_{io}	Input offset current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ °C}$		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ °C}$		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio, $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0\text{ V to } 2.5\text{ V}$, $V_{out} = 1.25\text{ V}$, $T_{op} = 25\text{ °C}$	58	75		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega$, $V_{out} = 0.5\text{ V to } 2\text{ V}$, $T_{op} = 25\text{ °C}$	80	89		
		$T_{min} < T_{op} < T_{max}$	75			
$V_{CC} - V_{OH}$	High-level output voltage	$R_L = 10\text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	mV
		$R_L = 600\ \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	
		$R_L = 600\ \Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
I_{out}	I_{sink}	$V_o = 2.5\text{ V}$, $T_{op} = 25\text{ °C}$	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	$V_o = 0\text{ V}$, $T_{op} = 25\text{ °C}$	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$, $T_{min} < T_{op} < T_{max}$		0.78	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$, $T_{op} = 25\text{ °C}$		20		MHz
Gain	Minimum gain for stability	Phase margin = 45°, $R_f = 10\text{ k}\Omega$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_{op} = 25\text{ °C}$, positive gain configuration		4		V/V
Gain	Minimum gain for stability	Phase margin = 45°, $R_f = 10\text{ k}\Omega$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_{op} = 25\text{ °C}$, negative gain configuration		-3		V/V
SR	Slew rate	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_{op} = 25\text{ °C}$		10		V/ μs



Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f = 10 \text{ kHz}, T_{op} = 25 \text{ }^\circ\text{C}$		21		nV/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion	$G = -3, f = 1 \text{ kHz}, R_L = 2 \text{ k}\Omega, \text{Bw} = 22 \text{ kHz}, V_{icm} = V_{CC}/2, V_{out} = 2 V_{pp}, T_{op} = 25 \text{ }^\circ\text{C}$		0.0025		%

1. Guaranteed by design.

Table 4. Electrical characteristics at $V_{CC+} = 3.3\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV99x	$T_{op} = 25\text{ }^{\circ}\text{C}$		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage, TSV99xA	$T_{op} = 25\text{ }^{\circ}\text{C}$			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/^{\circ}\text{C}$
I_{io}	Input offset current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ }^{\circ}\text{C}$		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ }^{\circ}\text{C}$		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio, $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0\text{ V to } 3.3\text{ V}$, $V_{out} = 1.65\text{ V}$, $T_{op} = 25\text{ }^{\circ}\text{C}$	60	78		dB
		$T_{min} < T_{op} < T_{max}$	55			
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega$, $V_{out} = 0.5\text{ V to } 2.8\text{ V}$, $T_{op} = 25\text{ }^{\circ}\text{C}$	80	89		
		$T_{min} < T_{op} < T_{max}$	75			
$V_{CC} - V_{OH}$	High-level output voltage	$R_L = 10\text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	mV
		$R_L = 600\text{ }\Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$, $T_{min} < T_{op} < T_{max}$		15	40	
		$R_L = 600\text{ }\Omega$, $T_{min} < T_{op} < T_{max}$		45	150	
I_{out}	I_{sink}	$V_o = 3.3\text{ V}$, $T_{op} = 25\text{ }^{\circ}\text{C}$	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	$V_o = 0\text{ V}$, $T_{op} = 25\text{ }^{\circ}\text{C}$	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$, $T_{min} < T_{op} < T_{max}$		0.8	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$, $T_{op} = 25\text{ }^{\circ}\text{C}$		20		MHz
Gain	Minimum gain for stability	Phase margin = 45° , $R_f = 10\text{ k}\Omega$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_{op} = 25\text{ }^{\circ}\text{C}$, positive gain configuration		4		V/V
		Phase margin = 45° , $R_f = 10\text{ k}\Omega$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_{op} = 25\text{ }^{\circ}\text{C}$, negative gain configuration		-3		
SR	Slew rate	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$, $T_{op} = 25\text{ }^{\circ}\text{C}$		10		V/ μs
e_n	Equivalent input noise voltage	$f = 10\text{ kHz}$, $T_{op} = 25\text{ }^{\circ}\text{C}$		21		nV/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion	$G = -3$, $f = 1\text{ kHz}$, $R_L = 2\text{ k}\Omega$, $B_w = 22\text{ kHz}$, $V_{icm} = V_{CC}/2$, $V_{out} = 2.8 V_{pp}$, $T_{op} = 25\text{ }^{\circ}\text{C}$		0.0018		%

1. Guaranteed by design.

Table 5. Electrical characteristics at $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage, TSV99x	$T_{op} = 25\text{ }^{\circ}\text{C}$		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage, TSV99xA	$T_{op} = 25\text{ }^{\circ}\text{C}$			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/^{\circ}\text{C}$
I_{io}	Input offset current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ }^{\circ}\text{C}$		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$ (1)	$T_{op} = 25\text{ }^{\circ}\text{C}$		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio, $20\log(\Delta V_{ic}/\Delta V_{io})$	$0\text{ V to }5\text{ V}, V_{out} = 2.5\text{ V},$ $T_{op} = 25\text{ }^{\circ}\text{C}$	62	82		dB
		$T_{min} < T_{op} < T_{max}$	57			
SVR	Supply voltage rejection ratio, $20\log(\Delta V_{cc}/\Delta V_{io})$	$V_{CC} = 2.5\text{ V to }5\text{ V}$	70	86		
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega, V_{out} = 0.5\text{ V to }4.5\text{ V},$ $T_{op} = 25\text{ }^{\circ}\text{C}$	80	91		
		$T_{min} < T_{op} < T_{max}$	75			
$V_{CC} - V_{OH}$	High-level output voltage	$R_L = 10\text{ k}\Omega, T_{min} < T_{op} < T_{max}$		15	40	mV
		$R_L = 600\text{ }\Omega, T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega, T_{min} < T_{op} < T_{max}$		15	40	
		$R_L = 600\text{ }\Omega, T_{min} < T_{op} < T_{max}$		45	150	
I_{out}	I_{sink}	$V_O = 5\text{ V}, T_{op} = 25\text{ }^{\circ}\text{C}$	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	$V_O = 0\text{ V}, T_{op} = 25\text{ }^{\circ}\text{C}$	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per channel)	No load, $V_{out} = 2.5\text{ V}, T_{min} < T_{op} < T_{max}$		0.82	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}, f = 100\text{ kHz},$ $T_{op} = 25\text{ }^{\circ}\text{C}$		20		MHz
Gain	Minimum gain for stability	Phase margin = 45° , $R_f = 10\text{ k}\Omega,$ $R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}, T_{op} = 25\text{ }^{\circ}\text{C},$ positive gain configuration		4		V/V
		Phase margin = 45° , $R_f = 10\text{ k}\Omega,$ $R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}, T_{op} = 25\text{ }^{\circ}\text{C},$ negative gain configuration		-3		
SR	Slew rate	$R_L = 2\text{ k}\Omega, C_L = 100\text{ pF}, f = 100\text{ kHz},$ $T_{op} = 25\text{ }^{\circ}\text{C}$		10		V/ μs
e_n	Equivalent input noise voltage	$f = 10\text{ kHz}, T_{op} = 25\text{ }^{\circ}\text{C}$		21		nV/ $\sqrt{\text{Hz}}$



Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion	$G = -3$, $f = 1$ kHz, $R_L = 2$ k Ω , $Bw = 22$ kHz, $V_{icm} = V_{CC}/2$, $V_{out} = 4.4 V_{pp}$, $T_{op} = 25$ °C		0.0014		%

1. *Guaranteed by design.*

4 Electrical characteristic curves

Figure 2. Input offset voltage distribution at T = 25 °C

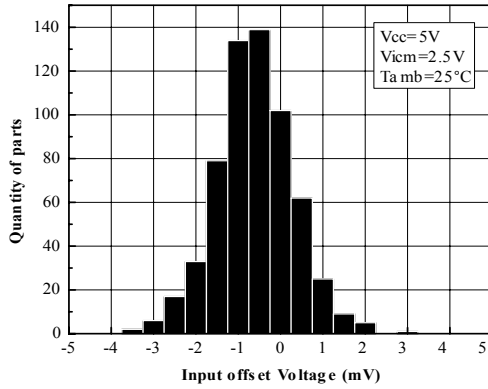


Figure 3. Input offset voltage distribution at T = 125 °C

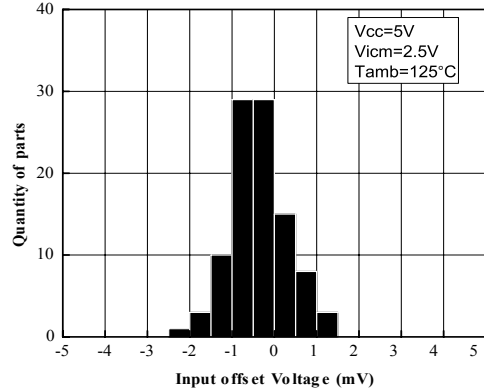


Figure 4. Supply current vs. input common-mode voltage at V_{CC} = 2.5 V

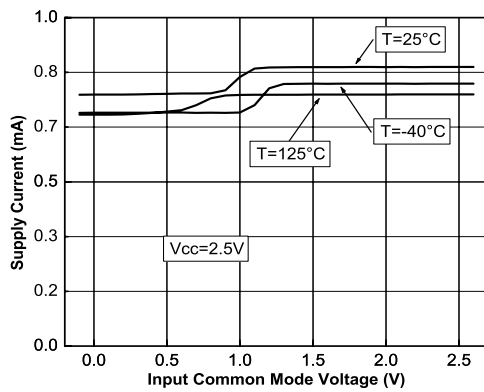


Figure 5. Supply current vs. input common-mode voltage at V_{CC} = 5 V

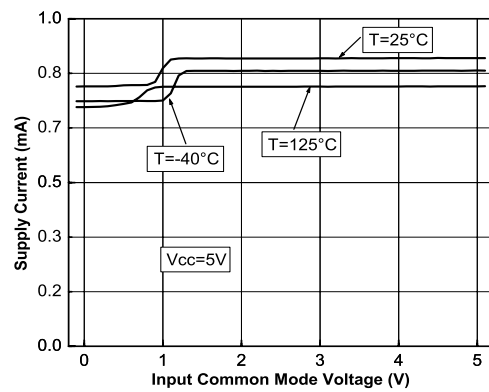


Figure 6. Output current vs. output voltage at V_{CC} = 2.5 V

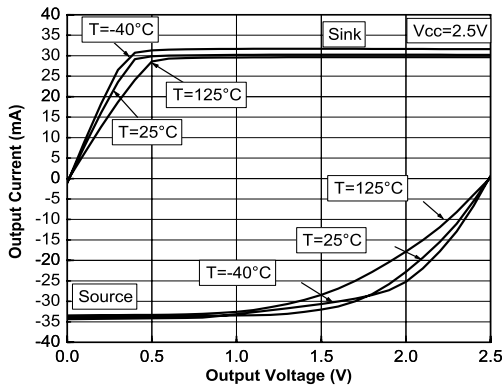


Figure 7. Output current vs. output voltage at V_{CC} = 5 V

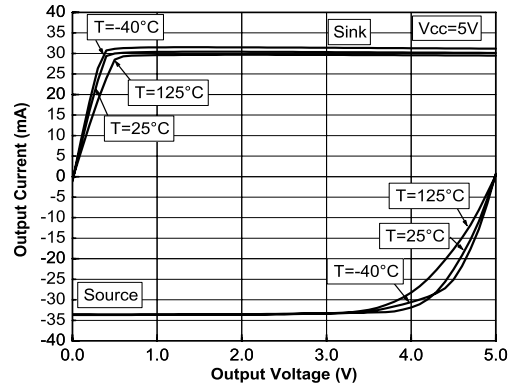


Figure 8. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V and $V_{icm} = 0.5$ V

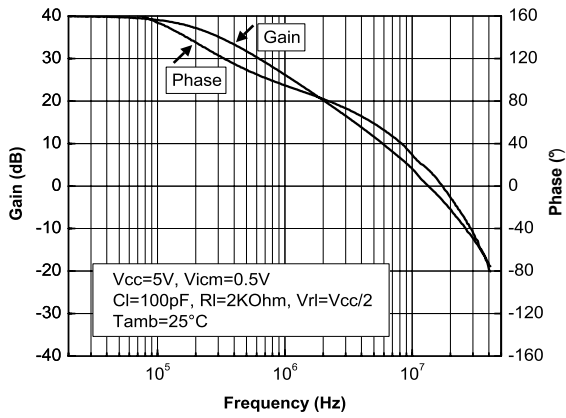


Figure 9. Voltage gain and phase vs. frequency at $V_{CC} = 5$ V and $V_{icm} = 2.5$ V

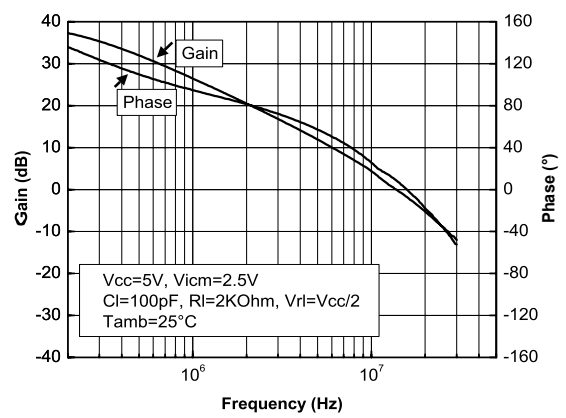


Figure 10. Positive slew rate

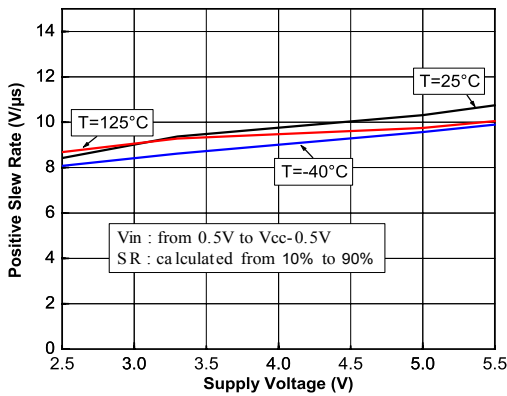


Figure 11. Negative slew rate

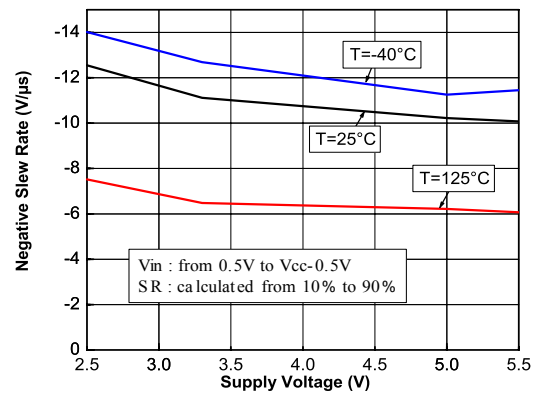


Figure 12. Distortion + noise vs. frequency

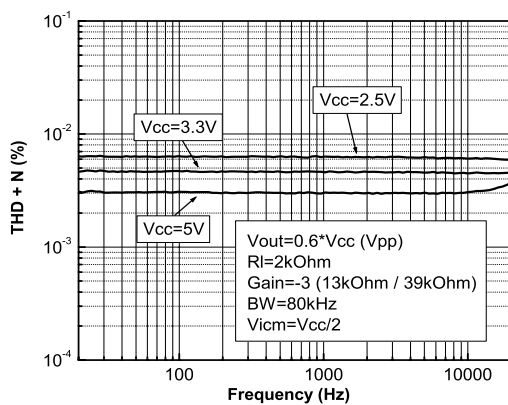


Figure 13. Distortion + noise vs. output voltage

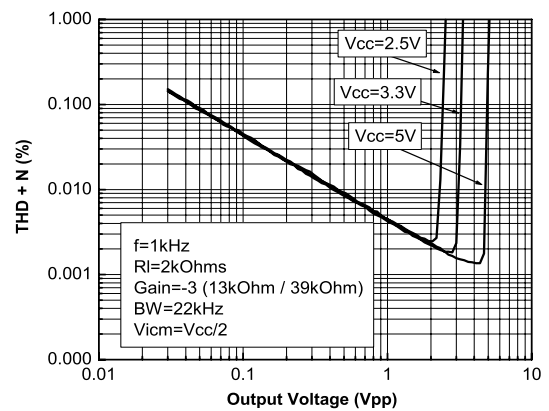


Figure 14. Noise vs. frequency

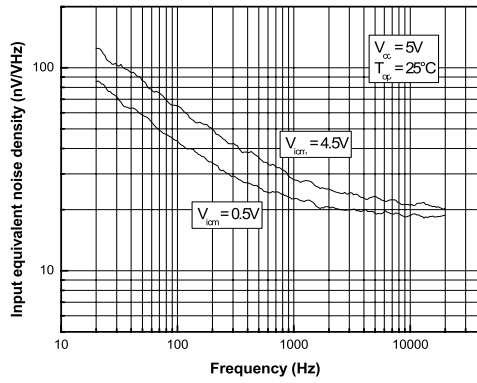
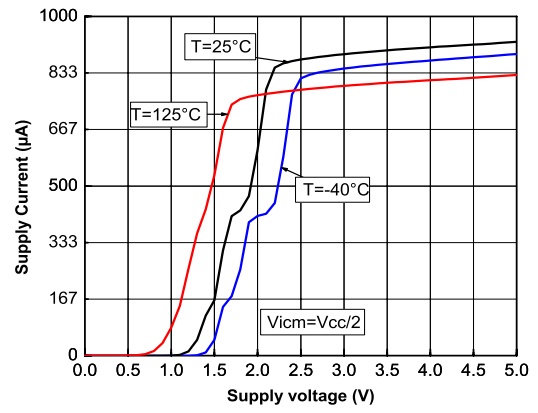


Figure 15. Supply current vs. supply voltage



5 Application information

5.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 k Ω .

The TSV99x products are not unity gain stable. To ensure proper stability they must be used in a gain configuration, with a minimum gain of -3 or 4.

However, they can be used in a “*follower*” configuration by adding a small, in-series resistor at the output, which drastically improves the stability of the device (Figure 16 shows the recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on the bench and simulated with the simulation model.

Another way to improve stability and reduce peaking is to add a capacitor in parallel with the feedback resistor. As shown in Figure 17, the feedback capacitor drastically reduces the peaking versus capacitive load (inverting gain configuration, gain = -2).

Figure 16. In-series resistor vs. capacitive load when TSV99x is used in follower configuration

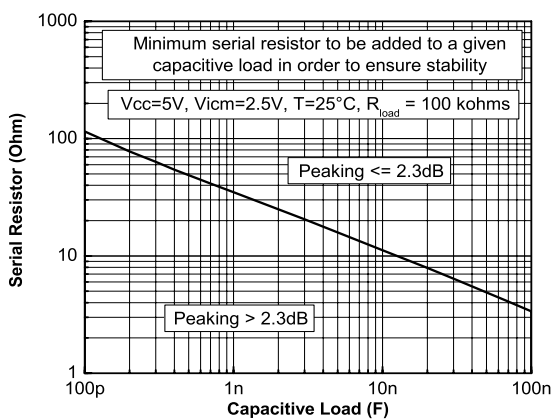
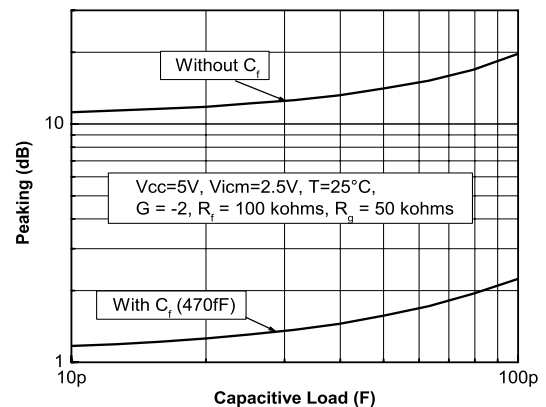


Figure 17. Peaking versus capacitive load, with or without feedback capacitor in inverting gain configuration



5.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

5.3 Macromodel

An accurate macromodel of the TSV99x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV99x operational amplifiers. It emulates the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, however, it does not replace on-board measurements.



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 18. SOT23-5 package outline

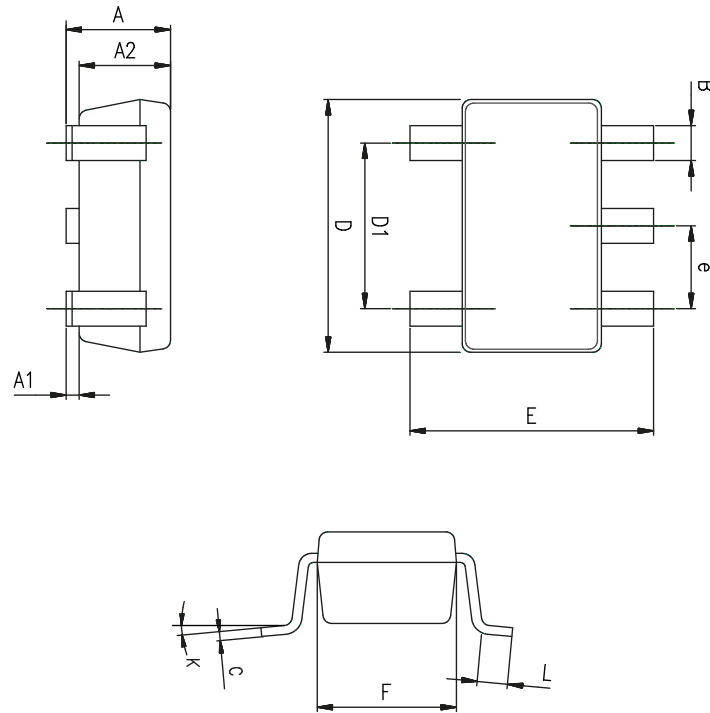


Table 6. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 DFN8 2 x 2 package information

Figure 19. DFN8 2 x 2 package outline

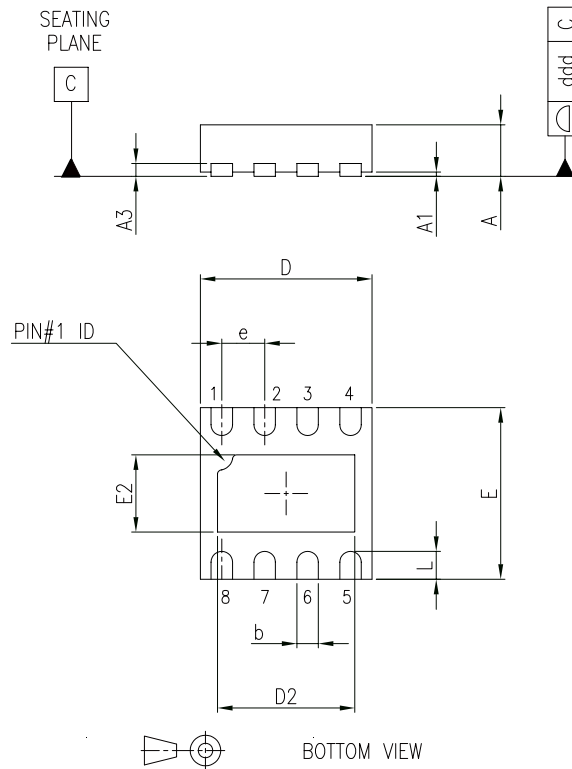
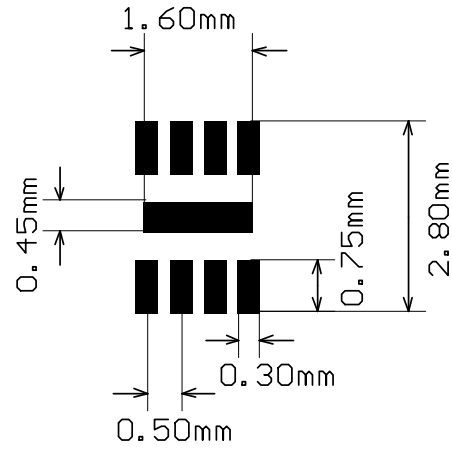


Table 7. DFN8 2 x 2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.425			0.017
ddd			0.08			0.003

Figure 20. DFN8 2 x 2 recommended footprint



Note: The exposed pad of the DFN8 2x2 package is not internally connected. It can be set to V_{CC^-} or left floating.

6.3 DFN6 1.3 x 1.6 x 0.55 package information

Figure 21. DFN6 1.3 x 1.6 x 0.55 package outline

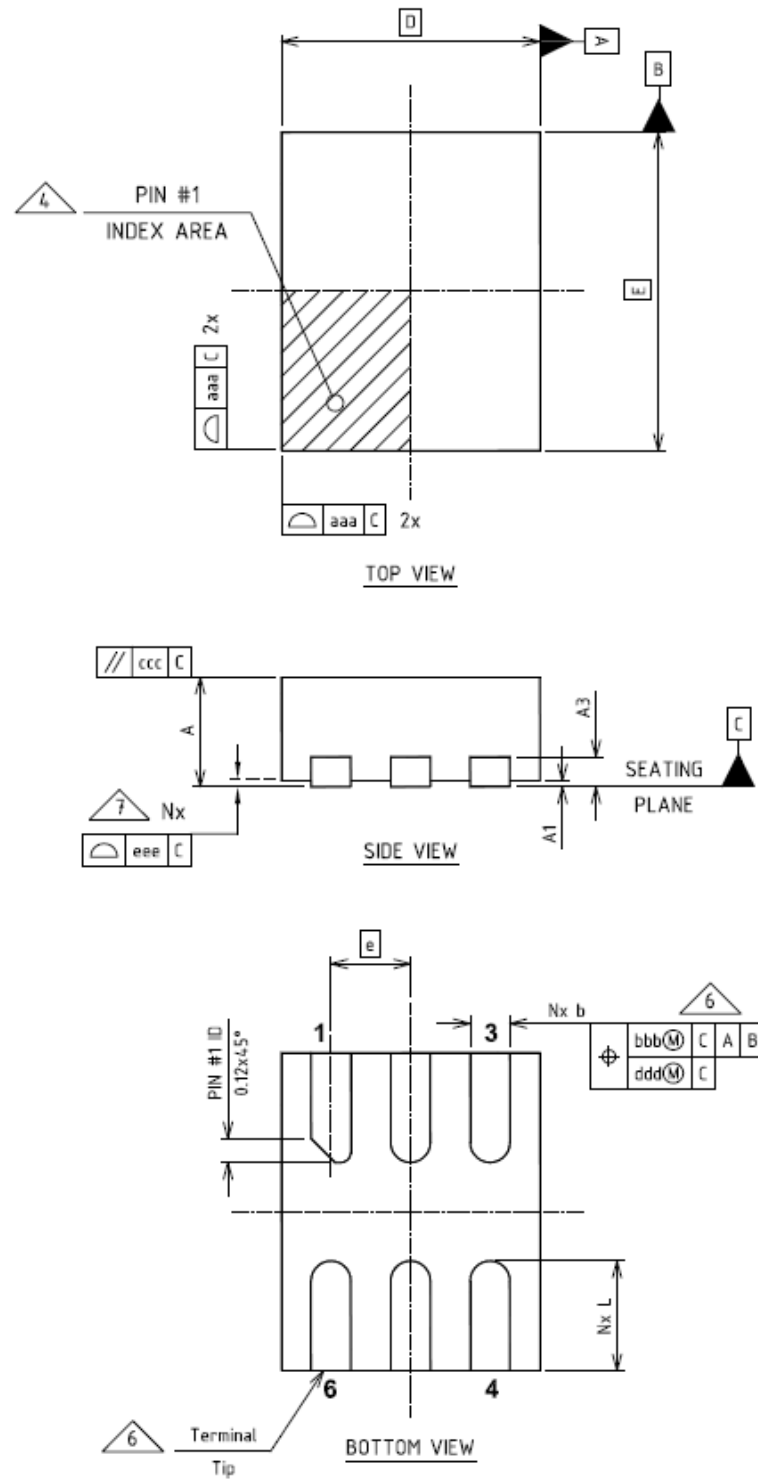
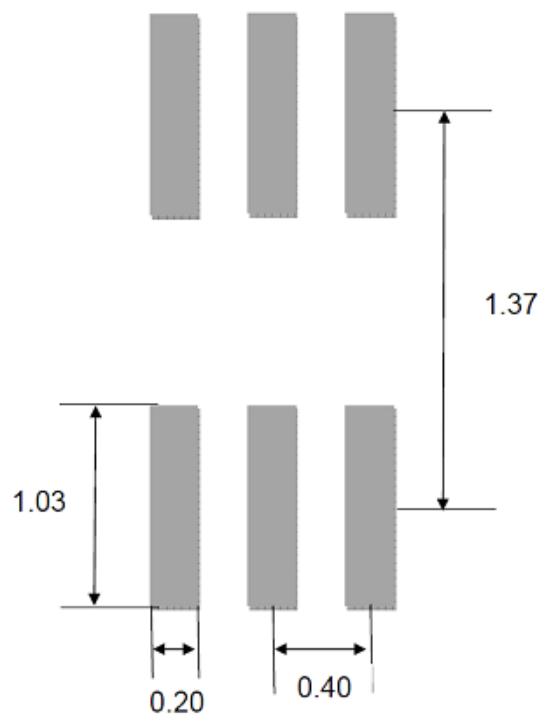


Table 8. DFN6 1.3 x 1.6 x 0.55 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.15			0.006	
B	0.15	0.20	0.25	0.006	0.008	0.010
D		1.30			0.051	
E		1.60			0.063	
e		0.40			0.016	
L	0.453	0.553	0.653	0.018	0.022	0.026
N		6			0.236	
aaa		0.05			0.002	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	

Figure 22. DFN6 1.3 x 1.6 x 0.55 recommended footprint



6.4 MiniSO8 package information

Figure 23. MiniSO8 package outline

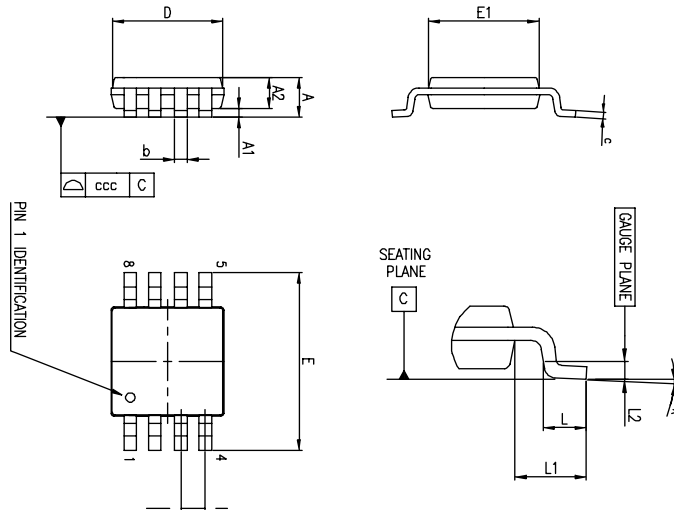


Table 9. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.5 SO8 package information

Figure 24. SO8 package outline

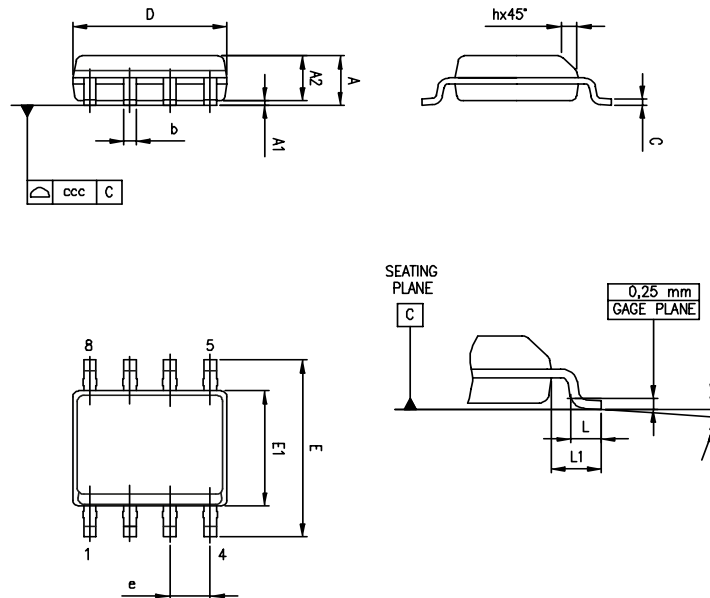


Table 10. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.6 SO-14 package information

Figure 25. SO-14 package outline

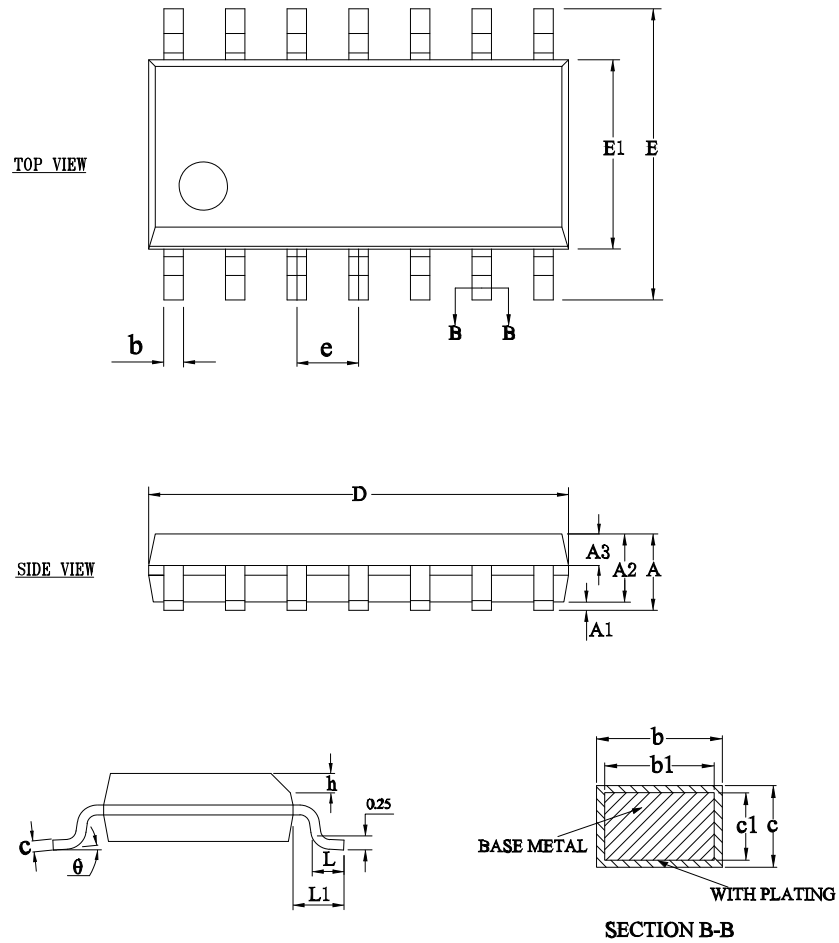
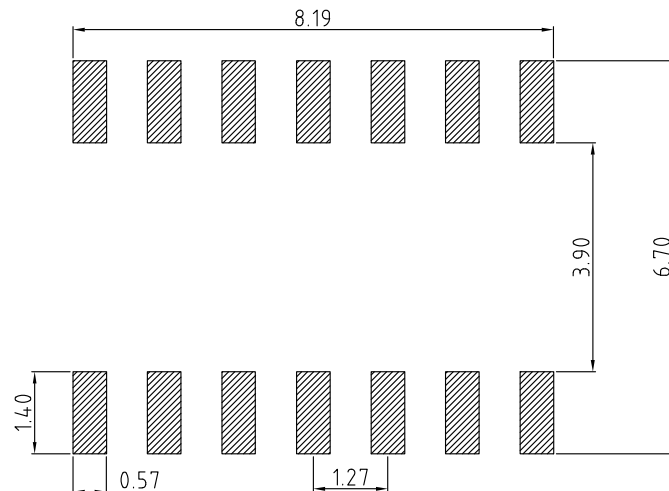


Table 11. SO-14 package mechanical data

Dim.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.225	0.004		0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.39		0.47	0.015		0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20		0.24	0.008		0.009
c1	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	8.55	8.65	8.75	0.337	0.341	0.344
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.50		0.80	0.020		0.031
L1	1.05 REF			0.041 REF		
θ	8° (max)					

Figure 26. SO-14 recommended footprint


6.7 TSSOP-14 package information

Figure 27. TSSOP-14 package outline

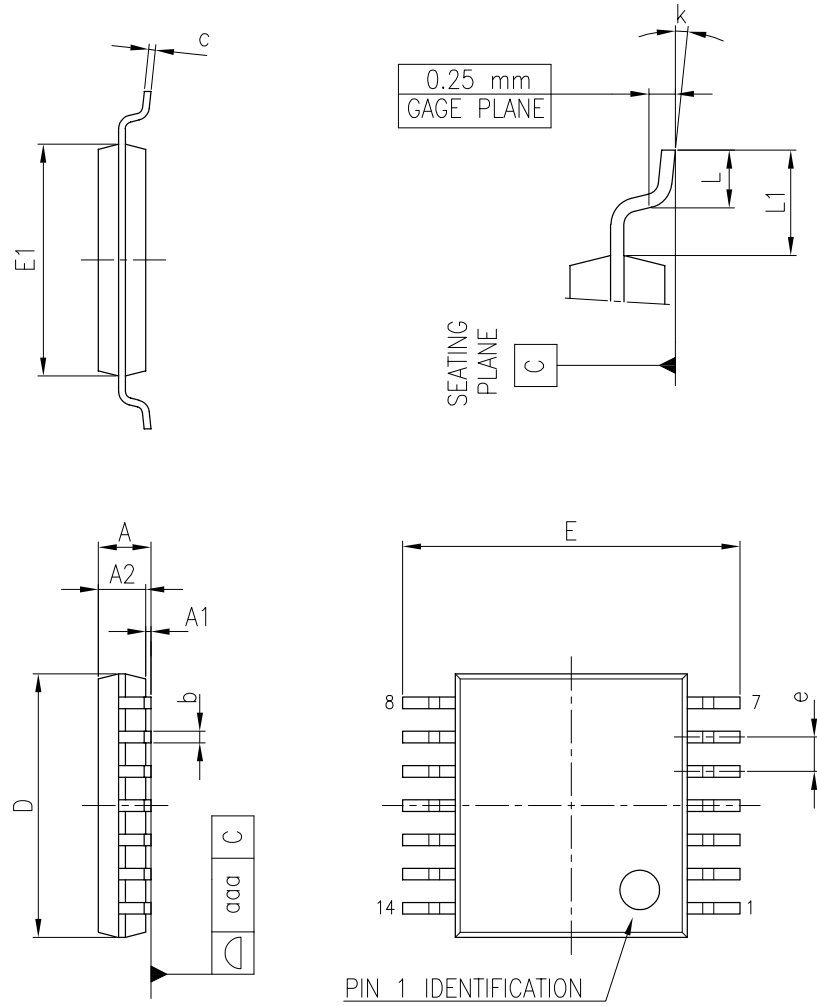
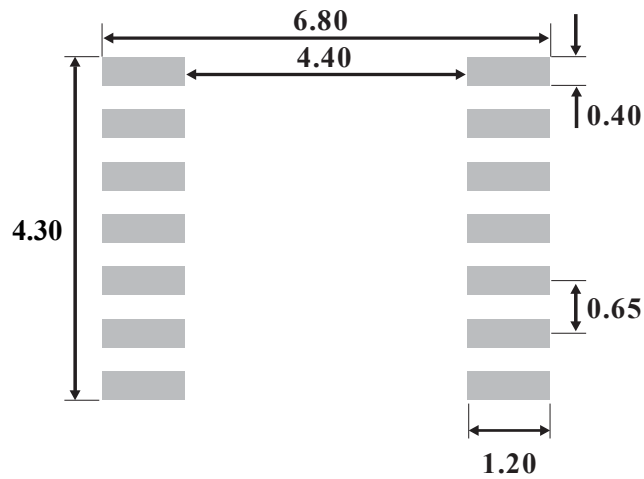


Table 12. TSSOP-14 package mechanical data

Dim.	Dimension					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.25 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	8° (max)					
aaa			0.10			0.004

Figure 28. TSSOP-14 recommended footprint



7 Ordering information

Table 13. Order code

Order code	Temperature range	Package	Packing	Marking
TSV991ILT	-40 °C to 125 °C	SOT23-5	Tape and reel	K130
TSV991AILT				K129
TSV991IQ2T		DFN8 2x2		K1F
TSV991AIQ2T				K1E
TSV991AIQ1T		DFN6 1.3x1.6x0.55		K5
TSV992IST		MiniSO8		K132
TSV992AIST				K135
TSV992IDT		SO8		V992I
TSV992AIDT		DFN8 2x2		V992AI
TSV992IQ2T				K38
TSV994IPT		TSSOP14		V994I
TSV994AIPT				V994AI
TSV994IDT		SO14		V994I
TSV994AIDT				V994AI
TSV991IYLT	-40 °C to 125 °C automotive grade ⁽¹⁾	SOT23-5	K149	
TSV991AIYLT			K150	
TSV991IYDT		SO8	V991IY	
TSV991AIYDT			V991AY	
TSV992IYDT		MiniSO8	V992IY	
TSV992AIYDT			V992AY	
TSV992IYST		SO14	K149	
TSV992AIYST			K150	
TSV994IYDT		TSSOP14	V994IY	
TSV994AIYDT			V994AIY	
TSV994IYPT		TSSOP14	V994IY	
TSV994AIYPT			V994AY	

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

Note: In the table above, all packages except the SO14 are "moisture sensitivity level 1" as per JEDEC J-STD-020-C. SO14 is JEDEC level 3.



Revision history

Table 14. Document revision history

Date	Revision	Changes
10-Mar-2014	10	Table 13: "Order codes": added new commercial product TSV991AIQ2T; corrected "Marking" error for TSV991IQ2T from K1E to K1F.
12-Jun-2015	11	Added DFN6 1.3 x 1.6 x 0.55 package for new order code TSV991AIQ1T. Updated "L" dimension of Section 4: "DFN8 2 x 2 mm (NB) package information". Updated min "k" value of Section 4.5: "SO8 package information".
27-Nov-2015	12	Table 3, Table 4, and Table 5: modified that $R_L = 600 \Omega$ (not 600 k Ω) for the high-level and low-level output voltage parameters. Section 5.2: updated name of package and titles of drawings and table; added note about exposed pad. Section 5.3: updated name of package.
03-Apr-2018	13	Updated cover image and Table 13. Order code.
19-Jun-2019	14	Updated the related product table in cover page.
14-Sep-2022	15	Updated figure on the cover page. Added TSV991IYDT and TSV991AIYDT new order codes in Table 13. Order code .
14-Mar-2023	16	Updated title, figure and related products on the cover page. Added ESD value for DFN6 in Table 1 and new Section 1 Package pin connections .



Contents

1	Package pin connections	2
2	Absolute maximum ratings and operating conditions	3
3	Electrical characteristics	5
4	Electrical characteristic curves	10
5	Application information	13
5.1	Driving resistive and capacitive loads	13
5.2	PCB layouts	13
5.3	Macromodel	13
6	Package information	14
6.1	SOT23-5 package information	15
6.2	DFN8 2 x 2 package information	16
6.3	DFN6 1.3 x 1.6 x 0.55 package information	18
6.4	MiniSO8 package information	20
6.5	SO8 package information	21
6.6	SO-14 package information	22
6.7	TSSOP-14 package information	24
7	Ordering information	26
	Revision history	27



List of tables

Table 1.	Absolute maximum ratings (AMR)	3
Table 2.	Operating conditions	4
Table 3.	Electrical characteristics at $V_{CC+} = 2.5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)	5
Table 4.	Electrical characteristics at $V_{CC+} = 3.3\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)	7
Table 5.	Electrical characteristics at $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)	8
Table 6.	SOT23-5 mechanical data	15
Table 7.	DFN8 2 x 2 mechanical data	16
Table 8.	DFN6 1.3 x 1.6 x 0.55 mechanical data	19
Table 9.	MiniSO8 package mechanical data	20
Table 10.	SO8 package mechanical data	21
Table 11.	SO-14 package mechanical data	23
Table 12.	TSSOP-14 package mechanical data	25
Table 13.	Order code	26
Table 14.	Document revision history	27



List of figures

Figure 1.	Pin connection (top view)	2
Figure 2.	Input offset voltage distribution at $T = 25\text{ }^{\circ}\text{C}$	10
Figure 3.	Input offset voltage distribution at $T = 125\text{ }^{\circ}\text{C}$	10
Figure 4.	Supply current vs. input common-mode voltage at $V_{CC} = 2.5\text{ V}$	10
Figure 5.	Supply current vs. input common-mode voltage at $V_{CC} = 5\text{ V}$	10
Figure 6.	Output current vs. output voltage at $V_{CC} = 2.5\text{ V}$	10
Figure 7.	Output current vs. output voltage at $V_{CC} = 5\text{ V}$	10
Figure 8.	Voltage gain and phase vs. frequency at $V_{CC} = 5\text{ V}$ and $V_{icm} = 0.5\text{ V}$	11
Figure 9.	Voltage gain and phase vs. frequency at $V_{CC} = 5\text{ V}$ and $V_{icm} = 2.5\text{ V}$	11
Figure 10.	Positive slew rate	11
Figure 11.	Negative slew rate	11
Figure 12.	Distortion + noise vs. frequency	11
Figure 13.	Distortion + noise vs. output voltage	11
Figure 14.	Noise vs. frequency	12
Figure 15.	Supply current vs. supply voltage	12
Figure 16.	In-series resistor vs. capacitive load when TSV99x is used in follower configuration	13
Figure 17.	Peaking versus capacitive load, with or without feedback capacitor in inverting gain configuration	13
Figure 18.	SOT23-5 package outline	15
Figure 19.	DFN8 2 x 2 package outline	16
Figure 20.	DFN8 2 x 2 recommended footprint	17
Figure 21.	DFN6 1.3 x 1.6 x 0.55 package outline	18
Figure 22.	DFN6 1.3 x 1.6 x 0.55 recommended footprint	19
Figure 23.	MiniSO8 package outline	20
Figure 24.	SO8 package outline	21
Figure 25.	SO-14 package outline	22
Figure 26.	SO-14 recommended footprint	23
Figure 27.	TSSOP-14 package outline	24
Figure 28.	TSSOP-14 recommended footprint	25



IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved