*Click **here** for production status of specific part numbers.*

MAX9611/MAX9612

High-Side, Current-Sense Amplifiers with 12-Bit ADC and Op Amp/Comparator

General Description

The MAX9611/MAX9612 are high-side current-sense amplifiers with an integrated 12-bit ADC and a gain block that can be configured either as an op amp or comparator, making these devices ideal for a number of industrial and automotive applications.

The high-side, current-sense amplifiers operate over a wide 0V to 60V input common-mode voltage range. The programmable full-scale voltage (440mV, 110mV, and 55mV) of these amplifiers offers wide dynamic range, accurate current measurement, and application flexibility in choosing sense resistor values. A choice of either an internal op amp or a comparator is provided to the user. The internal amplifier can be used to limit the inrush current or to create a current source in a closed-loop system. The comparator can be used to monitor fault events for fast response.

An I²C-controlled 12-bit, 500sps analog-to-digital converter (ADC) can be used to read the voltage across the sense resistor (V_{SENSE}), the input common-mode voltage (V_{RSCM}), op-amp/comparator output (V_{OUT}), op-amp/comparator reference voltage (V_{SET}), and internal die temperature. The I²C bus is compatible with 1.8V and 3.3V logic, allowing modern microcontrollers to interface to it.

The MAX9611 features a noninverting input-to-output configuration while the MAX9612 features an inverting input-to-output configuration.

The MAX9611/MAX9612 operate with a 2.7V to 5.5V supply voltage range, are fully specified over the -40°C to +125°C automotive temperature range, and are available in a 3mm x 5mm, 10-pin µMAX® package.

Applications

- Hybrid Automotive Power Supplies
- Server Backplanes
- Base-Station PA Control
- Base-Station Feeder Cable Bias-T
- Telecom Cards
- Battery-Operated Equipment

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Features

- 0V to +60V Input Common-Mode Voltage Range
- 2.7V to 5.5V Power-Supply Range, Compatible with 1.8V and 3.3V Logic
- 5µA Software Shutdown Current
- Integrated 12-Bit ADC
- 13µV Current-Sense ADC Resolution
- 500µV (max) Current-Sense ADC Input Offset Voltage
- 0.5% (max) Current-Sense ADC Gain Error
- I²C Bus with 16 Addresses
- Small, 3mm x 5mm 10-Pin µMAX Package
- -40°C to +125°C Operating Temperature Range

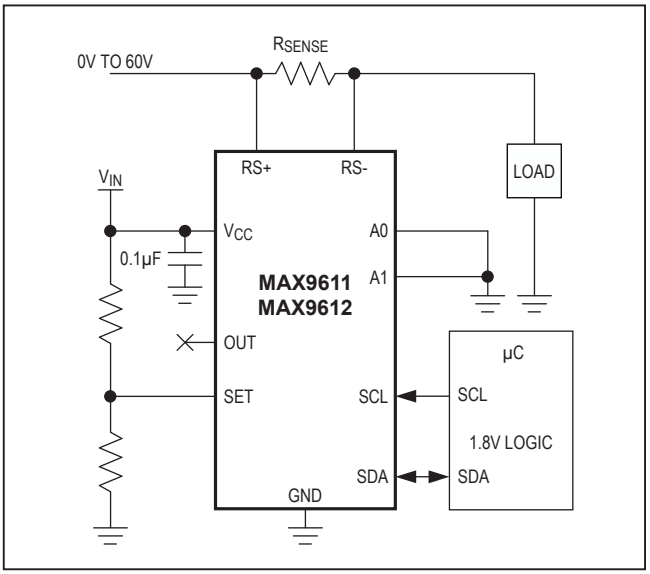
Ordering Information/Selector Guide

PART	OUTPUT	PIN-PACKAGE
MAX9611AUB+	Noninverting	10 µMAX
MAX9612AUB+	Inverting	10 µMAX

***Note:** All devices operate over the -40°C to +125°C temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Application Circuit



Functional Diagrams appear at end of data sheet.

maxim integrated™

Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +6V
RS+, RS-, OUT to GND .....-0.3V to +65V
Differential Input Voltage, RS+ - RS- .....±65V
All Other Pins to GND .....-0.3V to +6V
OUT Short-Circuit to GND.....Continuous
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 8.8mW/°C above +70°C).....707mW
µMAX Package Junction-to-Ambient
Thermal Resistance (θ_{JA}) (Note 1).....13°C/W
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 3.3V, V_{RS+} = V_{RS-} = +12V, V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER DC CHARACTERISTICS						
Input Common-Mode Range		Guaranteed by CMRR	0		60	V
Input Offset Voltage ADC Path (Note 3)	V_{OS}	T_A = +25°C, gain = 8x		0.045	0.5	mV
		T_A = -40°C to +125°C, gain = 8x			2	
		T_A = +25°C, gain = 4x		0.045	0.5	
		T_A = -40°C to +125°C, gain = 4x			2	
		T_A = +25°C, gain = 1x		0.1	0.8	
		T_A = -40°C to +125°C, gain = 1x			2.6	
Gain Error (Note 3)	GE	T_A = +25°C, gain = 8x		0.1	0.5	%
		T_A = -40°C to + 85°C, gain = 8x			1.8	
		T_A = -40°C to +125°C, gain = 8x			2.5	
		T_A = +25°C, gain = 4x		0.4	1.7	
		T_A = -40°C to +125°C, gain = 4x			3.1	
		T_A = +25°C, gain = 1x		1	4	
		T_A = -40°C to +125°C, gain = 1x			4.7	
Differential Input Resistance	R_{INDM}			300		kΩ
Common-Mode Input Resistance	R_{INCM}			12		MΩ
Input Bias Current	I_{RS+}, I_{RS-}	T_A = +25°C		1	2	µA
		T_A = -40°C to +125°C			5	
Input Offset Current (Note 4)	(I_{RS+}) - (I_{RS-})	T_A = +25°C		3	6	nA
		T_A = -40°C to +125°C			6	

Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{RS+} = V_{RS-} = +12V, V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	V_{RS-} = 0V to 60V, T_A = +25°C	Gain = 8x, V_{SENSE} = 50mV	106	120		dB
			Gain = 4x, V_{SENSE} = 100mV	106	120		
			Gain = 1x, V_{SENSE} = 400mV	100	120		
		V_{RS-} = 0V to 60V, T_A = -40°C to +125°C	Gain 8x, V_{SENSE} = 50mV	94			
			Gain 4x, V_{SENSE} = 100mV	94			
			Gain 1x, V_{SENSE} = 400mV	84			
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.5V	Gain = 8x, V_{SENSE} = 50mV	57	72		dB
			Gain = 4x, V_{SENSE} = 100mV	56	67		
			Gain = 1x, V_{SENSE} = 400mV	48	57		
Full-Scale Sense Voltage	FS	Used in gain error measurement	Gain = 8x		55		mV
			Gain = 4x		110		
			Gain = 1x		440		
LSB Step Size	LSB	Gain = 8x			13.44		µV
		Gain = 4x			26.88		
		Gain = 1x			107.50		
ANALOG PATH, CSA + AMPLIFIER/COMPARATOR							
Input Offset Voltage	V_{OS}	T_A = +25°C			0.350	4	mV
		T_A = -40°C to +125°C				10	
SET Input Bias Current	I_B				1	50	nA
Maximum SET Input Voltage Range					1.126		V
Signal Bandwidth	BW	Gain = 1x, R_{S-} = 11.6V			4		MHz
Gain Bandwidth	GBW				2.5		MHz
Propagation Delay	t_{PD}	In comparator mode, 10mV overdrive			1.5		µs
Internal Hysteresis	V_{HYS}	In comparator mode, nonlatching			8		mV
Output Sink Current		V_{OUT} = 4V			15		mA
Output Leakage Current		V_{OUT} = 36V			1.7	3	µA
Output Voltage Low	V_{OL}	I_{SINK} = 8mA, T_A = -40°C to +85°C				1	V
		I_{SINK} = 8mA, T_A = -40°C to +125°C			0.5	1.5	

Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{RS+} = V_{RS-} = +12V, V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT VOLTAGE MEASUREMENT (V_{OUT})							
Full-Scale Input Voltage					57.3		V
LSB Step Size	LSB				14		mV
Gain Error	GE	V_{RSCM} = (V_{RS+} - V_{RS-})/2	T_A = +25°C		0.8	6	%
			T_A = -40°C to +125°C			7	
Input Offset Voltage	V_{OSOUT}	T_A = +25°C			14	110	mV
		T_A = -40°C to +125°C				160	
COMMON-MODE VOLTAGE MEASUREMENT (V_{RSCM})							
Full-Scale Input Voltage					57.3		V
LSB Step Size	LSB				14		mV
Gain Error	GE	V_{RSCM} = (V_{RS+} - V_{RS-})/2	T_A = +25°C		0.3	6	%
			T_A = -40°C to +125°C			7	
Input Offset Voltage	V_{OSOUT}	T_A = +25°C			14	80	mV
		T_A = -40°C to +125°C				160	
SET VOLTAGE MEASUREMENT (V_{SET})							
Full-Scale Input Voltage					1.10		V
LSB Step Size					268		µV
Gain Error	GE	V_{RSCM} = (V_{RS+} - V_{RS-})/2	T_A = +25°C		0.2	5	%
			T_A = -40°C to +125°C			6	
Input Offset Voltage	V_{OSOUT}	T_A = +25°C			0.3	10	mV
		T_A = -40°C to +125°C				14	
Integral Nonlinearity	INL				1		LSB
Differential Nonlinearity	DNL				0.2		LSB
TEMPERATURE MEASUREMENT							
Accuracy					0.48		°C
Typical Measurement Range				-40		+125	°C
LSB Step Size	LSB				0.48		°C
ANALOG-TO-DIGITAL CONVERTER							
Resolution					12		Bit
Conversion Time					2		ms
SCL/SDA LOGIC LEVELS							
Input Voltage Low	V_{IL}	V_{CC} = 2.7V to 5.5V				0.4	V
		V_{CC} = 3.3V, T_A = +25°C				0.9	V
Input Voltage High	V_{IH}	V_{CC} = 2.7V to 5.5V		1.45			V
Input Hysteresis	V_{HYS}				0.05 x V_{CC}		V
Input Leakage Current					1	200	nA
A1/A0 LOGIC LEVELS							
Logic State 00-01 Threshold					1/4 x V_{CC}		V
Logic State 01-10 Threshold					1/2 x V_{CC}		V
Logic State 10-11 Threshold					3/4 x V_{CC}		V
Input Leakage Current					1	200	nA

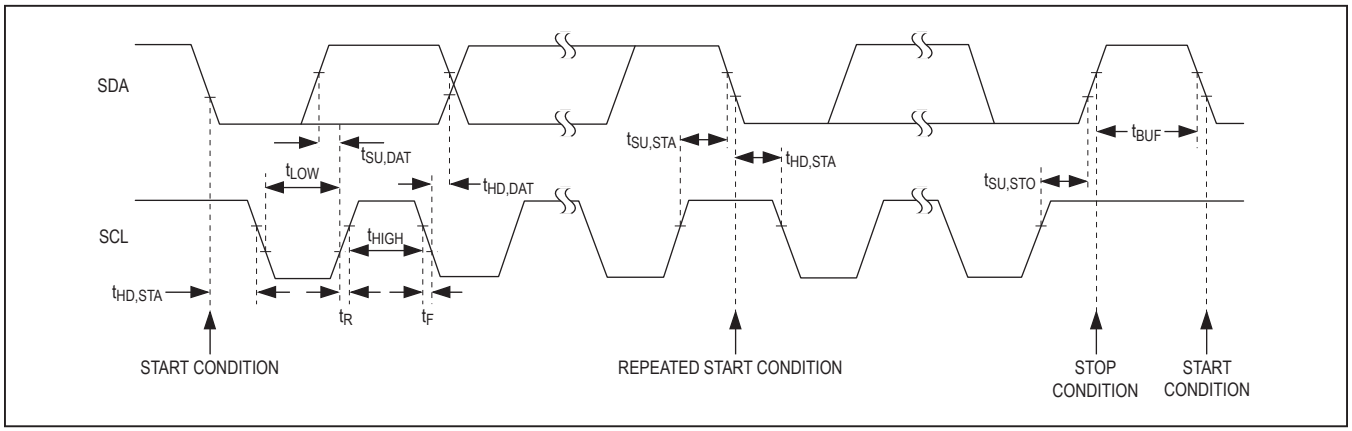
Electrical Characteristics (continued)

(V_{CC} = 3.3V, V_{RS+} = V_{RS-} = +12V, V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY CHARACTERISTICS						
Power-Supply Input Range	V_{CC}	Guaranteed by PSRR	2.7		5.5	V
Quiescent Current	I_{CC}			1.6	2.6	mA
Shutdown Current	I_{SHDN}	No activity on SCL		5	10	µA
I²C TIMING CHARACTERISTICS (COMPATIBLE WITH SMBus)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time, (Repeated) START Condition	$t_{DH,STA}$		0.6			µs
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{DH,DAT}$		0		900	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA/SCL Receiving Rise Time	t_R	(Note 5)	20 + 0.1C_B		300	ns
SDA/SCL Receiving Fall Time	t_F	(Note 5)	20 + 0.1C_B		300	
SDA Transmitting Fall Time	t_F	(Note 5)	20 + 0.1C_B		250	
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}			50		ns

Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: V_{OS} and gain error of current-sense amplifier extrapolated from a two-point measurement made at V_{SENSE} = (V_{RS+} - V_{RS-}) = 5mV to 50mV in gain of 8x, 5mV to 100mV in gain of 4x, and 10mV to 400mV in gain of 1x.
Note 4: Guaranteed by design.
Note 5: C_B is in pF.

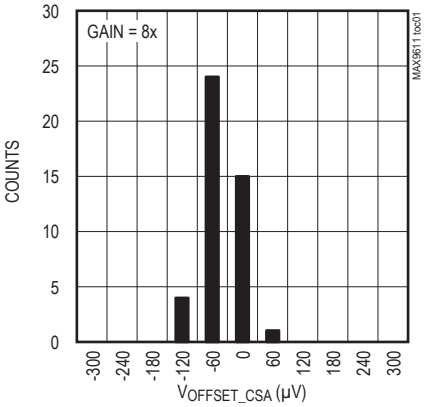
I²C Timing Diagram



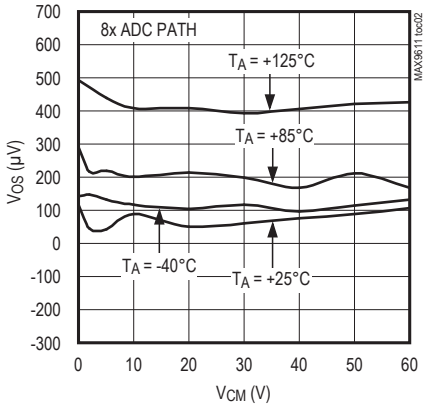
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{CM} = 12V, T_A = +25°C, unless otherwise noted.)

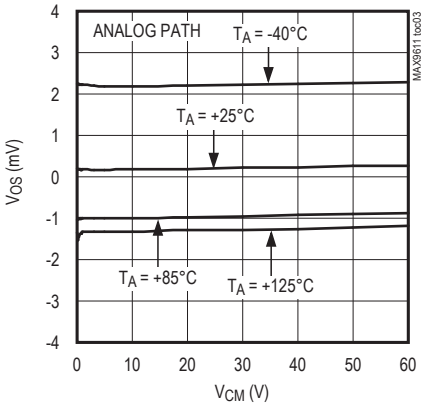
CSA HISTOGRAM



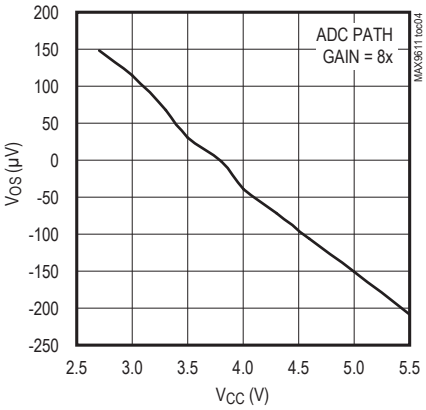
MAX9611 CSA OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



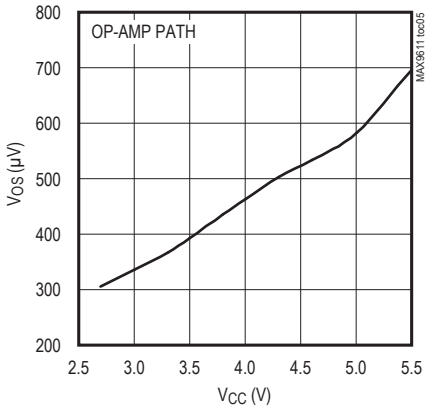
TOTAL OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



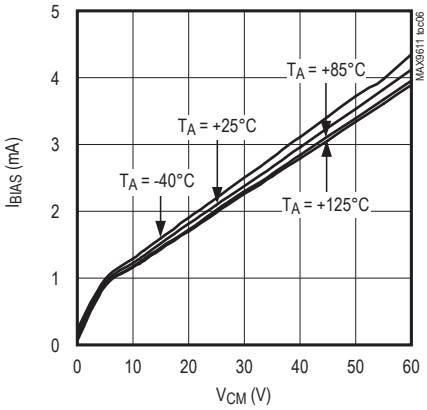
CSA OFFSET VOLTAGE vs. SUPPLY VOLTAGE



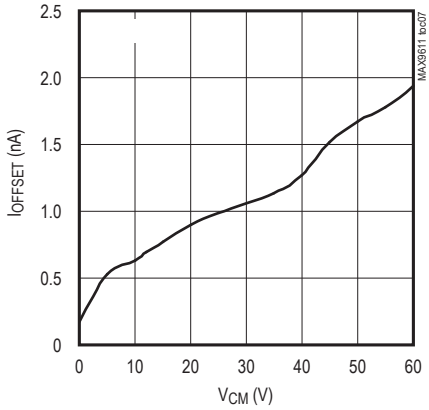
TOTAL OFFSET VOLTAGE vs. SUPPLY VOLTAGE



RS- BIAS CURRENT vs. COMMON-MODE VOLTAGE



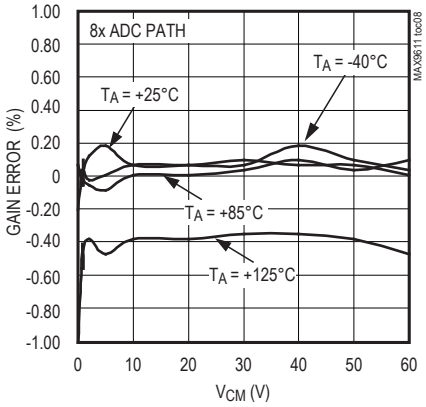
RS+, RS- OFFSET CURRENT vs. COMMON-MODE VOLTAGE



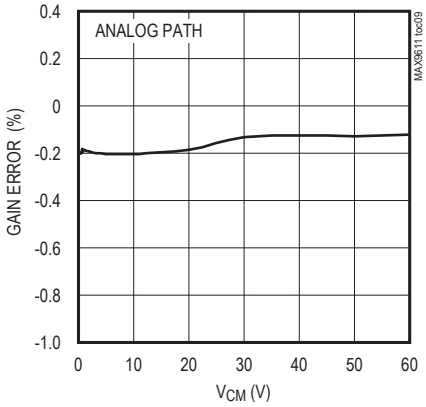
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 12V, T_A = +25°C, unless otherwise noted.)

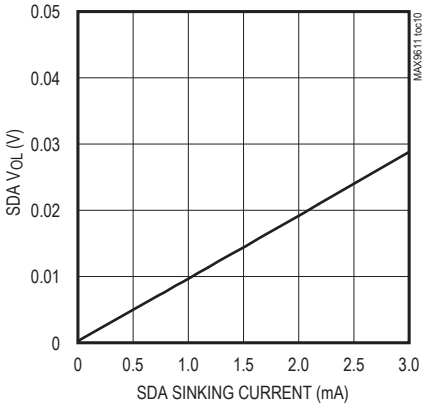
MAX9611 CSA GAIN ERROR vs. COMMON-MODE VOLTAGE



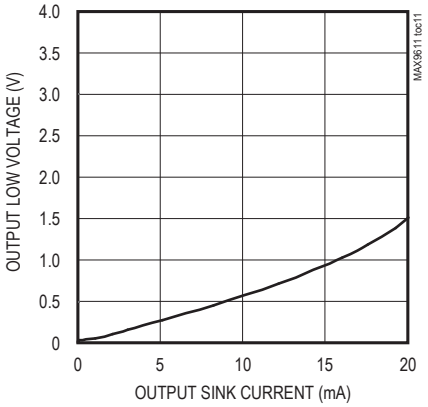
TOTAL GAIN ERROR vs. COMMON-MODE VOLTAGE



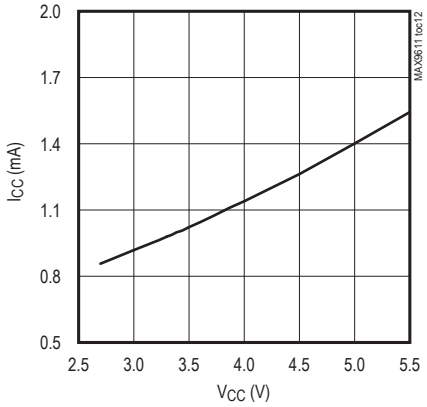
SDA/SCL V_{OL} vs. SINKING CURRENT



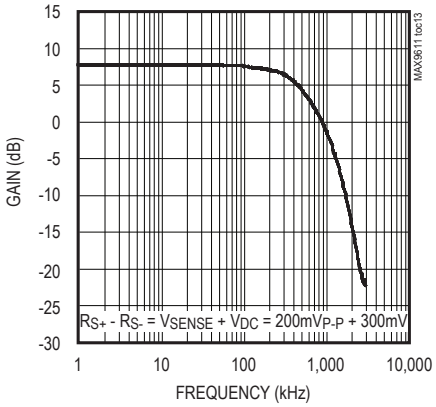
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



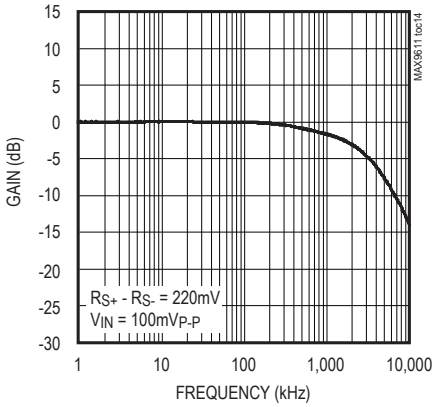
SUPPLY CURRENT vs. SUPPLY VOLTAGE



CSA GAIN vs. FREQUENCY (RS+/RS- TO OUT PATH)



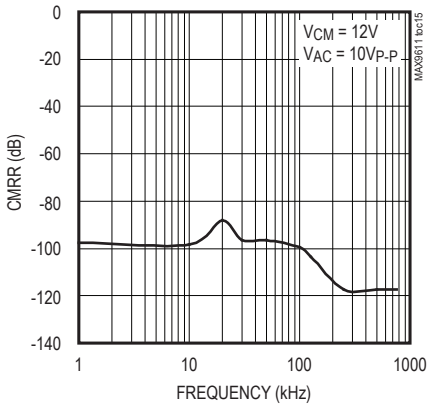
OP-AMP GAIN vs. FREQUENCY (SET TO OUT)



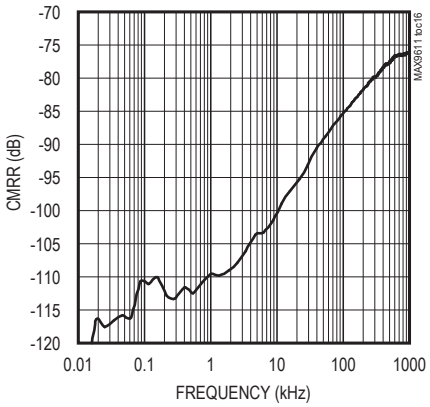
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 12V, T_A = +25°C, unless otherwise noted.)

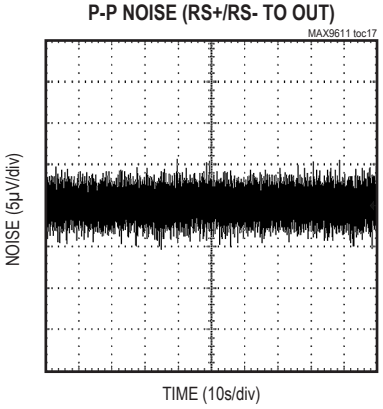
CMRR vs. FREQUENCY CSA ADC PATH



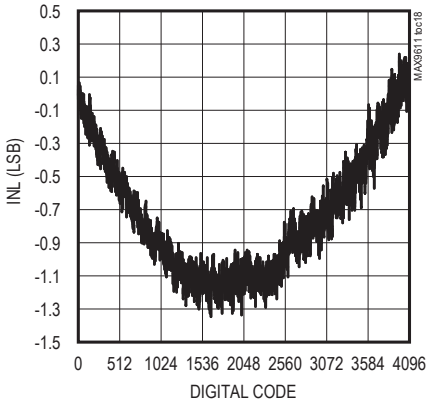
CMRR vs. FREQUENCY ANALOG OP-AMP PATH



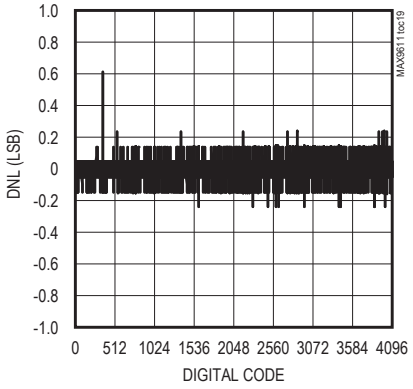
P-P NOISE (RS+/RS- TO OUT)



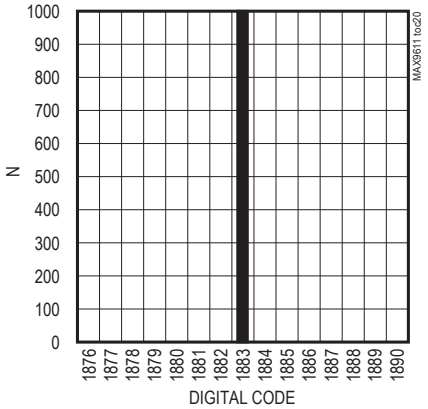
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (SET INPUT)



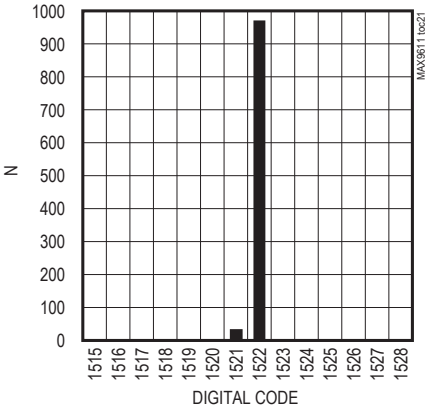
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (SET INPUT)



ADC NOISE HISTOGRAM ON V_{SET} = 0.5V



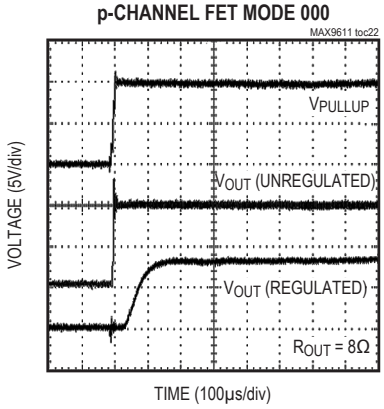
ADC NOISE HISTOGRAM ON V_{SENSE} = 20mV (GAIN = 8x)



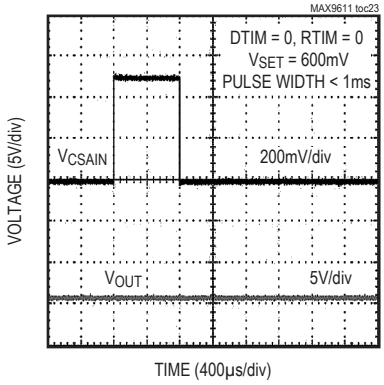
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 12V, T_A = +25°C, unless otherwise noted.)

HOT-SWAP OPERATION WITH p-CHANNEL FET MODE 000



WATCHDOG LATCH RETRY MODE 111



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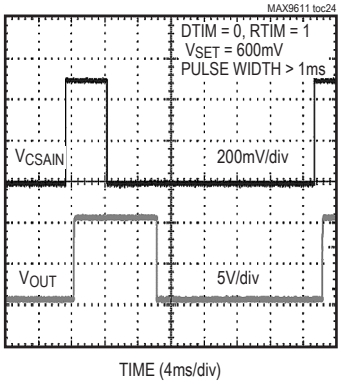

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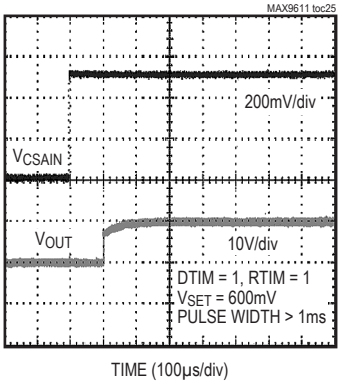

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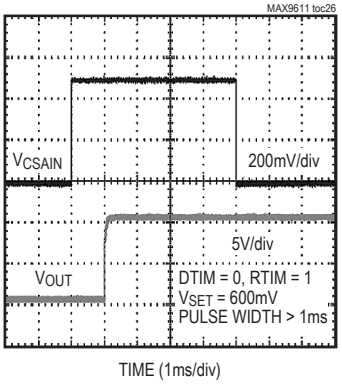

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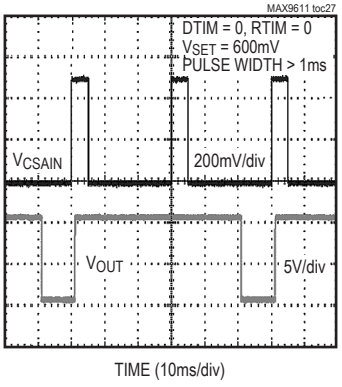
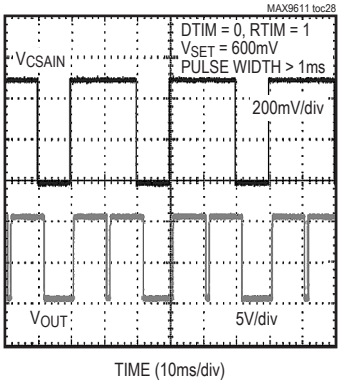
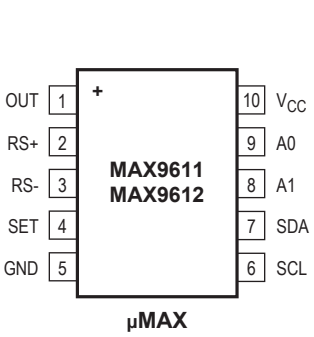


WATCHDOG LATCH RETRY MODE 111



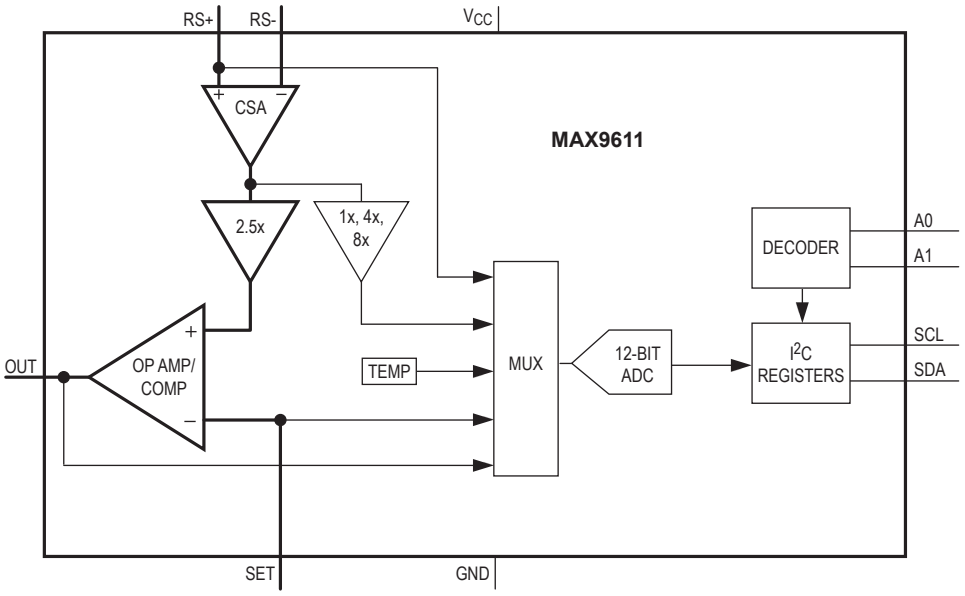
Pin Configuration

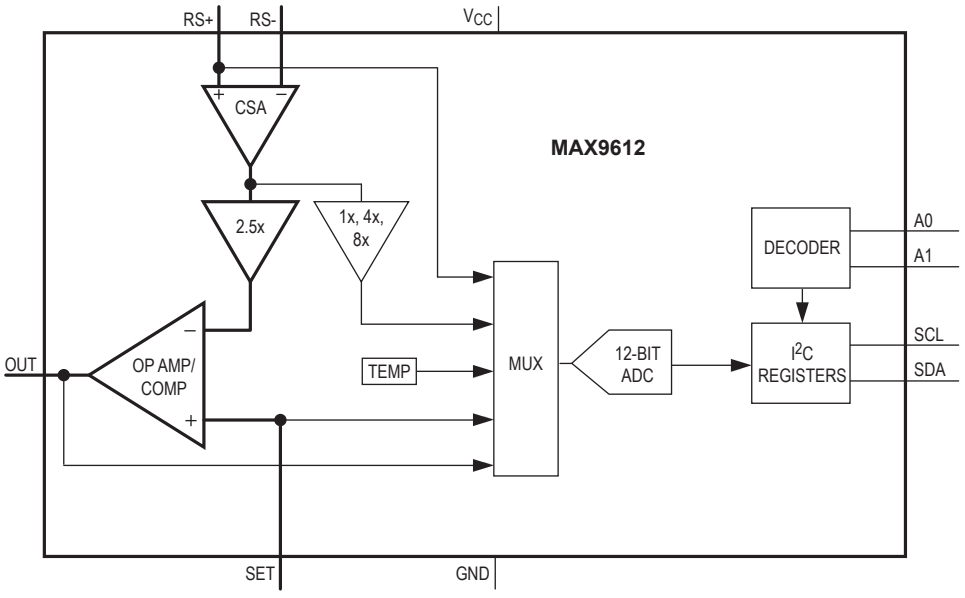


Pin Description

PIN	NAME	FUNCTION
1	OUT	Internal Amplifier/Comparator Output
2	RS+	Positive Current-Sensing Input. Power side connects to external sense resistor.
3	RS-	Negative Current-Sensing Input. Load side connects to external sense resistor.
4	SET	External Set-Point Voltage
5	GND	Ground
6	SCL	I^2C Interface Clock Input
7	SDA	I^2C Interface Data Input/Output
8	A1	Address Input 1
9	A0	Address Input 0
10	V_{CC}	Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF and a 4.7µF capacitor in parallel.

Functional Diagrams





NOTE: ANALOG PATH IN BOLD.

Detailed Description

The MAX9611/MAX9612 are high-side, current-sense amplifiers with an integrated 12-bit ADC and an internal selectable op amp/comparator. These devices are ideal for a variety of industrial and automotive applications.

The MAX9611/MAX9612's high-side, current-sense amplifiers operate over a wide 0V to 60V input common-mode voltage range. The programmable full-scale voltage (440mV, 110mV, and 55mV) allows for a wide dynamic range current measurement and application flexibility in choosing sense resistor values.

The I^2C bus is 1.8V and 3.3V logic compatible and can interface with modern microcontrollers. An internal 12-bit, 500sps integrating analog-to-digital converter (ADC) allows the user to read analog signals such as die temperature, V_{OUT}, V_{SET}, V_{RSCM}, and V_{SENSE}.

At power-up, the selectable op-amp/comparator block is configured in the op-amp mode. The op amp has an effective 60V Class A-type output stage and can be used to limit inrush currents and create a current source when used in a closed-loop system. When the internal comparator is selected, the MAX9611/MAX9612 can be configured to have a latched and retry functionality, allowing a 60V open-drain transistor output, ideal to operate high-side relay-disconnect FETs. The MAX9611 has a noninverting input-to-output configuration while the MAX9612 has an inverting input-to-output configuration.

Current-Sense Amplifier

The MAX9611/MAX9612 feature a precision current-sense amplifier with a 0V to 60V input common-mode voltage range. An internal negative charge pump eliminates input stage crossover distortion, typical in most rail-to-rail input current-sense amplifiers. Low input bias currents and low input offset currents allow a wide selection of input filters to be designed without degrading the accuracy of the current-sense amplifier.

The current-sense amplifier inputs feature both a -0.3V/+65V common-mode absolute maximum rating as well as a ±65V differential absolute maximum rating, allowing a wide variety of fault conditions to be withstood easily by the device without damage.

The current-sense amplifier has a gain of 2.5V/V and connects directly to the output op-amp/comparator inputs. The ADC path features a 1x, 4x, and 8x programmable gain providing for 440mV, 110mV, and 55mV full-scale sense voltage.

Analog-to-Digital Converter (ADC)

The MAX9611/MAX9612 feature an internal dual-slope integrating 12-bit ADC that has a 2ms conversion time and a 1.8V and 3.3V logic-compatible I^2C bus. An internal mux allows the following on-chip variables to be read: input sense voltage, input common-mode voltage, SET voltage, OUT voltage, and die temperature.

Temperature Measurement

Die temperature can be read by the ADC over the entire operating range (-40°C to +125°C) with 0.5°C resolution. Die temperature can be used for application calibration and thermal monitoring and is available in a 9-bit, two's complement format. Readings outside of normal operating temperature range (-40°C to +125°C) are inaccurate and should be considered invalid. See Table 1 for binary and hex values.

Table 1. Binary and Hex Digital Output Values for Temperature Measurements

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
+122.4	0111 1111 1xxx xxxx	7F8x
+24	0001 1001 0xxx xxxx	190x
+0.48	0000 0000 1xxx xxxx	008x
0	0000 0000 0xxx xxxx	000x
-0.48	1111 1111 1xxx xxxx	FF8x
-24	1110 0111 0xxx xxxx	E70x
-40	1101 1001 1xxx xxxx	D98x

SET Voltage Measurement

The SET voltage serves as a reference voltage for the internal op amp or comparator around which a control loop can be designed. The low bias current for SET allows high-impedance resistor-dividers and current output DACs to be used, making it easy to interface without introducing additional errors.

The SET input can also serve as an auxiliary input port to the ADC if the op amp or comparator is not utilized in the application. Its full-scale input range extends from 0V to 1.10V.

OUT Voltage Measurement

The internal amplifier/comparator output voltage can be monitored over the entire 0V to 57.3V range by the ADC. An internal high-value resistor-divider on OUT reduces leakage current effects.

Common-Mode Voltage Measurement

The input common-mode voltage is defined as the average of the voltage at RS+ and RS-. A high-value resistor-divider allows measurement of the input common-mode voltage over the 0V to 57.3V range.

Sense Voltage Measurement

Three programmable gains allow for a wide range of currents to be read by the ADC. The current-sense amplifier gain can be set to 1x, 4x, or 8x. The full-scale sense voltages are then 440mV, 110mV, and 55mV, respectively.

Output Amplifier/Comparator

The MAX9611/MAX9612 feature an internally selectable op amp and comparator where one of the inputs is connected to the 2.5x current-sense amplifier, and the other input is connected to the SET input. The op amp or the comparator output can be selected and connected to OUT. The output stage is an open-drain 60V nFET, that requires a suitable pullup resistor for proper operation. The op amp then behaves like a Class-A output stage. Select op amp or comparator function in Control Register 1 (0x0A) bit 7 (see Tables 4 and 5).

Watchdog/Latch/Retry Functionality

Internal digital circuitry is used to implement a watchdog feature that can be useful to handle normal application transients that are not true fault conditions. This feature applies both to the op amp and comparator modes of part operation. A watchdog delay time is internally set to 1ms by default but can be changed to 100µs. The retry delay time is internally set to 50ms by default, but can be changed to 10ms (see Tables 6 and 7).

In normal operation mode, (Control Register 1 (0x0A) 000x xxxx), the amplifier output responds to the difference between its inputs, i.e., the CSA output voltage and the SET voltage. In open-loop configuration, the op amp can be used as a comparator.

In a watchdog-latch-retry mode (Control Register 1 (0x0A) 111x xxxx), the output of the comparator waits for a watchdog delay time (to ensure the CSA output continues to stay above the SET voltage for this duration) before responding, and then latches onto this state. After a retry delay time, it resets the comparator state and the cycle repeats.

Similar functionality is implemented for the op-amp mode as well (Control Register 1 (0x0A) 000x xxxx to 011x xxxx).

A RESET bit is defined in Control Register 1 (0x0A) to reset a latched state when commanded by the user.

I²C Interface

The MAX9611/MAX9612 I²C interface consists of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX9611/MAX9612 and the master at rates up to 400kHz. The MAX9611/MAX9612 are slave devices that transfer and receive data. The master (typically a microcontroller) initiates data transfer on the bus and generates the SCL signal to permit that transfer.

Slave Address

A bus master initiates communication with a slave device by issuing a START (S) condition followed by a slave address. When idle, the MAX9611/MAX9612 continuously wait for a START condition followed by their slave address. When the MAX9611/MAX9612 recognize a slave address, it is ready to accept or send data. The MAX9611/MAX9612 offer 16 different slave addresses using two address inputs, A1 and A0. See Table 2 for different slave address options. The least significant bit (LSB) of the address byte (R/W) determines whether the master is writing to or reading from the MAX9611/MAX9612 (R/W = 0 selects a write condition, R/W = 1 selects a read condition). After receiving the address, the MAX9611/MAX9612 (slave) issue an acknowledge by pulling SDA low for one clock cycle.

I²C Write Operation

A write operation (Figure 1) begins with the bus master issuing a START condition followed by seven address bits and a write bit (R/W = 0). If the address byte is successfully received, the MAX9611/MAX9612 (slave) issue an acknowledge (A). The master then writes to the slave and the sequence is terminated by a STOP (P) condition for a single write operation.

For a burst write operation, more data bytes are sent after the register address before the transaction is terminated.

Table 2. MAX9611/MAX9612 Address Description

A1	A0	DEVICE WRITE ADDRESS (hex)	DEVICE READ ADDRESS (hex)
0	0	0xE0	0xE1
0	1/3 x V_{CC}	0xE2	0xE3
0	2/3 x V_{CC}	0xE4	0xE5
0	V_{CC}	0xE6	0xE7
1/3 x V_{CC}	0	0xE8	0xE9
1/3 x V_{CC}	1/3 x V_{CC}	0xEA	0xEB
1/3 x V_{CC}	2/3 x V_{CC}	0xEC	0xED
1/3 x V_{CC}	V_{CC}	0xEE	0xEF
2/3 x V_{CC}	0	0xF0	0xF1
2/3 x V_{CC}	1/3 x V_{CC}	0xF2	0xF3
2/3 x V_{CC}	2/3 x V_{CC}	0xF4	0xF5
2/3 x V_{CC}	V_{CC}	0xF6	0xF7
V_{CC}	0	0xF8	0xF9
V_{CC}	1/3 x V_{CC}	0xFA	0xFB
V_{CC}	2/3 x V_{CC}	0xFC	0xFD
V_{CC}	V_{CC}	0xFE	0xFF

I²C Read Operation

In an I²C read operation (Figure 2), the bus master issues a write command first by initiating a START condition followed by seven address bits, a write bit (R/W = 0) and the 8-bit register address. The master then issues a Repeated START (Sr) condition, followed by seven address bits, a read bit (R/W = 1). If the address byte is successfully received, the MAX9611/MAX9612 (slave) issue an acknowledge (A). The master then reads from the slave. For continuous read, the master issues an acknowledge bit (AM) after each received byte. The master terminates the read operation by sending a not acknowledge (NA) bit. The MAX9611/MAX9612 then release the data line SDA allowing the master to generate a STOP condition.

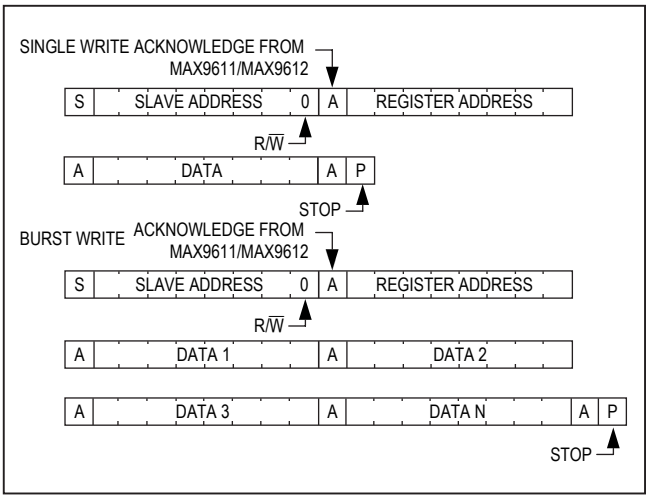


Figure 1. I²C Write Operation

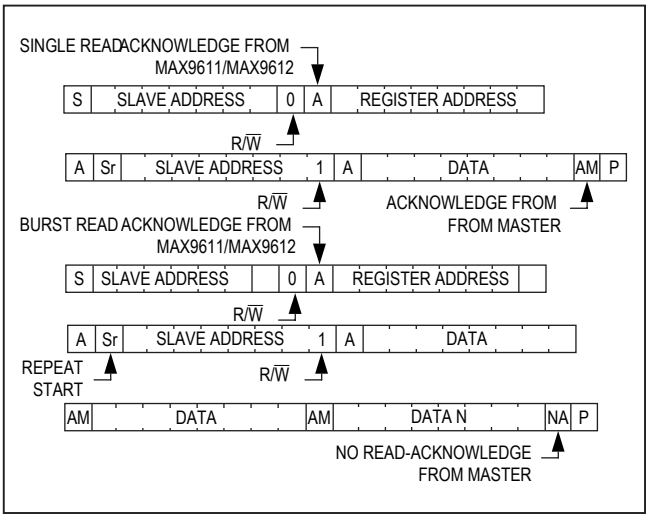


Figure 2. I²C Read Operation

Registers

The MAX9611/MAX9612 include five 12-bit data register banks and two 8-bit control registers.

The two control registers are read/write registers used to configure the ADC for different modes of operation.

Table 3 lists all the registers, their corresponding POR values and their addresses.

Table 3. Internal Register/Addresses

REGISTERS	POR VALUES (hex)	REGISTER ADDRESS (hex)
CSA DATA BYTE 1 (MSBs)	0x000	0x00
CSA DATA BYTE 1 (LSBs)	0x000	0x01
RS+ DATA BYTE 1 (MSBs)	0x000	0x02
RS+ DATA BYTE 1 (LSBs)	0x000	0x03
OUT DATA BYTE 1 (MSBs)	0x000	0x04
OUT DATA BYTE 1 (LSBs)	0x000	0x05
SET DATA BYTE 1 (MSBs)	0x000	0x06
SET DATA BYTE 1 (LSBs)	0x000	0x07
TEMP DATA BYTE 1 (MSBs)	0x800	0x08
TEMP DATA BYTE 1 (LSBs)	0x000	0x09
CONTROL REGISTER 1	0x000	0x0A
CONTROL REGISTER 2	0x000	0x0B

Data Registers

The five 12-bit data registers banks comprise two 8-bit registers for 8 MSBs and 4 LSBs. The 12-bit data is split between the two 8-bit data bytes as seen in Figure 1. They are read-only registers that hold the converted data. Do not issue a STOP command until both bytes are read. Instead use a Repeated START command to read the second byte.

Byte 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MSB12	MSB11	MSB10	MSB09	MSB08	MSB07	MSB06	MSB05

Byte 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LSB05	LSB03	LSB02	LSB01	0	0	0	0

Control Register 1

Control Register 1 is an 8-bit write/read register that configures the MAX9611/MAX9612 for different modes of operation. Tables 4 and 5 show the bit location and function for Control Register 1.

Table 4. Control Register 1 Bit Location

BIT NUMBER	7	6	5	4	3	2	1	0
BIT NAME	MODE2	MODE1	MODE0	LR	SHDN	MUX2	MUX1	MUX0
POR VALUE	0	0	0	0	0	0	0	0

Table 5. Control Register 1 Bit Description

BIT	BIT NAME	FUNCTION
2, 1, 0	MUX2, MUX1, MUX0	000 Channel A: Read current-sense amplifier output from ADC, gain = 1x 001 Channel A: Read current-sense amplifier output from ADC, gain = 4x 010 Channel A: Read current-sense amplifier output from ADC, gain = 8x 011 Channel B: Read average voltage of RS+ (input common-mode voltage) from ADC 100 Channel C: Read voltage of OUT from ADC 101 Channel D: Read voltage of SET from ADC 110 Channel E: Read internal die temperature from ADC 111 Read all channels in fast-read mode, sequentially every 2ms. Uses last gain setting.
3	SHDN	Power-on state = 0 0 = Normal operation 1 = Shutdown mode
4	LR	0 = Normal operation 1 = Reset if comparator is latched due to MODE = 111. This bit is automatically reset after a 1 is written.
7, 6, 5	MODE2, MODE1, MODE0	000 = Normal operation for op amp/comparator 111 = Comparator mode. OUT remains low until CSA output > V_{SET} for 1ms, OUT latches high for 50ms, then OUT autoretries by going low. The comparator has an internal ±10mV hysteresis voltage to help with noise immunity. For MAX9612, the polarity is reversed. 011 = Op-amp mode. OUT regulates pFET for 1ms at V_{SET}, OUT latches high for 50ms, then OUT autoretries by going low. For MAX9612, the polarity is reversed.

Control Register 2

Control Register 2 is an 8-bit write/read register that provides the different time delay options for asserting the comparator output when monitoring fault events. Tables 6 and 7 show the bit location and function for Control Register 2.

Table 6. Control Register 2

BIT NUMBER	7	6	5	4	3	2	1	0
BIT NAME	X	X	X	X	DTIM	RTIM	X	X
POR VALUE	0	0	0	0	0	0	0	0

Table 7. Control Register 2 Bit Descriptions

BIT	BIT NAME	FUNCTION
7, 6, 5, 4	X	Set to 0
3	DTIM	Watchdog delay time 0 = 1ms 1 = 100µs
2	RTIM	Watchdog retry delay time 0 = 50ms 1 = 10ms
1, 0	X	Set to 0

Power-On Reset

The MAX9611/MAX9612 include power-on reset circuitry that ensures all registers reset to a known state on power-up. Once V_{CC} goes above 2.4V, the POR circuit releases the registers for normal operation.

Applications Information

Inrush Current Limiter

The MAX9611 can be used as an inrush current limiter for a number of applications as shown in Figure 3. Note that the sense resistor can be placed on either side of the pFET. Since the input common-mode voltage of the MAX9611 extends to ground, the sense resistor can be placed at the load side as well, allowing current to be sensed even when there is a dead-short on the load.

The inrush current limiting circuit reads and measures the load current during normal operation and can limit the load current to a user-set value. In normal operation, the load current is below the set threshold. The pFET is fully turned on because the op-amp output is at 0V. In the event of an overcurrent situation at the load, the op-amp controls the pFET's gate-voltage so it transitions to a linear region, thus limiting the load current. In this case, the op-amp output voltage is between 0V and V_{BAT}, as required for current-limiting.

Choose a suitable sense resistor and a low R_{DS-ON} pFET to ensure the best efficiency during normal operation. Choose a pFET with large power dissipation to ensure compliance with safe operating area of the pFET. The MAX9611 comes equipped with a variety of watchdog options to help with this design (see Control Register 2, Table 7).

Choose resistor values R1 and R2 to ensure that the pFET is fully on in normal operating conditions and to ensure that the VGS maximum rating is not exceeded. Also, R1 and R2 help limit the current in the open-drain output stage of the internal op amp. R_{COMP} and C_{COMP} help rolloff high-frequency gain of the feedback control system. R2 and C_{COMP} set a pole, for which 10kHz is a good choice. R_{COMP} and C_{COMP} set a zero, for which 100kHz is a good choice.

With the internal gain of the current-sense amplifier (2.5V/V), the inrush current-limit threshold can be set using resistor-divider R3 and R4 as follows:

$$\frac{V_{CC} \times R3}{(R4 + R3)(2.5 \times R_{SENSE})} = I_{LIMIT}$$

Note: The inrush current limiter can be changed to a high-side relay-disconnect circuit by using the MAX9611 set to comparator mode (MODE 111).

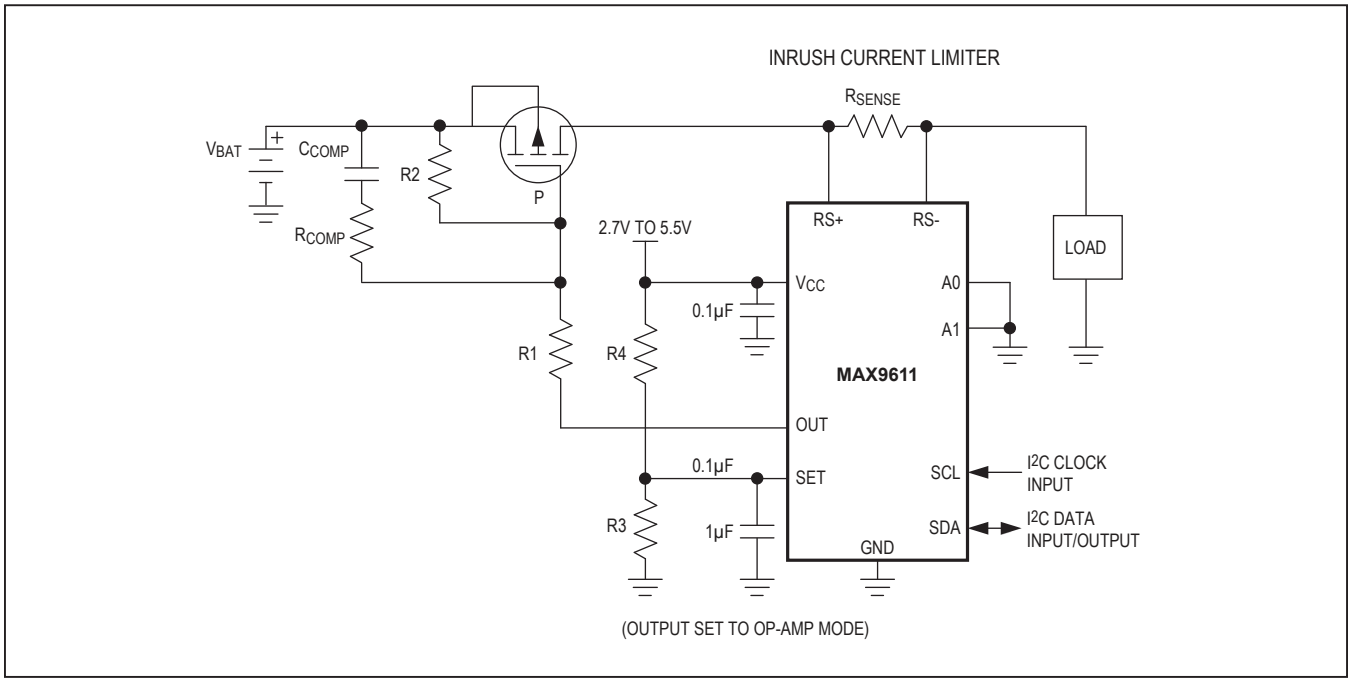


Figure 3. Inrush Current Limiter

Base-Station PA Gain Control

While the MAX9611 is designed to control high-side pFETs, the MAX9612 can be similarly used to control low-side nFETs. For example, the MAX9612 can be used to control the DC bias point of power amplifier LDMOS or GaN nFETs in base-station applications. The circuit shown in Figure 4 also allows the option to apply negative bias voltages to the PA FET, which is required for certain types of transistors for proper operation.

In the circuit shown, the nFET is in a linear mode of operation to allow it to amplify high-frequency RF signals, while the MAX9612 sets the DC operating point. The gain of the FET can be varied by changing its drain current. This operating point can be varied by an external DAC voltage that feeds the SET pin.

V_{NEG} and V_{CLAMP} together with R1, R2, and R3 set the DC bias point limits for the PA transistor. V_{CLAMP} is a suitable positive voltage and V_{NEG} is a suitable negative voltage. When V_{OUT} = 0V, the gate voltage of the PA FET is:

$$\frac{V_{NEG} \times R2}{(R1 + R2)} = V_{OUT}$$

When the OUT open-dran transistor is off, the gate voltage of the PA FET is:

$$V_{GATE} = \frac{V_{CLAMP} R1}{R1 + R2 + R3} + \frac{V_{NEG}(R2 + R3)}{R1 + R2 + R3}$$

R_{COMP} and C_{COMP} connected to the OUT pin compensate the internal amplifier. Choose a corner frequency of 100kHz.

Choose suitable R_{SENSE} as required for the application. The inductor isolates the DC measuring point of current from the high-frequency AC signals through the PA FET, as well as helping with the high-frequency gain.

Power-Supply Bypassing and Grounding

The MAX9611/MAX9612 share a common ground pin for both the analog and digital on-chip circuitry. It is therefore very important to properly bypass the V_{CC} to GND, and to have a solid low-noise ground plane on the circuit board so as to minimize ground bounce. Bypass V_{CC} to GND with low ESR 0.1µF in parallel with a 4.7µF ceramic capacitor to GND placed as close as possible to the device.

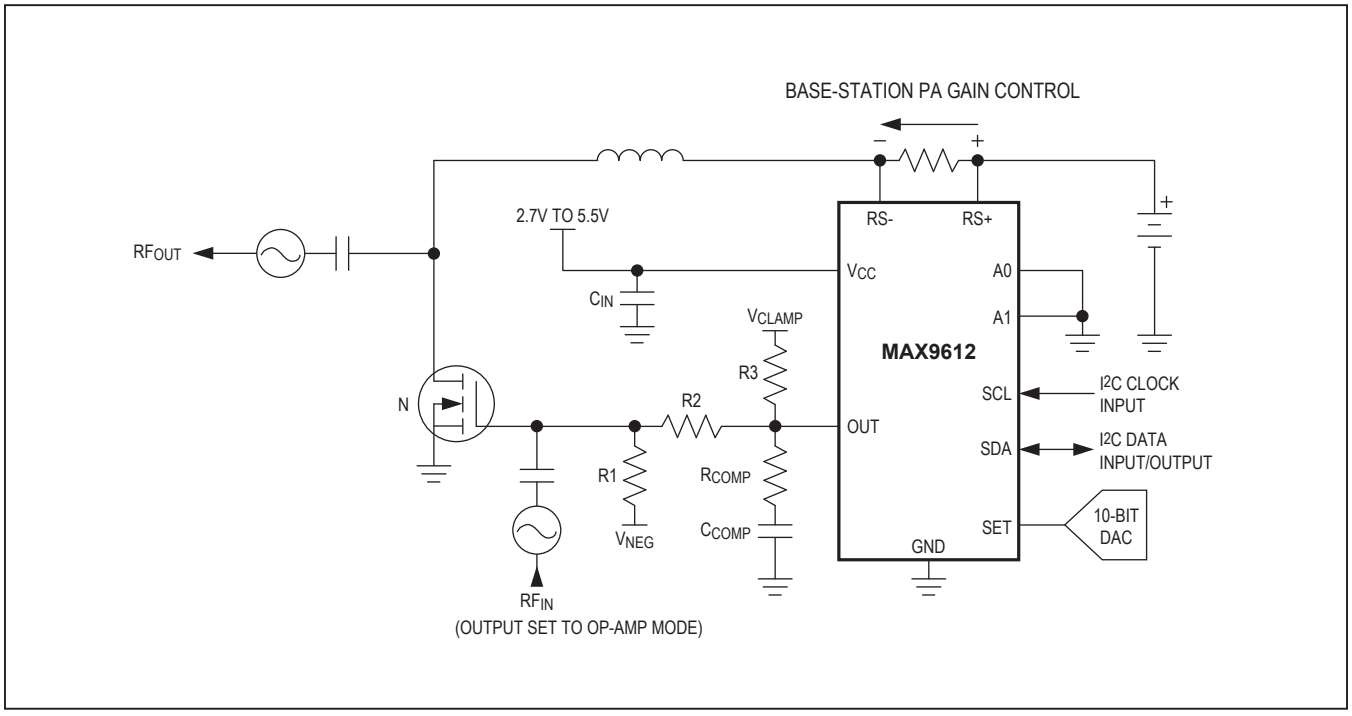


Figure 4. Base-Station PA Gain Control

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10+2	**21-0061**	**90-0330**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	11/10	Updated text in Table 5 to add “comparator” to mode 000 for bits 7, 6, 5	16
2	1/11	Relaxed room temperature limits for 4x and 8x gains from 0.3mV to 0.5mv	1, 2
3	6/11	Updated TYP spec for output current sink in the *Electrical Characteristics* and TOC 11	3, 7
4	6/14	Update equation in *Inrush Current Limiter* section	17
5	12/19	Updated *Electrical Characteristics*	4

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