Multioutput Power Management Solution with 4 Buck Switching and 3 LDO Linear Regulators

FEATURES

- **Quad Adjustable High Efficiency Step-Down DC/DC Converters: 2.5A, 2.5A, 1.5A, 1.5A**
- **Three 300mA LDO Regulators (Two Adjustable)**
- **Independent Enable Pin-Strap Sequencing**
- Power Good
- 2.25MHz Switching Frequency
- 12µA Standby Current
- 150°C T_J Operation (LT3383H)
- Side Wettable 40-Lead 6mm × 6mm QFN Package

APPLICATIONS

- Automotive
- Industrial
- Communications
- General Purpose Multichannel Power Supplies

DESCRIPTION

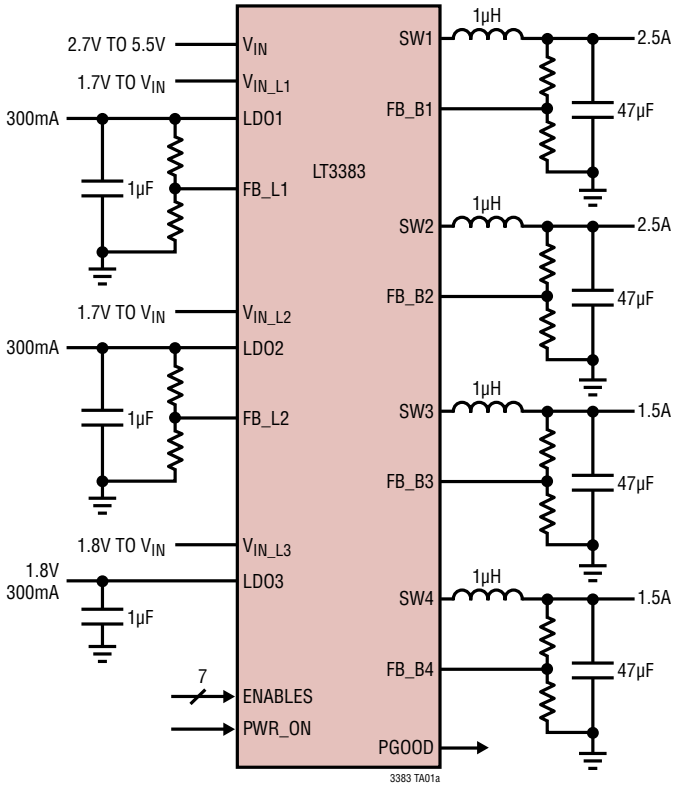
The LT®3383 is a complete power management solution for advanced portable application processor-based systems. The device contains four synchronous step-down DC/DC converters for core, memory, I/O, and system on-chip (SoC) rails and three 300mA LDO regulators for low noise analog supplies.

Regulator start-up is sequenced by connecting outputs to enable pins in the desired order. A master power-on pin is provided to initiate pin-strapped power-on sequences.

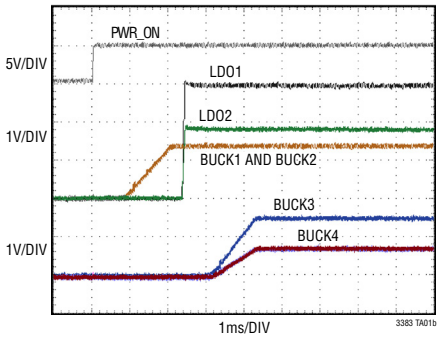
A status pin is available to indicate regulator undervoltages. If an overtemperature or low supply fault is detected all regulators are disabled during the fault condition.

The device is available in a 40-lead 6mm × 6mm QFN with wettable flanks for optical inspection.

TYPICAL APPLICATION



Start-Up Sequence

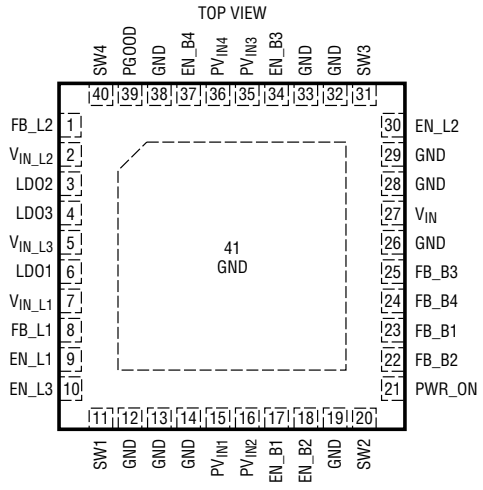


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 6V
PV_{IN1}, PV_{IN2}, PV_{IN3}, PV_{IN4}.....V_{IN} – 0.3V to V_{IN} + 0.3V
V_{IN_L1}, V_{IN_L2}, V_{IN_L3} ..... –0.3V to V_{IN} + 0.3V
LDO1, FB_L1, LDO2, FB_L2, LDO3, FB_B1, FB_B2, FB_B3, FB_B4, PGOOD, EN_B1, EN_B2, EN_B3, EN_B4, EN_L1, EN_L2, EN_L3, PWR_ON ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJM PACKAGE
40-LEAD (6mm × 6mm) WETTABLE PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3383EUJM#PBF	LT3383EUJM#TRPBF	LT3383UJM	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT3383IUJM#PBF	LT3383IUJM#TRPBF	LT3383UJM	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT3383HUJM#PBF	LT3383HUJM#TRPBF	LT3383UJM	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L1} = V_{IN_L2} = V_{IN_L3} = 3.8V. All regulators disabled unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Supply Voltage, V_{IN}		●	2.7		5.5	V
V_{IN} Standby Current	PWR_ON = 0V	●		12	21	µA
V_{IN} Undervoltage Fault Rising (Note 7) V_{IN} Undervoltage Fault Falling		● ●	 2.35	2.55 2.45	2.65	V V
Step-Down Switching Regulators 1, 2, 3 and 4						
Output Voltage Range		●	V_{FB}		PV_{IN}	V
V_{IN} Quiescent Current	FB_B*x* = 850mV (Note 5)	●		120	200	µA
Feedback Regulation Voltage (V_{FB})		●	714	725	736	mV
Feedback Pin Input Current	FB_B*x* = 850mV		–0.05		0.05	µA
Maximum Duty Cycle	FB_B*x* = 0V	●	100			%
Minimum Duty Cycle		●		18	24	%
SW Pull-Down Resistance	Regulator Disabled			625		Ω
Feedback Reference Soft-Start Rate	(Note 6)			0.8		V/ms
Switching Frequency		●	1.7	2.25	2.7	MHz
1.5A Step-Down Switching Regulators 3 and 4						
PMOS Current Limit		●	2.0			A
PMOS On-Resistance				160		mΩ
NMOS On-Resistance				80		mΩ
2.5A Step-Down Switching Regulators 1 and 2						
PMOS Current Limit		●	3.0			A
PMOS On-Resistance				120		mΩ
NMOS On-Resistance				70		mΩ
LDO Regulators 1, 2 and 3						
Feedback Reference Soft-Start Rate				10		V/ms
Output Pull-Down Resistance	Regulator Disabled			625		Ω
LDO Regulators 1 and 2						
V_{IN_Lx} Input Voltage		●	1.7		V_{IN}	V
Output Voltage Range	I_{LDO} = 0mA		V_{FB_Lx}		V_{IN_Lx}	V
Available Output Current		●	300			mA
V_{IN_Lx} Quiescent Current V_{IN_Lx} Shutdown Current	Regulator Enabled, I_{LDO} = 0A Regulator Disabled	● ●		12 0	25 1	µA µA
V_{IN} Quiescent Current	Regulator Enabled	●		50	85	µA
Feedback Regulation Voltage		●	0.707	0.725	0.743	V
Line Regulation	I_{LDO} = 1mA, V_{IN} = 2.7V to 5.5V			0.01		%/V
Load Regulation	I_{LDO} = 1mA to 300mA			0.01		%
Short-Circuit Current Limit					770	mA
Dropout Voltage (Note 4)	I_{LDO} = 300mA, V_{LDO} = 2.5V I_{LDO} = 300mA, V_{LDO} = 1.2V			210 450	260 615	mV mV
Feedback Pin Input Current	FB_L*x* = 725mV		–0.05		0.05	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L1} = V_{IN_L2} = V_{IN_L3} = 3.8V. All regulators disabled unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator 3						
V_{IN_L3} Input Voltage		●	2.35		V_{IN}	V
Output Voltage	I_{LDO} = 1mA	●	1.746	1.8	1.854	V
Available Output Current		●	300			mA
V_{IN_L3} Quiescent Current V_{IN_L3} Shutdown Current	Regulator Enabled, I_{LDO} = 0A Regulator Disabled	● ●		14 0	25 1	µA µA
V_{IN} Quiescent Current	Regulator Enabled	●		50	85	µA
Line Regulation	I_{LDO} =1mA, V_{IN} = 2.7V to 5.5V			0.01		%/V
Load Regulation	I_{LDO} = 1mA to 300mA			0.05		%
Short-Circuit Current Limit					770	mA
Dropout Voltage (Note 4)	I_{LDO} = 300mA, V_{LDO3} = 1.8V			280	350	mV
Enable Inputs						
Threshold Rising	All Enables Low	●		0.75	1.2	V
Threshold Falling	One Enable High	●	0.4	0.7		V
Precision Threshold	One or More Regulators Previously Enabled	●	0.370	0.400	0.430	V
Input Pull-Down Resistance				4.5		MΩ
PWR_ON						
Threshold		●	0.370	0.400	0.430	V
Pull-Down Resistance				4.5		MΩ
PWR_ON High to Allow Enables Delay				3		ms
PWR_ON High to Inhibit Enables Delay				3		ms
PGOOD						
PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
PGOOD Output High Leakage Current	V_{PGOOD} = 3.8V		–0.1		0.1	µA
PGOOD Threshold Rising PGOOD Threshold Falling				–6 –8		% %

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed Under Absolute Maximum ratings may cause permanent damage to the device. Exposure to any Absolute Maximum rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3383 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT3383E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3383I is guaranteed over the –40°C to 125°C operating junction temperature range and the LT3383H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts), and package to junction ambient thermal impedance (θ_{JA} in Watts/°C) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}).$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LT3383 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Dropout voltage is defined as ($V_{IN\_Lx} – V_{LDOx}$) when V_{LDOx} is 3% lower than V_{LDOx} measured with $V_{IN} = V_{IN\_Lx} = 4.3V$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

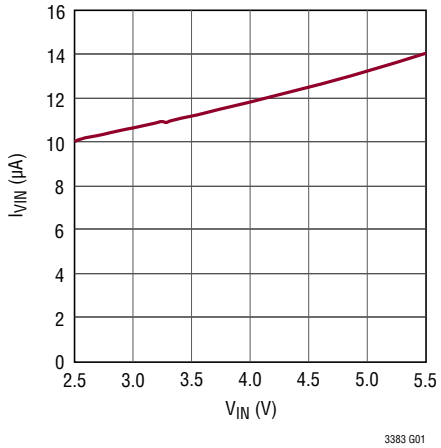
Note 6: Soft-Start measured in test mode with regulator error amplifier in unity-gain mode.

Note 7: The LT3383 will operate before V_{IN} has risen higher than V_{IN} undervoltage fault rising (2.65V max) but will shutdown if V_{IN} does not cross the rising threshold in less than 5 seconds. Please refer to the Operation section.

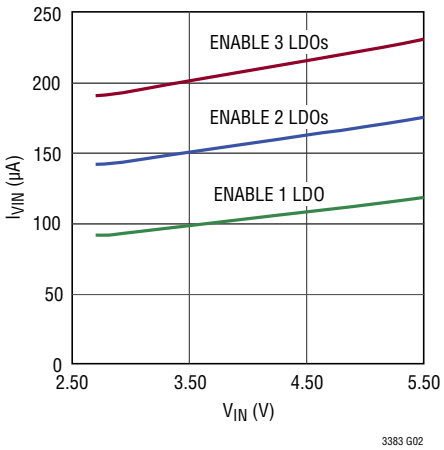
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C unless otherwise noted

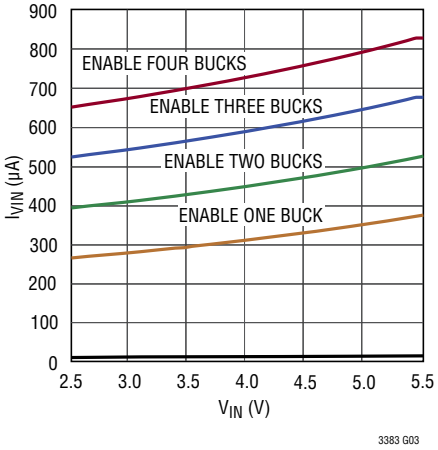
Standby I_{VIN} vs V_{IN}



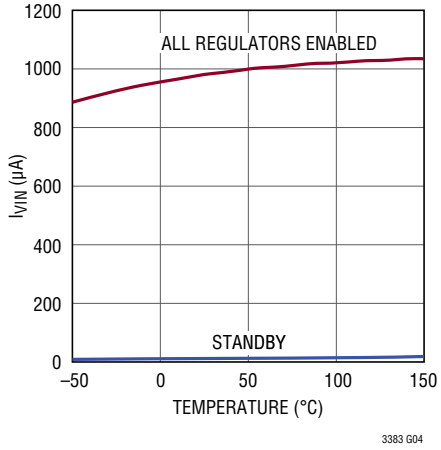
LDO1 to LDO3 I_{VIN} vs V_{IN}



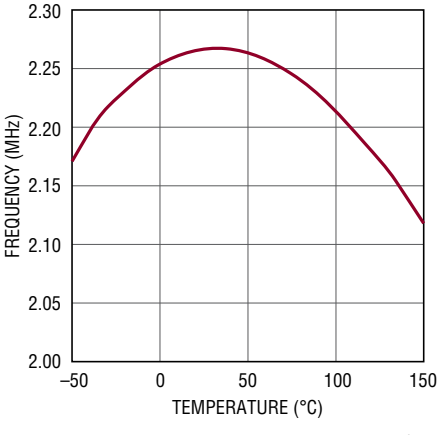
Step-Down Switching Regulator I_{VIN} vs V_{IN}



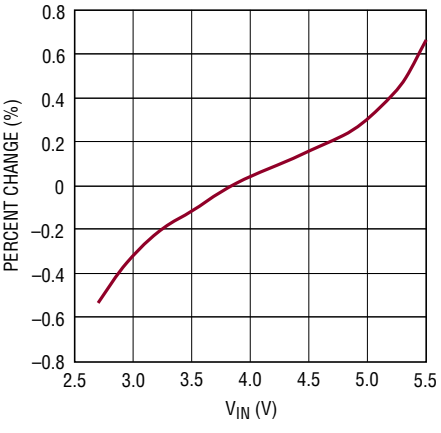
Input Supply Current vs Temperature



Oscillator Frequency vs Temperature



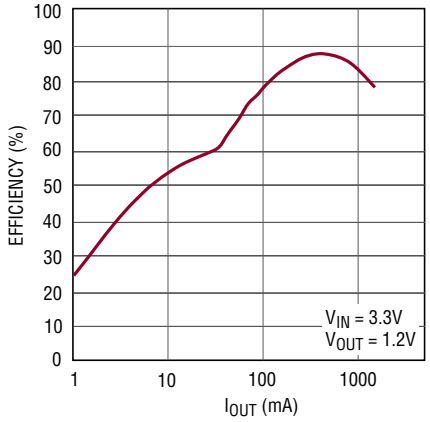
Oscillator Frequency Change vs V_{IN}



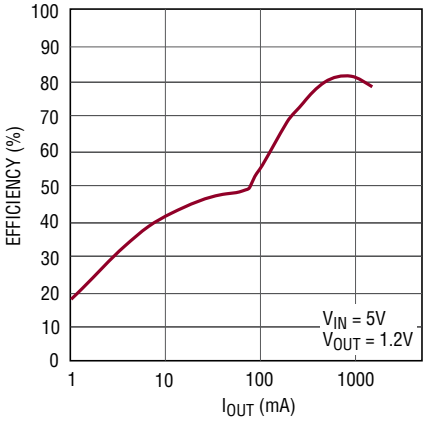
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C unless otherwise noted

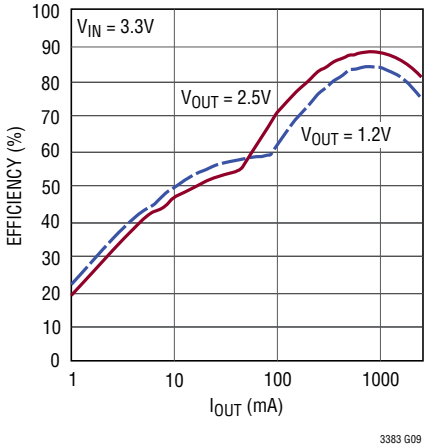
Step-Down Switching Regulators 3 and 4 Efficiency vs I_{OUT}



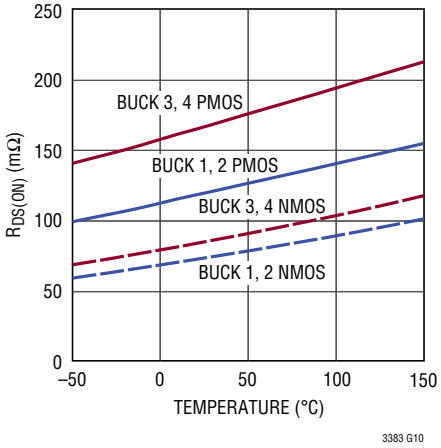
Step-Down Switching Regulators 3 and 4 Efficiency vs I_{OUT}



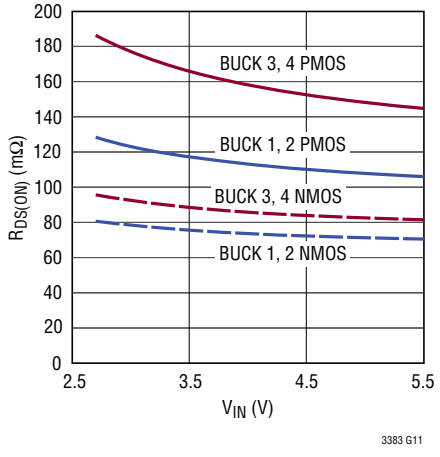
Step-Down Switching Regulators 1 and 2 Efficiency vs I_{OUT}



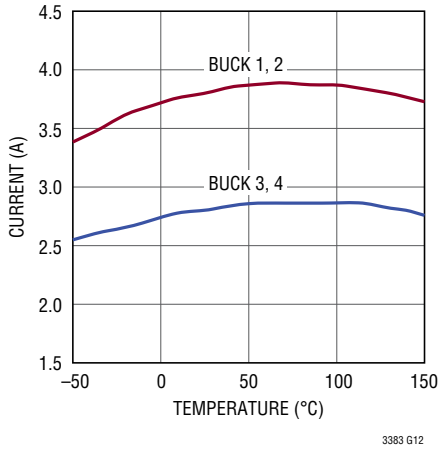
Buck $R_{DS(ON)}$ vs Temperature



Buck $R_{DS(ON)}$ vs V_{IN}



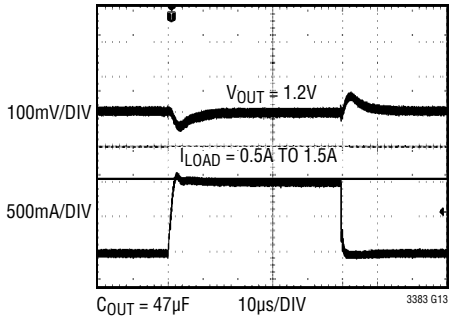
Step-Down Switching Regulator Current Limit vs Temperature



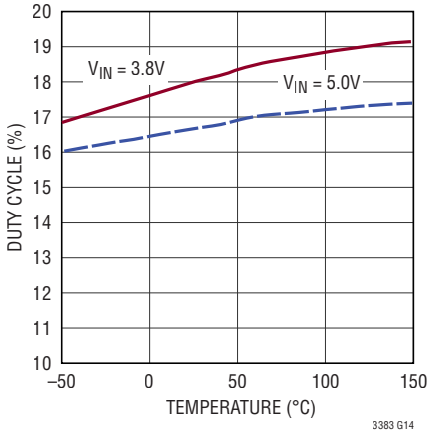
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C unless otherwise noted

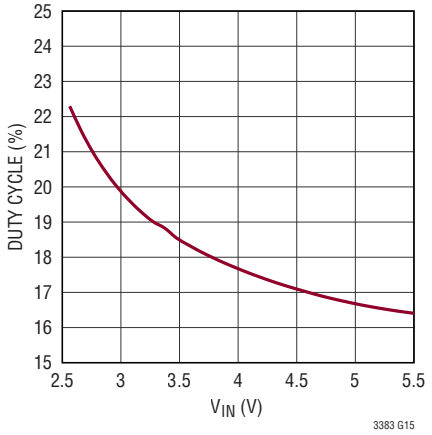
Step-Down Switching Regulator Load Step



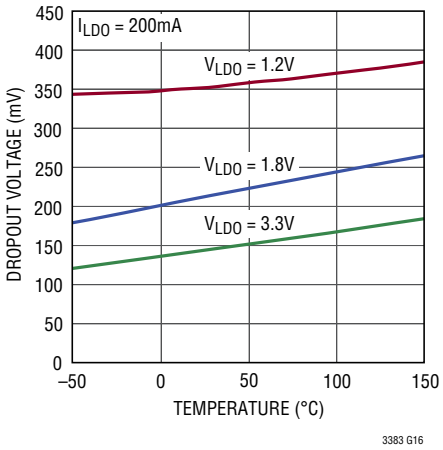
Buck Minimum Duty Cycle vs Temperature



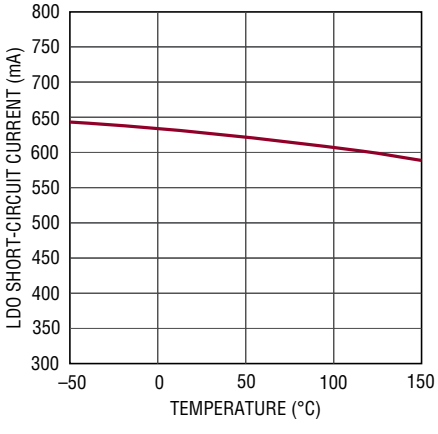
Buck Minimum Duty Cycle vs V_{IN}



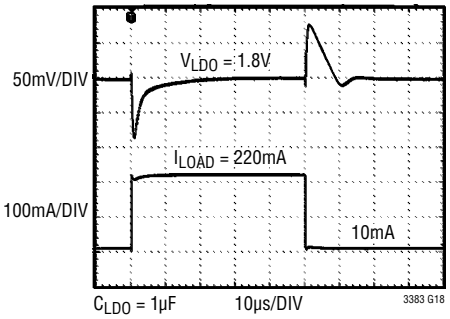
LDO1 to LDO3 Dropout Voltage vs Temperature



LDO1 to LDO3 Short-Circuit Current vs Temperature



LDO1 to LDO3 Load Step Response



PIN FUNCTIONS

FB_L2 (Pin 1): Feedback Input for LDO2. Set output voltage using a resistor divider connected from LDO2 to this pin to ground.

V_{IN_L2} (Pin 2): Power Input for LDO2. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L2} should not exceed voltage on V_{IN} pin.

LDO2 (Pin 3): Output Voltage of LDO2. Nominal output voltage is set with a resistor feedback divider that servos to a fixed 725mV reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO3 (Pin 4): Output Voltage of LDO3. Nominal output voltage is a fixed 1.8V. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_L3} (Pin 5): Power Input for LDO3. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L3} should not exceed voltage on V_{IN} pin.

LDO1 (Pin 6): Output Voltage of LDO1. Nominal output voltage is set with a resistor feedback divider that servos to a fixed 725mV reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_L1} (Pin 7): Power Input for LDO1. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. Voltage on V_{IN_L1} should not exceed voltage on V_{IN} pin.

FB_L1 (Pin 8): Feedback Input for LDO1. Set output voltage using a resistor divider connected from LDO1 to this pin to ground.

EN_L1 (Pin 9): Enable LDO1 Input. Active high enables LDO1. A weak pull-down pulls EN_L1 low when left floating.

EN_L3 (Pin 10): Enable LDO3 Input. Active high enables LDO3. A weak pull-down pulls EN_L3 low when left floating.

SW1 (Pin 11): Switch Pin for Step-Down Switching Regulator 1. Connect one side of step-down switching regulator 1 inductor to this pin.

GND (Pin 12): Ground

GND (Pin 13): Ground

GND (Pin 14): Ground

PV_{IN1} (Pin 15): Power Input for Step-Down Switching Regulator 1. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

PV_{IN2} (Pin 16): Power Input for Step-Down Switching Regulator 2. Tie this pin to the V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

EN_B1 (Pin 17): Enable Step-Down Switching Regulator 1. Active high input enables step-down switching regulator 1. A weak pull-down pulls EN_B1 low when left floating.

EN_B2 (Pin 18): Enable Step-Down Switching Regulator 2. Active high input enables step-down switching regulator 2. A weak pull-down pulls EN_B2 low when left floating.

GND (Pin 19): Ground.

SW2 (Pin 20): Switch Pin for Step-Down Switching Regulator 2. Connect one side of step-down switching regulator 2 inductor to this pin.

PWR_ON (Pin 21): Power On. PWR_ON is a master enable and disable input. When low, PWR_ON inhibits the regulator enable pins. When high, PWR_ON allows enable pin operation.

FB_B2 (Pin 22): Feedback Input for Step-Down Switching Regulator 2. Set output voltage using resistor divider connected from the output of step-down switching regulator 2 to this pin to ground.

FB_B1 (Pin 23): Feedback Input for Step-Down Switching Regulator 1. Set output voltage using resistor divider connected from the output of step-down switching regulator 1 to this pin to ground.

FB_B4 (Pin 24): Feedback Input for Step-Down Switching Regulator 4. Set output voltage using resistor divider connected from the output of step-down switching regulator 4 to this pin to ground.

PIN FUNCTIONS

FB_B3 (Pin 25): Feedback Input for Step-Down Switching Regulator 3. Set output voltage using resistor divider connected from the output of step-down switching regulator 3 to this pin to ground.

GND (Pin 26): Ground.

V_{IN} (Pin 27): Supply Voltage Input. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor. All switching regulator PV_{IN} supplies should be tied to V_{IN}.

GND (Pin 28): Ground.

GND (Pin 29): Ground.

EN_L2 (Pin 30): Enable LDO2 Input. Active high enables LDO2. A weak pull-down pulls EN_L2 low when left floating.

SW3 (Pin 31): Switch Pin for Step-Down Switching Regulator 3. Connect one side of step-down switching regulator 3 inductor to this pin.

GND (Pin 32): Ground.

GND (Pin 33): Ground.

EN_B3 (Pin 34): Enable Step-Down Switching Regulator 3. Active high input enables step-down switching regulator 3. A weak pull-down pulls EN_B3 low when left floating.

PV_{IN3} (Pin 35): Power Input for Step-Down Switching Regulator 3. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

PV_{IN4} (Pin 36): Power Input for Step-Down Switching Regulator 4. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10µF or greater ceramic capacitor.

EN_B4 (Pin 37): Enable Step-Down Switching Regulator 4. Active high enables step-down switching regulator 4. A week pull-down pulls EN_B4 low when left floating.

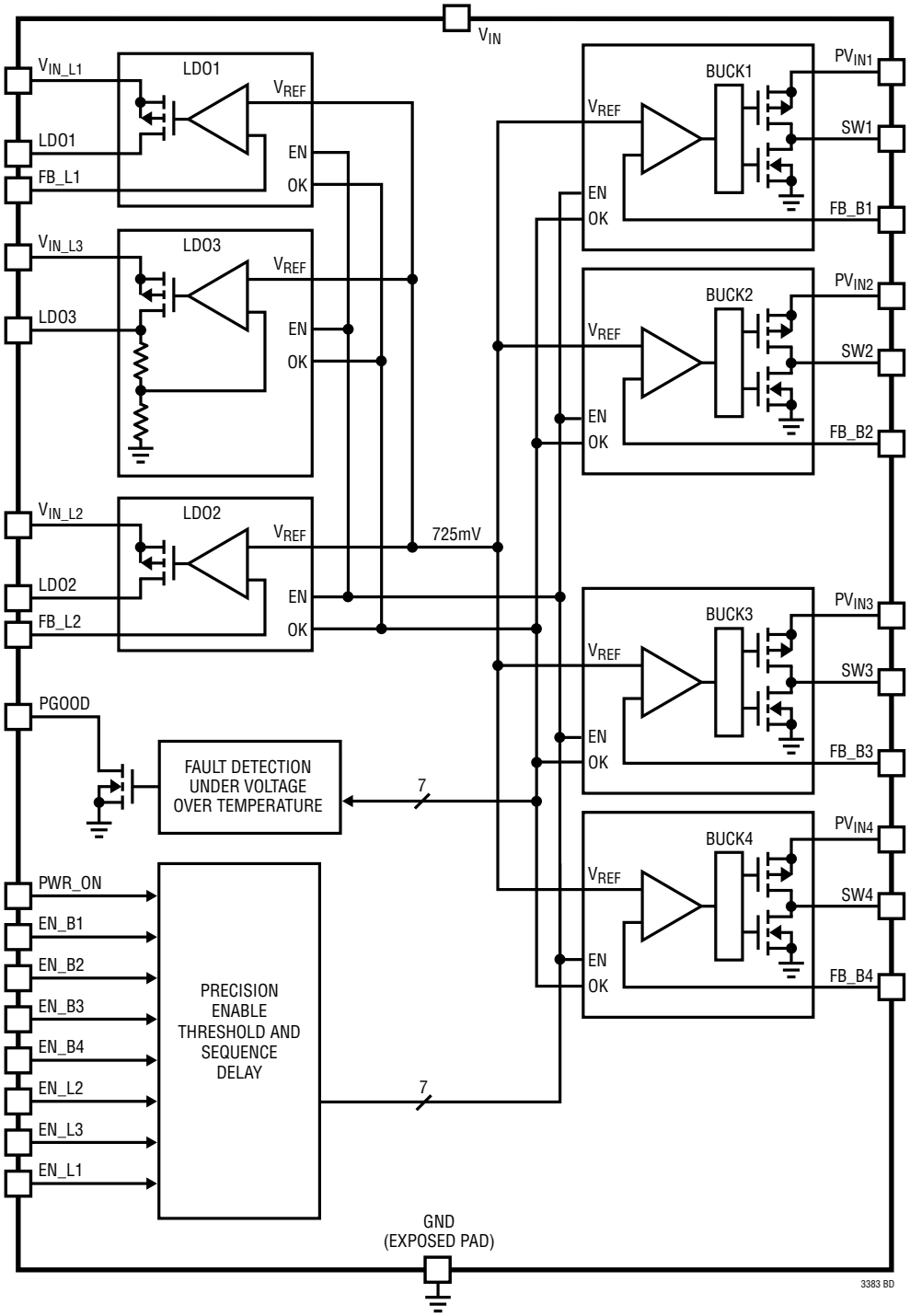
GND (Pin 38): Ground.

PGOOD (Pin 39): Power Good Output. Open-drain output pulls low when any enabled regulator falls below power good threshold. Pulls low when all regulators are disabled.

SW4 (Pin 40): Switch Pin for Step-Down Switching Regulator 4. Connect one side of step-down switching regulator 4 inductor to this pin.

GND (Exposed Pad Pin 41): Ground. The exposed pad must be connected to a continuous ground plane of the printed circuit board by multiple interconnect vias directly under the LT3383 to maximize electrical and thermal conduction.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3383 is a multi-topology, multiple-output voltage regulator. It generates a total of seven voltage rails. Supplying the voltage rails are two 2.5A step-down regulators, two 1.5A step-down regulators, and three 300mA low dropout regulators. Supporting the multiple regulators is a highly configurable power-on sequencing capability.

300mA Low Dropout Regulators

Three LDO regulators on the LT3383 will each deliver up to 300mA output. Each LDO regulator has a separate input supply to help manage power loss in the LDO output devices. When disabled, the regulator outputs are pulled to ground through a 625Ω resistor. A low ESR 1µF ceramic capacitor should be tied from the LDO output to ground. The 300mA LDO regulators have current limit control circuits. The LDO input voltages, V_{IN_L1}, V_{IN_L2}, and V_{IN_L3} must be at a potential of V_{IN} or less.

LT3383 Resistor Programmable LDO1 and LDO2

LDO1 and LDO2 output voltages are programmed by resistor dividers tied from the LDO output pin to the feedback pin as shown in Figure 1. The output voltage is calculated using the following formula:

$$V_{LDO} = \left(1 + \frac{R1}{R2}\right) \bullet (725)(mV)$$

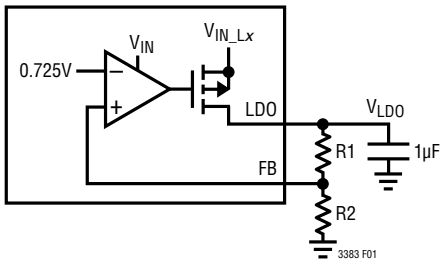


Figure 1. LDO1 and LDO2 Application Circuit

STEP-DOWN SWITCHING REGULATORS

The LT3383 contains four buck regulators. Two of the buck regulators are capable of delivering up to 2.5A load current and the other two can deliver up to 1.5A each. The regulators have forward and reverse current limiting, and soft-start.

The LT3383 buck regulators are capable of 100% duty cycle, or dropout, regulation. When in dropout the regulator output voltage is equal to PV_{IN} minus the load current times $R_{DS(ON)}$ of the converters PMOS device and inductor DCR.

Operating Mode

The buck regulators operate in pulse-skipping mode. In pulse-skipping mode the regulator skips pulses at light loads but operates at constant frequency at higher loads.

Setting Output Voltage

The output voltage is set by using a resistor divider connected from the step-down switching regulator output to its feedback pin as shown in Figure 2. The output voltage is calculated using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (725)(mV)$$

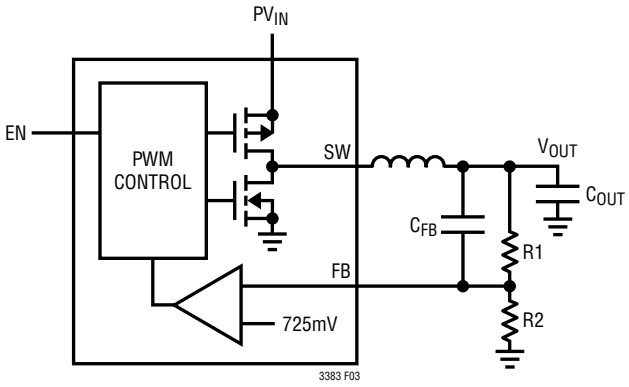


Figure 2. Step-Down Switching Regulator Application Circuit

OPERATION

Typical values for R1 are in the range of 40k to 1M. Capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance on the FB pin and helps to improve load step transient response. A value of 10pF is recommended.

Inductor Selection

The choice of step-down switching regulator inductor influences the efficiency and output voltage ripple of the converter. A larger inductor improves efficiency since the peak current is closer to the average output current. Larger inductors generally have higher series resistance that counters the efficiency advantage of reduced peak current.

Inductor ripple current is a function of switching frequency, inductance, V_{IN}, and V_{OUT} as shown in this equation:

$$\Delta I_L = \frac{1}{f \bullet L} \bullet V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A good starting design point is to use an inductor that gives ripple equal to 30% of the maximum output current. Select an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure the inductor does not saturate.

Input and Output Capacitor Selection

Low ESR ceramic capacitors should be used at both the output and input supply of the switching regulators. Only X5R or X7R ceramic capacitors should be used since they have better temperature and voltage stability than other ceramic types.

Minimum On-Time

The lowest duty cycle at which the step-down converter can maintain constant frequency operation in regulation is determined by the minimum on-time. Minimum on-time is the shortest time duration that the converter can turn its top PMOS on and off again (typically 70ns). If the duty cycle requires an average on-time which falls below the minimum on time of the converter, the output voltage ripple will increase as the converter skips cycles to maintain regulation.

Soft-Start

To reduce inrush current at start-up each buck regulator soft starts when enabled. When enabled the internal reference voltage is ramped from ground to 725mV at a rate of 0.8V/ms.

PWR_ON Enable Control

The PWR_ON pin acts as a master enable pin by inhibiting or allowing all the individual regulator enable pins. A typical use is to drive PWR_ON with a power-good status pin from a pre-regulator. Figure 3 shows the timing relationship between PWR_ON and inhibition of the enable pins.

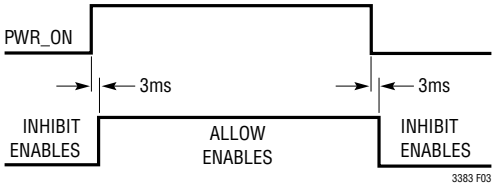


Figure 3. Power-Up and Down with PWR_ON

POWER ON SEQUENCING

Enable Pin Operation

The LT3383 enable pins facilitate pin-strapping output rails to enable pins to up-sequence the LT3383 regulators in any order. Figure 4 shows an example of pin-strapped sequence connections. The enable pins normally have a 0.75V (typical) input voltage threshold.

If any enable is driven high, the remaining enable input thresholds switch to an accurate 400mV threshold. To ensure separation of the sequenced rails, there is a built-in

OPERATION

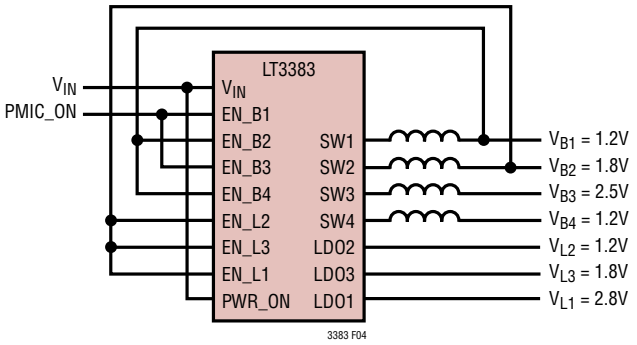


Figure 4. Pin-Strapped Power-On Sequence Application

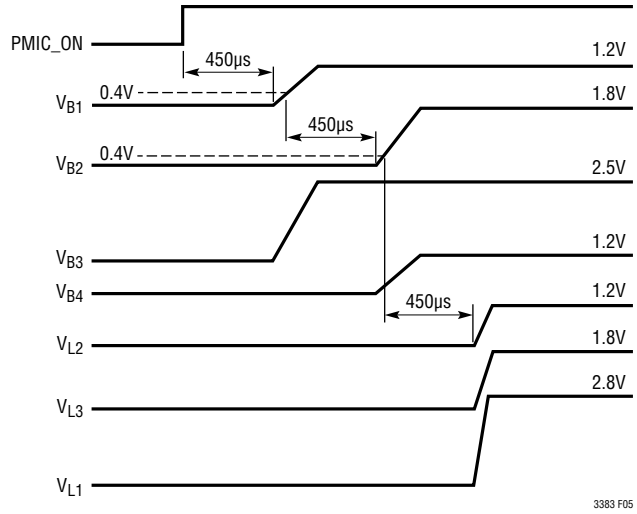


Figure 5. Pin-Strapped Power-On Sequence

450µs delay from the enable pin threshold crossing to the internal enable of the regulator. Figure 5 shows the start-up timing of the example shown in Figure 4.

FAULT DETECTION AND REPORTING

The LT3383 has fault detection circuits that monitor for V_{IN} undervoltage, die overtemperature, and regulator output undervoltage.

V_{IN} Undervoltage

The undervoltage (UV) circuit monitors the input supply voltage, V_{IN}, and when the voltage falls below 2.45V creates a fault condition that forces the LT3383 to disable all outputs until V_{IN} rises above UVLO rising threshold.

The V_{IN} undervoltage fault rising (2.65V max) defines the voltage at which V_{IN} rising undervoltage fault is detected. The LT3383 will respond to PWR_ON and regulator enable pins when V_{IN} is less than the V_{IN} undervoltage fault rising threshold at initial application of V_{IN}. An internal timer will inhibit all enables if V_{IN} does not cross the rising fault threshold within 5 seconds. PWR_ON and enables should be asserted only when the application has applied V_{IN} greater than the minimum V_{IN} input of 2.7V. A power good signal from a V_{IN} preregulator or voltage divider from V_{IN} to the 400mV (Typ) PWR_ON input threshold may be used to ensure V_{IN} is above 2.7V.

Overtemperature

To prevent thermal damage the LT3383 incorporates an overtemperature (OT) circuit. When the die temperature reaches 155°C the OT circuit creates a fault condition that forces the LT3383 to disable all outputs until the temperature falls below the overtemperature threshold.

PGOOD Status Pin

The PGOOD open-drain status pin is pulled low when all regulators are disabled. PGOOD is released when all enabled regulator outputs are above 94% of their programmed value. When any enabled regulator output falls below 92% of its programmed value for longer than 50µs the PGOOD pin is pulled low. A 50µs transient filter on PGOOD prevents PGOOD glitches due to transients. The PGOOD pin is held low for a minimum of 1ms. Figure 6 shows the timing of PGOOD during enable and fault events.

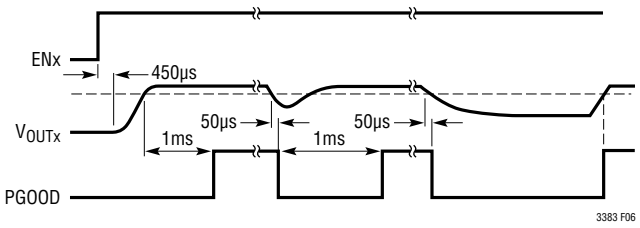


Figure 6. Output Low Voltage PGOOD Timing

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS AND BOARD LAYOUT

Printed Circuit Board Power Dissipation

In order to ensure optimal performance and the ability to deliver maximum output power to any regulator, it is critical that the exposed ground pad on the backside of the LT3383 package be soldered to a ground plane on the board. Correctly soldered to a 2500mm^2 ground plane on a double-sided 1oz copper board, the LT3383 has a thermal resistance(θ_{JA}) of approximately 33°C/W. Failure to make good thermal contact between the exposed pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 33°C/W. To ensure the junction temperature of the LT3383 die does not exceed the maximum rated limit and to prevent overtemperature faults, the power output of the LT3383 must be managed by the application. The total power dissipation in the LT3383 is approximated by summing the power dissipation in each of the switching regulators and the LDO regulators. The power dissipation in a switching regulator is estimated by:

$$P_{D(SWx)} = V_{OUTx} \bullet I_{OUTx} \bullet \frac{100\text{-}Eff\%}{100} (W)$$

where V_{OUTx} is the programmed output voltage, I_{OUTx} is the load current, and Eff is the % efficiency that can be measured or looked up from the efficiency curves for the programmed output voltage.

The power dissipated by an LDO regulator is estimated by:

$$P_{D(LDOx)} = (V_{IN\_Lx} - V_{LDOx}) \bullet I_{LDOx} (W)$$

where V_{LDOx} is the programmed output voltage, $V_{IN(LDOx)}$ is the LDO supply voltage, and I_{LDOx} is the output load current. If one of the switching regulator outputs is used as an LDO supply voltage, remember to include the LDO supply current in the switching regulator load current for calculating power loss.

An example using the equations above with the parameters in Table 1 shows an application that is at a junction temperature of 118°C at an ambient temperature of 55°C. LDO2, LDO3, and LDO1 are powered by step-down Buck2 and Buck4. The total load on Buck2 and Buck4 is the sum of the application load and the LDO load. This example is with the LDO regulators at one-third rated current and the switching regulators at three-quarters rated current.

Table 1. LT3383 Power Loss Example

	V_{IN}	V_{OUT}	APPLICATION LOAD (A)	TOTAL LOAD (A)	EFF (%)	P_D (mW)
LDO2	1.8	1.2	0.1	0.100	–	60.00
LDO3	3.3	1.8	0.1	0.100	–	150.00
LDO1	3.3	2.5	0.1	0.100	–	80.00
Buck1	3.8	1.2	1.875	1.875	80	450.00
Buck2	3.8	1.8	1.775	1.875	85	506.25
Buck3	3.8	1.25	1.125	1.125	80	281.25
Buck4	3.8	3.3	0.925	1.125	90	371.25
					Total Power =	1899
				Internal Junction Temperature at 55°C Ambient		118°C

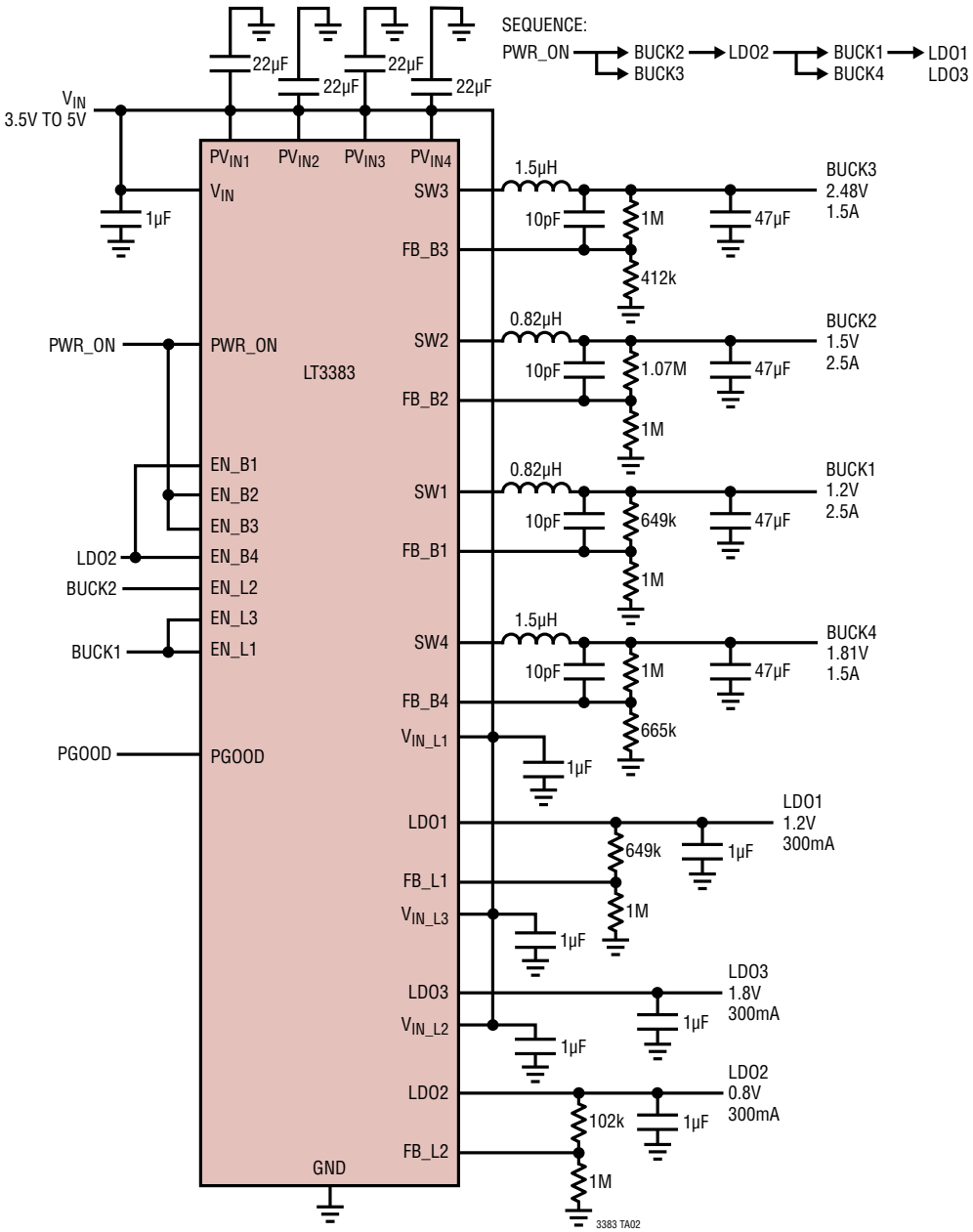
Printed Circuit Board Layout

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LT3383:

1. Connect the exposed pad of the package (Pin 41) directly to a large ground plane to minimize thermal and electrical impedance.
2. The switching regulator input supply traces to their decoupling capacitors should be as short as possible. Connect the GND side of the capacitors directly to the ground plane of the board. The decoupling capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from the capacitors to the LT3383 pins.
3. Minimize the switching power traces connecting SW1, SW2, SW3, and SW4 to the inductors to reduce radiated EMI and parasitic coupling. Keep sensitive nodes such as the feedback pins away from or shielded from the large voltage swings on the switching nodes.
4. Minimize the length of the connection between the step-down switching regulator inductors and the output capacitors. Connect the GND side of the output capacitors directly to the thermal ground plane of the board.

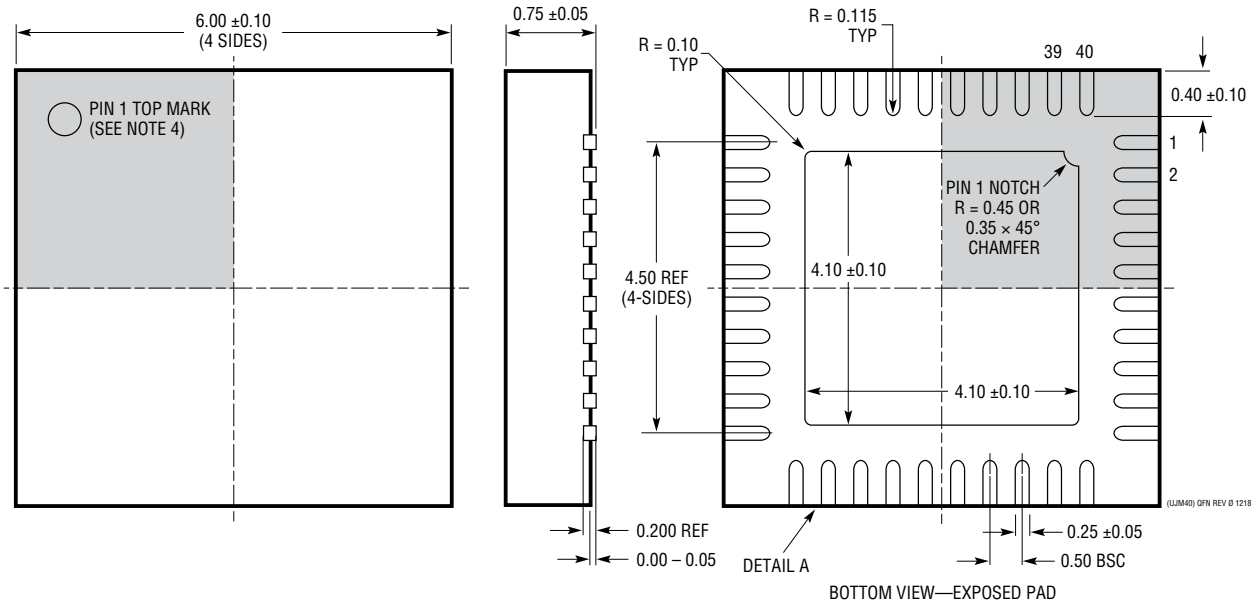
TYPICAL APPLICATIONS

LT3383 Seven Power Rails

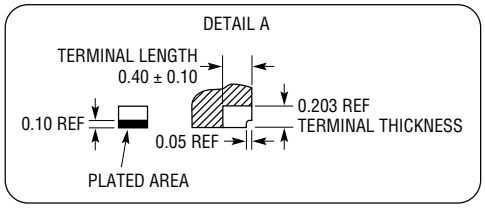


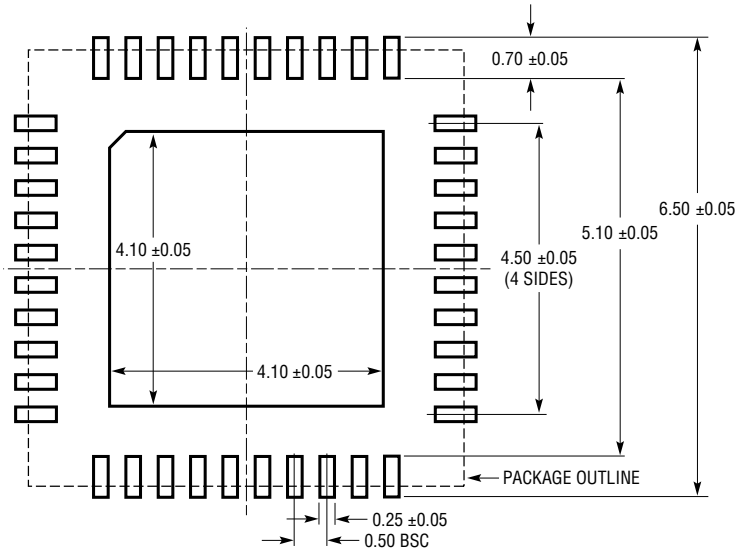
PACKAGE DESCRIPTION

UJM Package
40-Lead Plastic Side Wettable QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1681 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

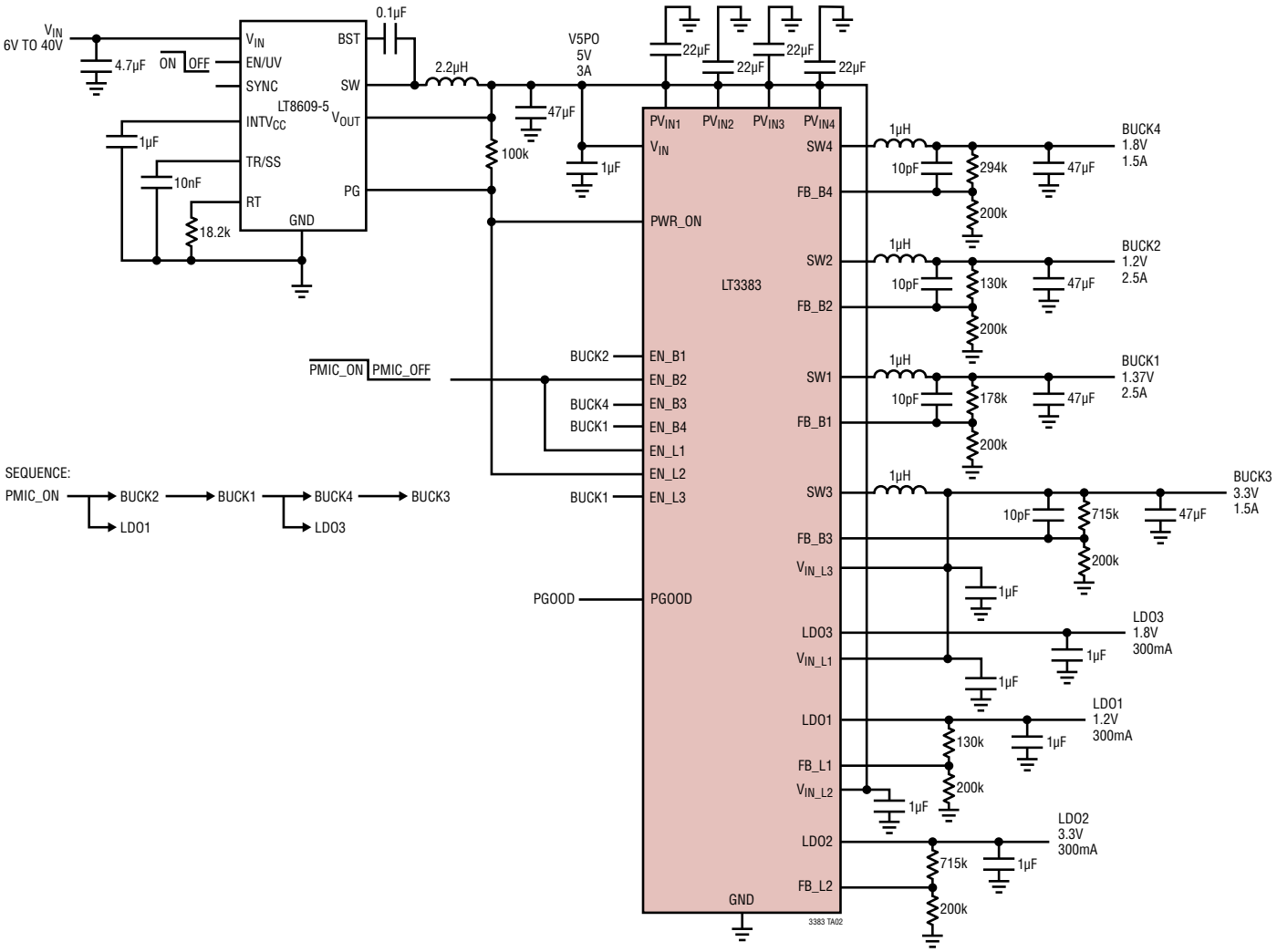




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

Seven Sequenced Power Rails From 40V Input Using LT8609-5



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3676/ LTC3676-1	PMIC for Application Processors	Quad I²C Adjustable High Efficiency Step-Down DC/DC Converters: 2.5A, 2.5A, 15A, 1.5A, Three 300mA LDO Regulators (Two Adjustable), DDR Power Solutions with VTT and VTTR Reference, Pushbutton ON/OFF Control, LTC3676-1 Supports DDR, 40-Lead 6mm × 6mm × 0.75mm QFN Package.
LTC3375	8-Channel Programmable, Parallelable 1A Buck DC/DCs	8-Channel Independent Step-Down DC/DCs. Master Slave Configurable for Up to 4A per Output Channel with a Single Inductor, Die Temperature Monitor Output, 48-Lead 7mm × 7mm QFN Package.
LTC3589/ LTC3589-1/ LTC3589-2	8-Output Regulator with Sequencing and I²C	Triple I²C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A. High Efficiency 1.2A Buck-Boost DC/DC Converter. Triple 250mA LDO Regulators. Pushbutton ON/OFF Control with System Reset. Flexible Pin-Strap Sequencing Operation. I²C and Independent Enable Control Pins, DVS and Slew Rate Control, 40-Lead 6mm × 6mm × 0.75mm QFN Package.
LTC3586/ LTC3586-1	Switching USB Power Manager PMIC with Li-Ion/Polymer Charger	Complete Multifunction PMIC: Switching Power Manager, 1A Buck-Boost + 2 Bucks + Boost + LDO, 4mm × 6mm QFN-38 Package, LTC3586-1 Version Has 4.1V V_{FLOAT}.

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:
LT3383HUJM#PBF LT3383HUJM#TRPBF LT3383IUJM#PBF LT3383IUJM#TRPBF LT3383EUJM#PBF LT3383EUJM#TRPBF DC2984A