Dual 2-to-4 line decoder/demultiplexer Rev. 5 — 14 January 2021

### 1. General description

The 74HC139; 74HCT139 decodes two binary weighted address inputs (nA0, nA1) to four mutually exclusive outputs (n $\overline{Y}$ 0 to n $\overline{Y}$ 3). Each decoder features an enable input (n $\overline{E}$ ). When n $\overline{E}$  is HIGH all outputs are forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

### 2. Features and benefits

- Input levels:
  - For 74HC139: CMOS level
  - For 74HCT139: TTL level
- Demultiplexing capability
- 2 independent 2-to-4 decoders
- Multifunction capability
- Suitable for memory decoding, data routing or code conversion
- Complies with JEDEC standard no. 7A
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
- MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Ordering information

#### Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74HC139D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1					
74 HCT139D			body width 3.9 mm						
74HC139PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package;	SOT403-1					
74HCT139PW			16 leads; body width 4.4 mm						

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### 4. Functional diagram

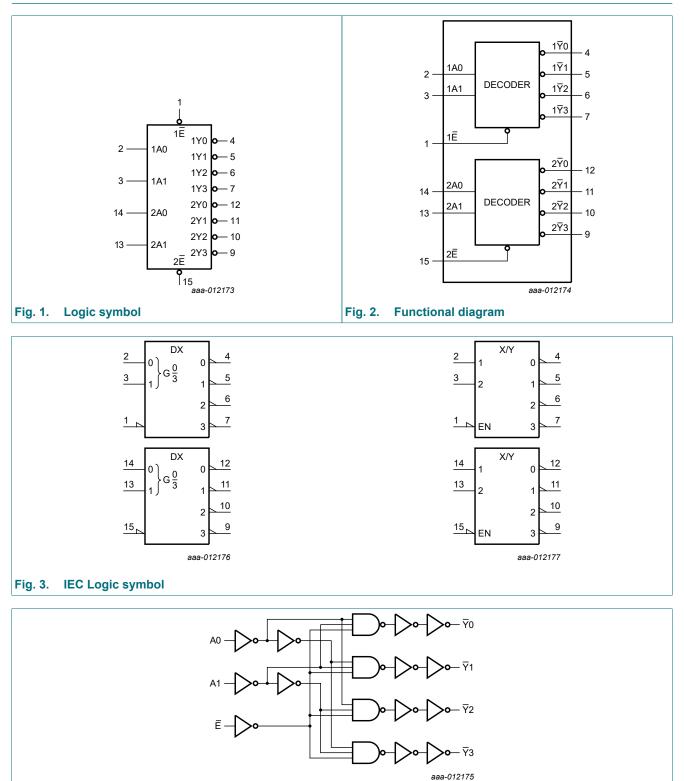
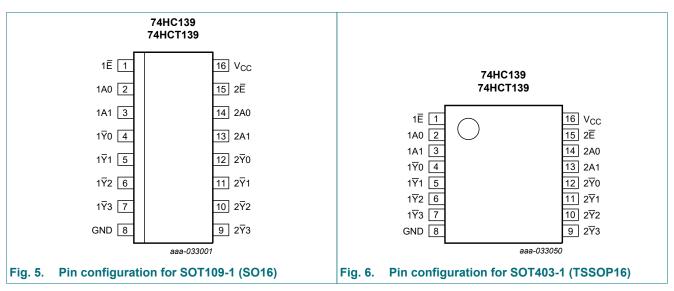


Fig. 4. Logic diagram (one decoder/demultiplexer)

### 5. Pinning information



### 5.2. Pin description

Table :	2. Pin	description

Symbol	Pin	
1E, 2E	1, 15	enable input (active LOW)
1A0, 1A1	2, 3	address input
170, 171, 172, 173	4, 5, 6, 7	output (active LOW)
GND	8	ground (0 V)
270, 271, 272, 273	12, 11, 10, 9	output (active LOW)
2A0, 2A1	14, 13	address input
V <sub>CC</sub>	16	positive supply voltage

### 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Control	Input		Output						
nĒ	nA1	nA0	n¥3	n <u></u> ¥2	n <u></u> ¶1	n¥0			
Н	Х	Х	Н	Н	Н	Н			
L	L	L	Н	Н	Н	L			
L	L	Н	Н	Н	L	Н			
L	Н	L	Н	L	Н	Н			
L	Н	Н	L	Н	Н	Н			

### 5.1. Pinning

### 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
l <sub>IK</sub>	input clamping current	$V_{I}$ < -0.5 V or $V_{I}$ > $V_{CC}$ + 0.5 V		-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V		-	±20	mA
lo	output current	$V_{O}$ = -0.5 V to ( $V_{CC}$ + 0.5 V)		-	±25	mA
I <sub>CC</sub>	quiescent supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation		[1]	-	500	mW

 For SOT109-1 (SO16) package: P<sub>tot</sub> derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P<sub>tot</sub> derates linearly with 8.5 mW/K above 91 °C.

### 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC139			74HCT139			Unit
			Min	Тур	Мах	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

# 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Мах	Min	Max	1
74HC13	9	1								
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current		-	-	±0.5	-	±5.0	-	±10.0	μA
I <sub>CC</sub>	supply current	$V_1 = V_{CC}$ or GND; $I_0 = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	39									
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_{I}$ = $V_{IH}$ or $V_{IL}$ ; $V_{CC}$ = 4.5 V								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	μA

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Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	1
I <sub>OZ</sub>	OFF-state output current		-	-	±0.5	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	$V_{I} = V_{CC} - 2.1 V;$ other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		per input pin; 1An inputs	-	70	252	-	315	-	343	μA
		per input pin; 2An inputs	-	70	252	-	315	-	343	μA
		per input pin; nE inputs	-	135	486	-	607.5	-	661.5	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

# **10.** Dynamic characteristics

#### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L$  = 50 pF unless otherwise specified; for test circuit see Fig. 9.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Мах	Min	Max	
74HC139	9					1				
t <sub>pd</sub>	propagation	nAn to $n\overline{Y}n$ ; see Fig. 7 [1	]							
	delay	V <sub>CC</sub> = 2.0 V	-	39	145	-	180	-	220	ns
		V <sub>CC</sub> = 4.5 V	-	14	29	-	36	-	44	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	11	25	-	31	-	38	ns
		nE to nYn; see Fig. 8 [1	]							
		V <sub>CC</sub> = 2.0 V	-	33	135	-	170	-	205	ns
		V <sub>CC</sub> = 4.5 V	-	12	27	-	34	-	41	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	10	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	10	23	-	29	-	35	ns
t <sub>t</sub>	transition	nYn; see <u>Fig. 7</u> and <u>Fig. 8</u> [2	]							
	time	V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L = 50 \text{ pF}; \text{ f} = 1 \text{ MHz};$ [3 V <sub>I</sub> = GND to V <sub>CC</sub>	- [	42	-	-	-	-	-	pF

#### **Dual 2-to-4 line decoder/demultiplexer**

Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
74HCT1	39										
t <sub>pd</sub>	propagation	nAn to Yn; see <u>Fig. 7</u>	[1]								
	delay	V <sub>CC</sub> = 4.5 V		-	16	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF		-	13	-	-	-	-	-	ns
		nĒ to nŸn; see <u>Fig. 8</u>	[1]								
		V <sub>CC</sub> = 4.5 V		-	16	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF		-	13	-	-	-	-	-	ns
t <sub>t</sub>	transition	n <del>Y</del> n; see <u>Fig. 7</u> and <u>Fig. 8</u>	[2]								
	time	V <sub>CC</sub> = 4.5 V		-	7	15	-	19	-	22	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	[3]	-	44	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2]

 $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ). [3]

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

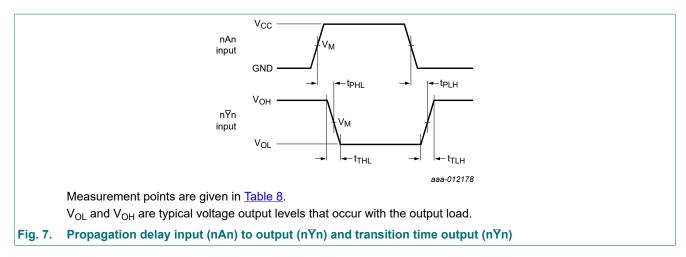
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

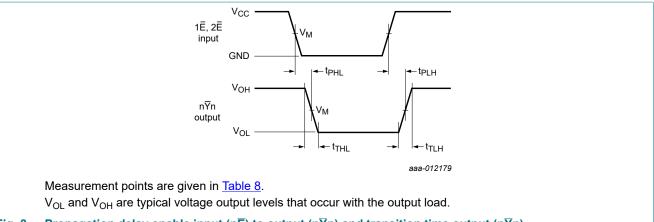
N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

#### 10.1. Waveforms and test circuit



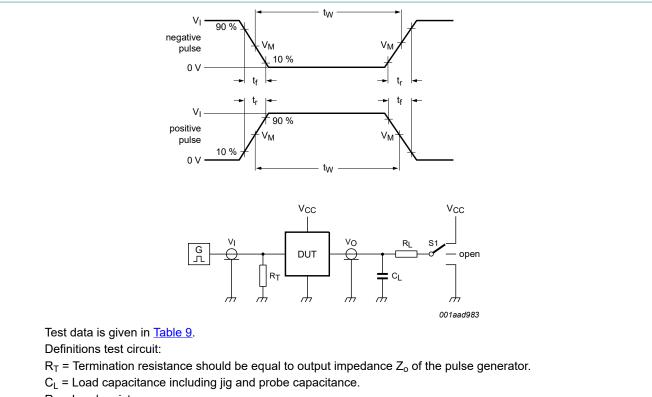
#### Dual 2-to-4 line decoder/demultiplexer



#### Fig. 8. Propagation delay enable input $(n\overline{E})$ to output $(n\overline{Y}n)$ and transition time output $(n\overline{Y}n)$

#### Table 8. Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC139	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT139	1.3 V	1.3 V



- R<sub>L</sub> = Load resistance.
- S1 = Test selection switch.

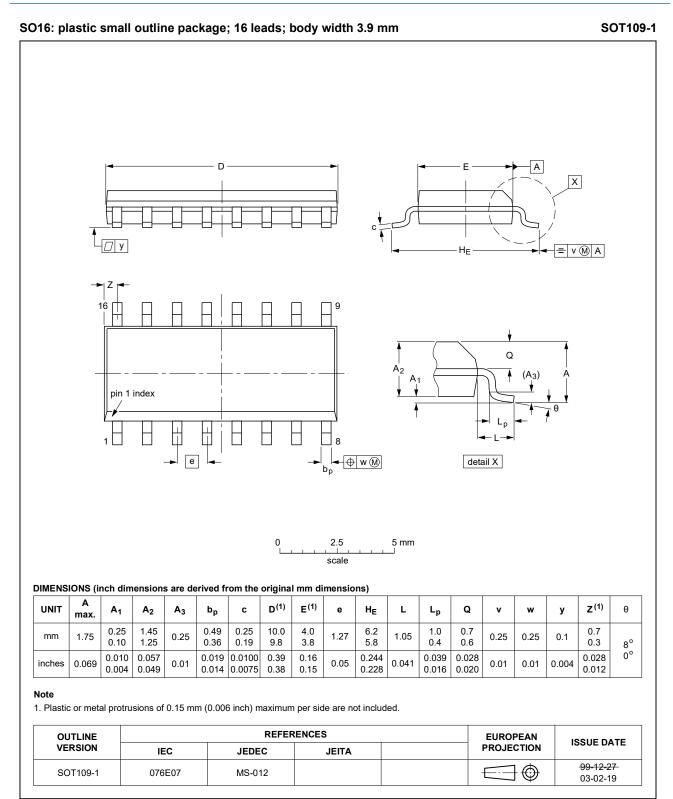
#### Fig. 9. Test circuit for measuring switching times

#### Table 9. Test data

Туре	Input		Load		S1 position			
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
74HC139	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	
74HCT139	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	

74HC\_HCT139

### 11. Package outline



#### Fig. 10. Package outline SOT109-1 (SO16)

74HC\_HCT139

#### Dual 2-to-4 line decoder/demultiplexer

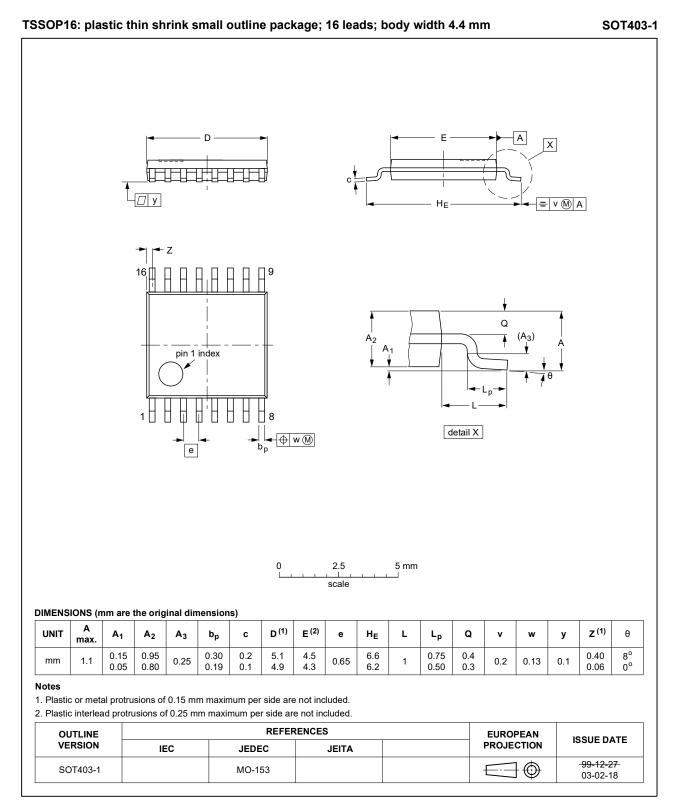


Fig. 11. Package outline SOT403-1 (TSSOP16)

<sup>74</sup>HC\_HCT139

# 12. Abbreviations

Table 10. Abbreviations				
Acronym	Description			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
ММ	Machine Model			
TTL	Transistor-Transistor Logic			

# 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT139 v.5	20210114	Product data sheet	-	74HC_HCT139 v.4	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC139DB and 74HCT139DB (SOT338-1 / SSOP16) removed.</li> <li><u>Section 7</u>: Derating values for P<sub>tot</sub> total power dissipation have been updated.</li> </ul>				
74HC_HCT139 v.4	20151211	Product data sheet	-	74HC_HCT139 v.3	
Modifications:	Type numbers 74HC139N and 74HCT139N (SOT38-4) removed.				
74HC_HCT139 v.3	20140328	Product data sheet	-	74HC_HCT139 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74HC_HCT139_CNV v.2	19930927	Product specification	-	-	

# 14. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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