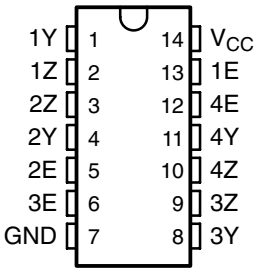
- **Qualified for Automotive Applications**
- **Low ON Resistance**
  – 25 Ω Typical (V_{CC} = 4.5 V)
- **Fast Switching and Propagation Speeds**
- **Low OFF Leakage Current**
- **Wide Operating Temperature Range: –40°C to 125°C**
- **Direct LSTTL Input Logic Compatibility: V_{IL} = 0.8 V Max, V_{IH} = 2 V Min**
- **CMOS Input Compatibility: $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}**

M OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD74HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operation speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear ON resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER§	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HCT4066QM96Q1	HCT4066Q
	TSSOP – PW	Reel of 2000	CD74HCT4066QPWRQ1	HK4066Q

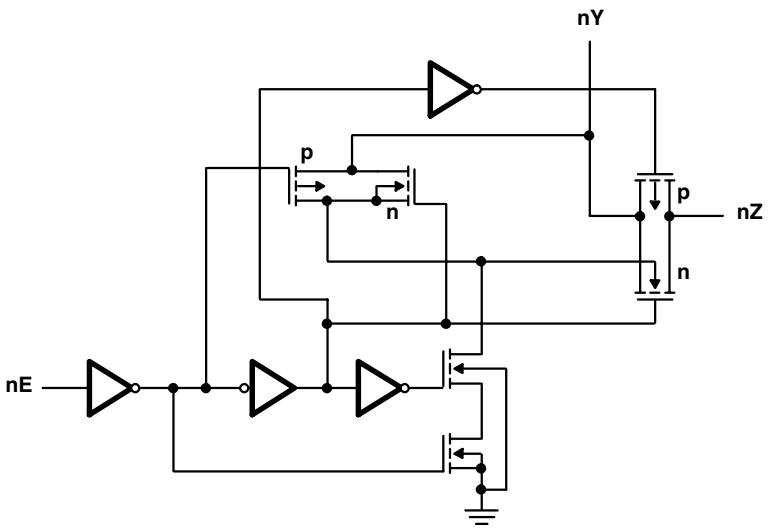
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ The suffix 96 denotes tape and reel.

FUNCTION TABLE

INPUT nE	SWITCH
L	Off
H	On

H = High level
L = Low level

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to +7 V
Input clamp current, I_{IK} ($V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . . ±20 mA
Switch current, I_O (see Note 2) ($V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Output source or sink current per output pin, I_O ($V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 86°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs (terminals 1, 4, 8, and 11), the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{on} values shown in the electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into terminals 2, 3, 9, and 10.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 4.5 V	0	500	ns
T_A	Operating free-air temperature		–40	125	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_I	V_{CC}	T_A = 25°C			T_A = –40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I_{IL}	Any control		V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{IZ}	V_{IS} = V_{CC} or GND		V_{IL}	5.5 V			±0.1		±1	µA
r_{on}	I_O = 1 mA, See Figure 7	V_{IS} = V_{CC} or GND	V_{CC}	4.5 V		25	80		128	Ω
		V_{IS} = V_{CC} to GND	V_{CC}	4.5 V		35	95		142	
Δr_{on}	Between any two switches		V_{CC}	4.5 V		1				Ω
I_{CC}			V_{CC} or GND	5.5 V			2		40	µA
ΔI_{CC}	Per input pin: 1 unit load, See Note 5		V_{CC} – 2.1 V	4.5 V to 5.5 V		100	360		490	µA
C_I	Control inputs						10		10	pF

NOTE 5: For dual-supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

INPUT	UNIT LOADS†
All	1

† Unit load is ΔI_{CC} limit specified in the electrical characteristics table, e.g., 360 µA max at 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = –40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	Y or Z	Z or Y	C_L = 15 pF	5 V		4				ns
			C_L = 50 pF	4.5 V			12		18	
t_{en}	E	Y or Z	C_L = 15 pF	5 V		9				ns
			C_L = 50 pF	4.5 V			24		36	
t_{dis}	E	Y or Z	C_L = 15 pF	5 V		14				ns
			C_L = 50 pF	4.5 V			35		53	

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 6)	38	pF

NOTE 6: C_{pd} is used to determine the dynamic power consumption (P_D), per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_I) + \Sigma (C_L + C_S) \times V_{CC}^2 \times f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

analog channel characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
f_{max}	Switch frequency response bandwidth at –3 dB	See Figure 2 and Figure 8 and Notes 7 and 8	4.5 V	200	MHz
	Crosstalk between any two switches	See Figure 1 and Figure 9 and Notes 8 and 9	4.5 V	–72	dB
	Total harmonic distortion	See Figure 3, 1 kHz, V_{IS} = 4 V_{P-P}	4.5 V	0.023	%
	Control to switch feedthrough noise	See Figure 4	4.5 V	130	mV
	Switch OFF signal feedthrough	See Figure 5 and Figure 9 and Notes 8 and 9	4.5 V	–72	dB
C_S	Switch input capacitance			5	pF

NOTES: 7. Adjust input voltage to obtain 0 dBm at output, f = 1 MHz.
8. V_{IS} is centered at $V_{CC}/2$.
9. Adjust input for 0 dBm at V_{IS}.

PARAMETER MEASUREMENT INFORMATION

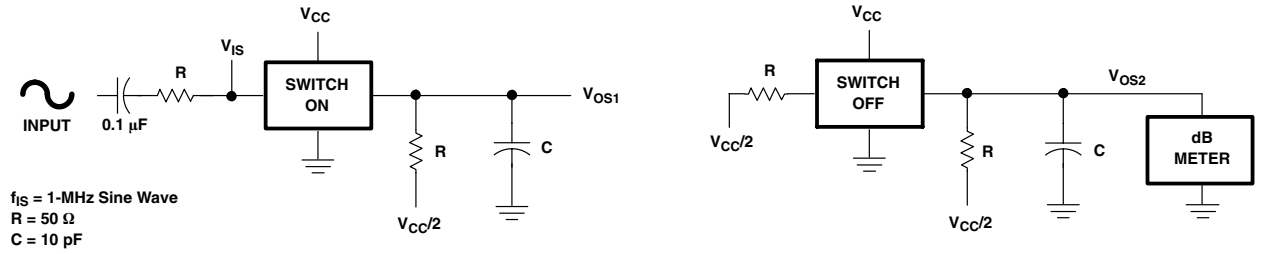


Figure 1. Crosstalk Between Two Switches Test Circuit

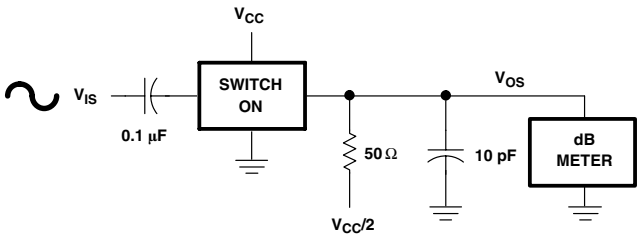


Figure 2. Frequency-Response Test Circuit

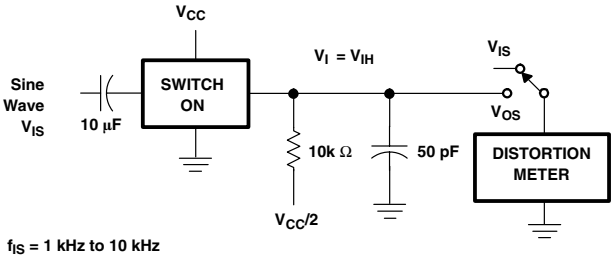


Figure 3. Total Harmonic Distortion Test Circuit

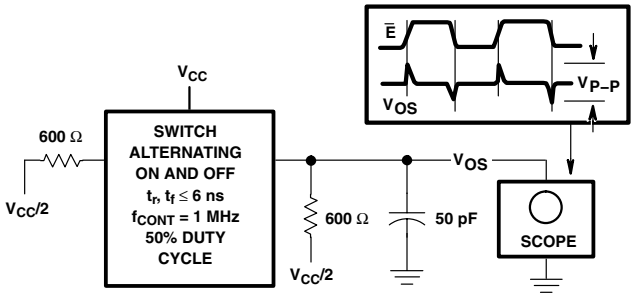


Figure 4. Control-to-Switch Feedthrough Noise Test Circuit

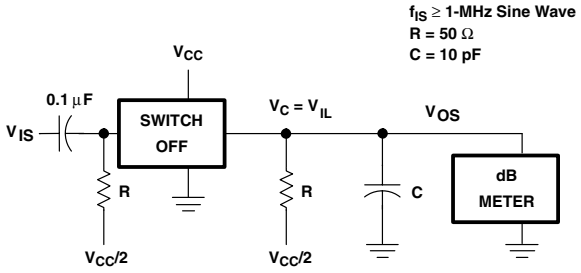
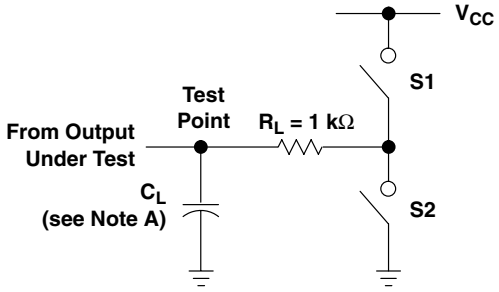


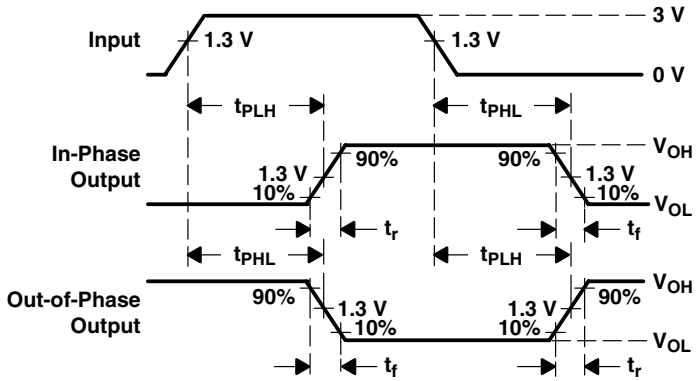
Figure 5. Switch OFF Signal Feedthrough Test Circuit

PARAMETER MEASUREMENT INFORMATION

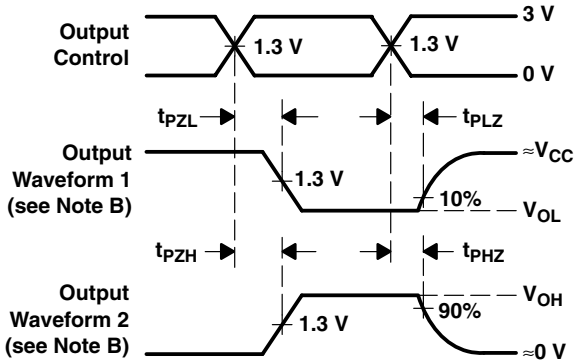


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

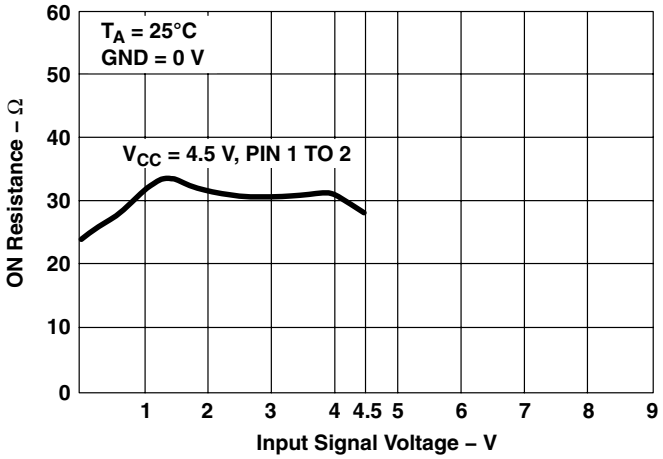


Figure 7. Typical ON Resistance vs Input Signal Voltage

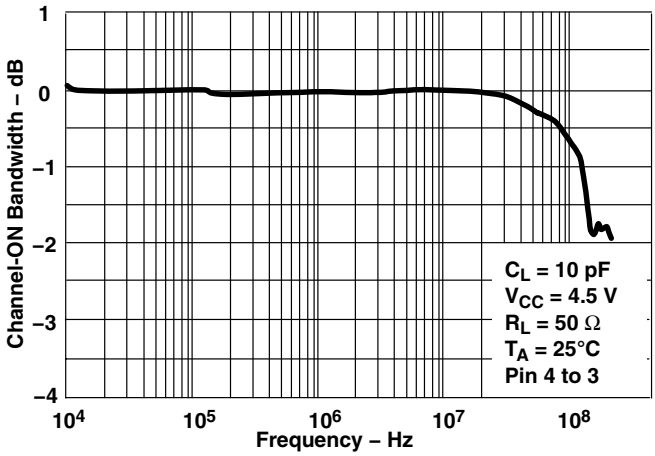


Figure 8. Switch Frequency Response, V_{CC} = 4.5 V

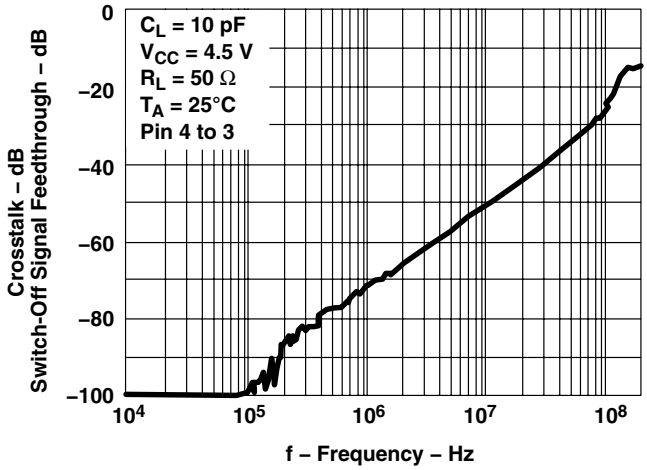


Figure 9. Switch-OFF Signal Feedthrough and Crosstalk vs Frequency, V_{CC} = 4.5 V

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4066QM96Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4066Q	Samples
CD74HCT4066QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HK4066Q	Samples
D24066QM96G4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4066Q	Samples
HCT4066QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HK4066Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD74HCT4066-Q1 :

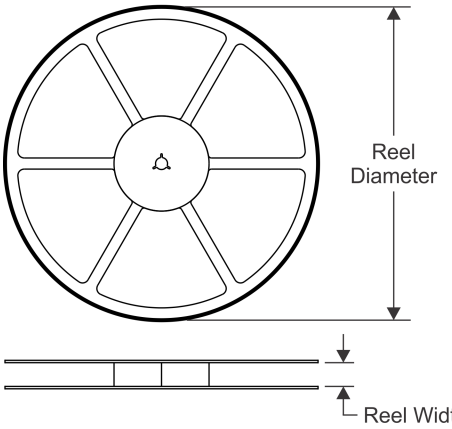
- Catalog: CD74HCT4066

NOTE: Qualified Version Definitions:

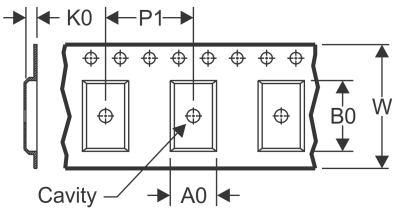
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

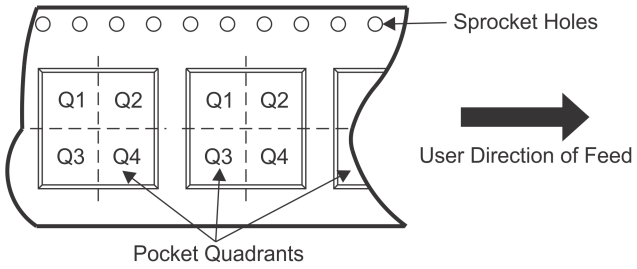


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

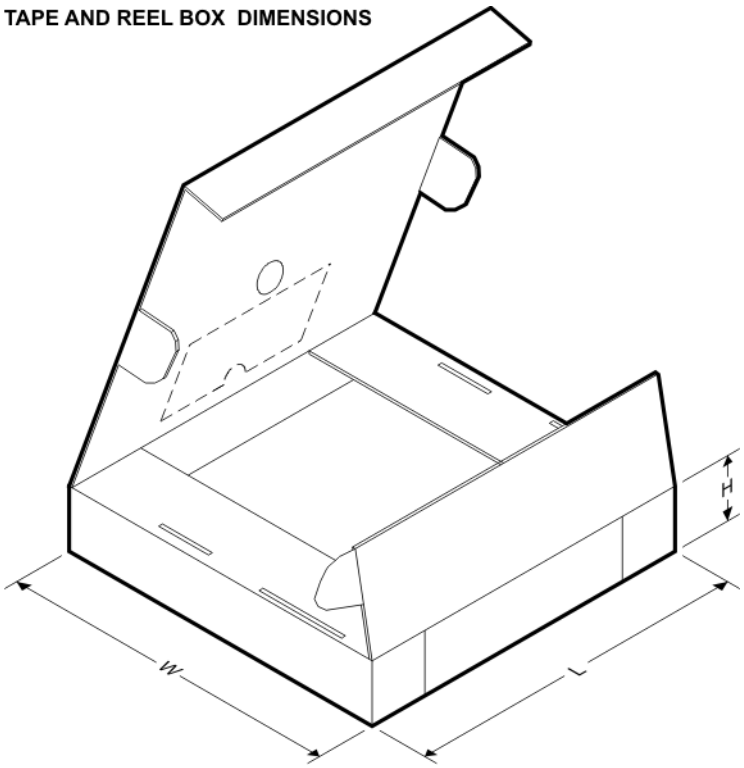
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT4066QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
HCT4066QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

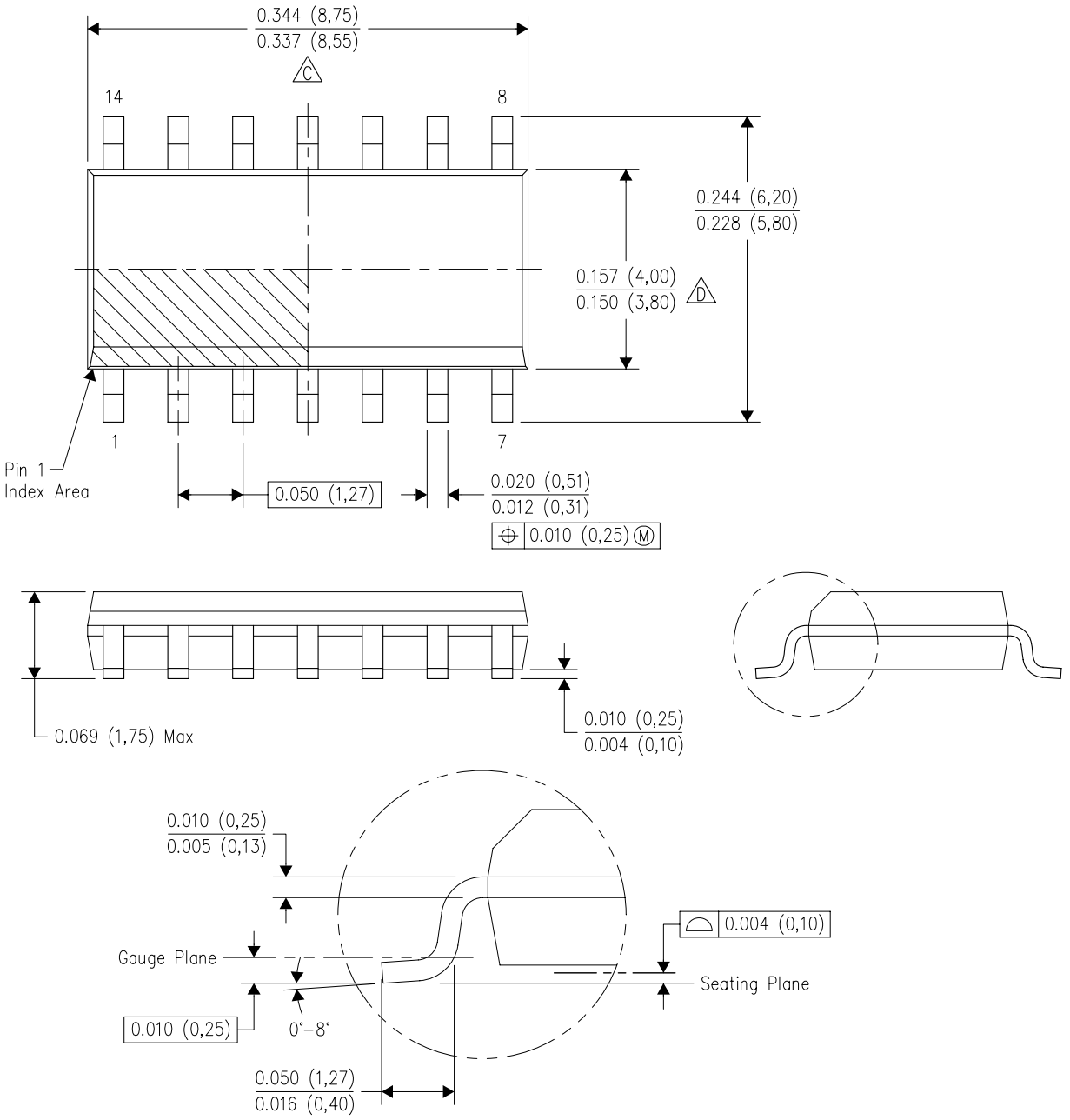
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT4066QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
HCT4066QPWRG4Q1	TSSOP	PW	14	2000	853.0	449.0	35.0

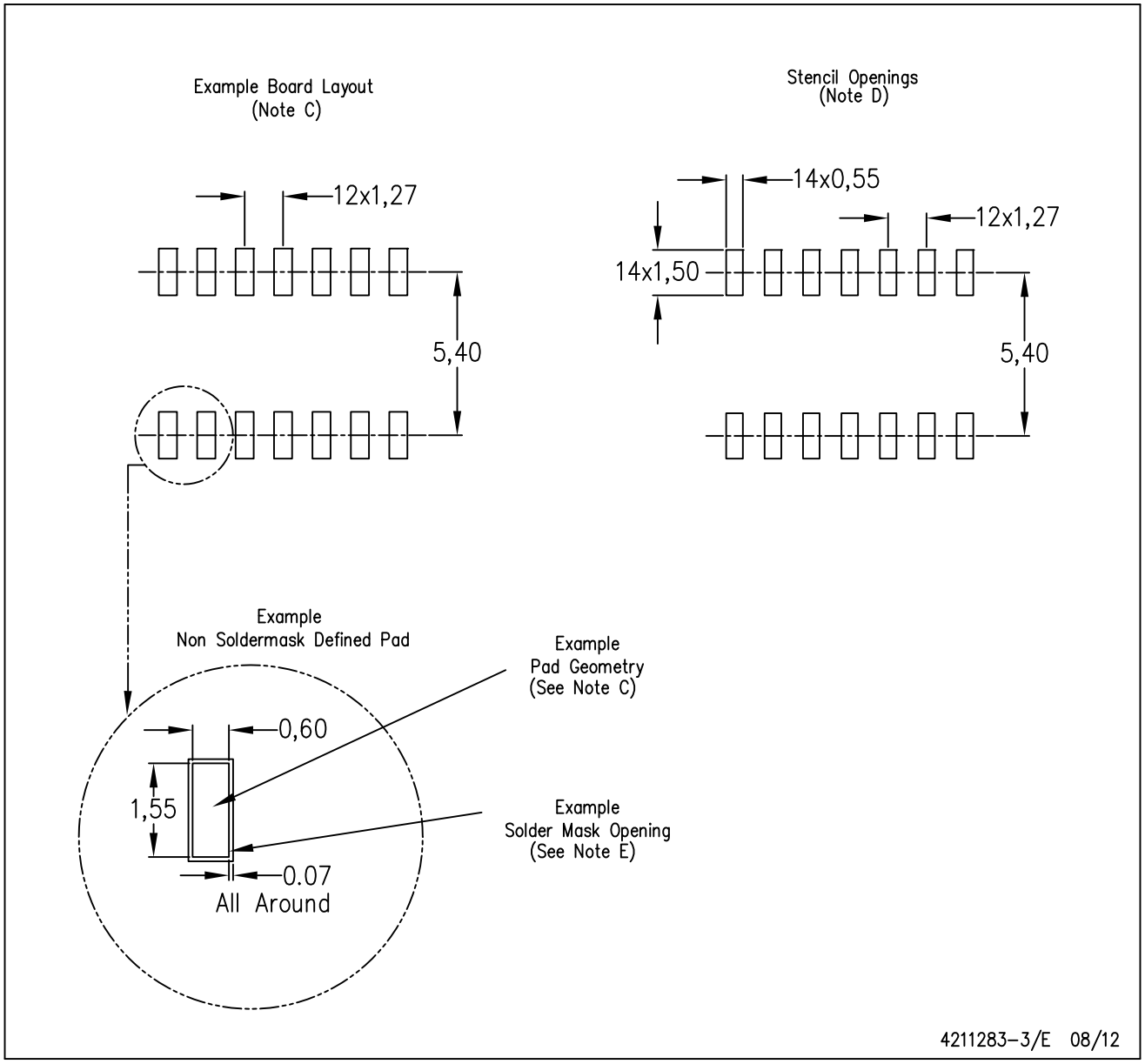
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

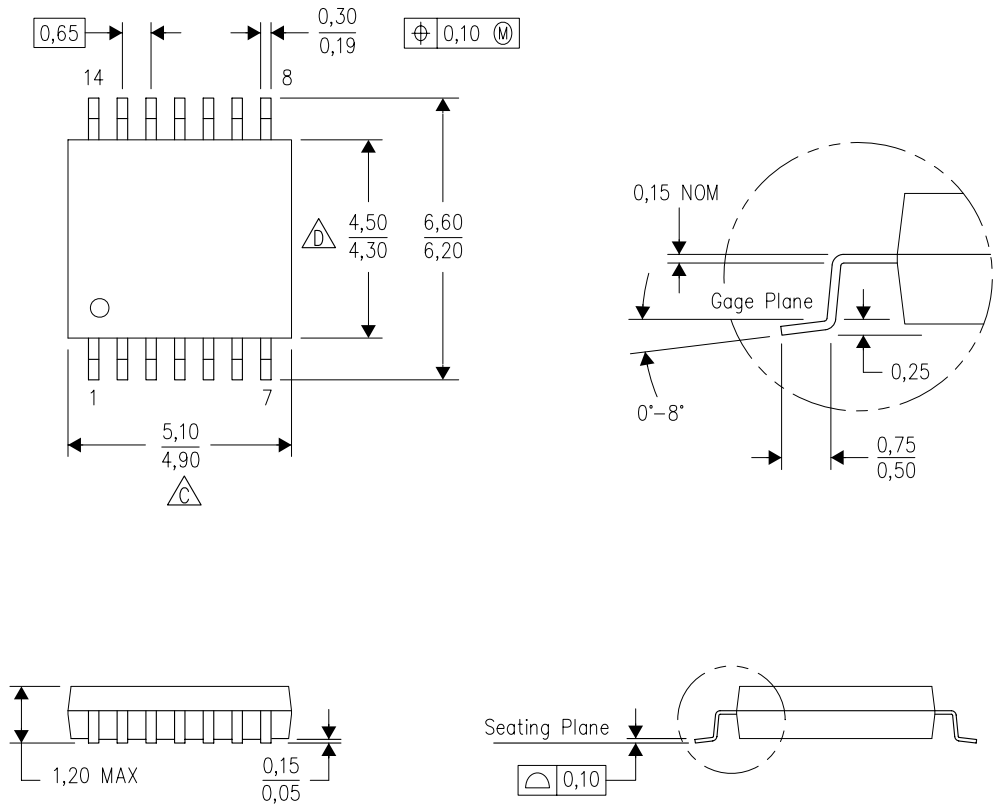
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

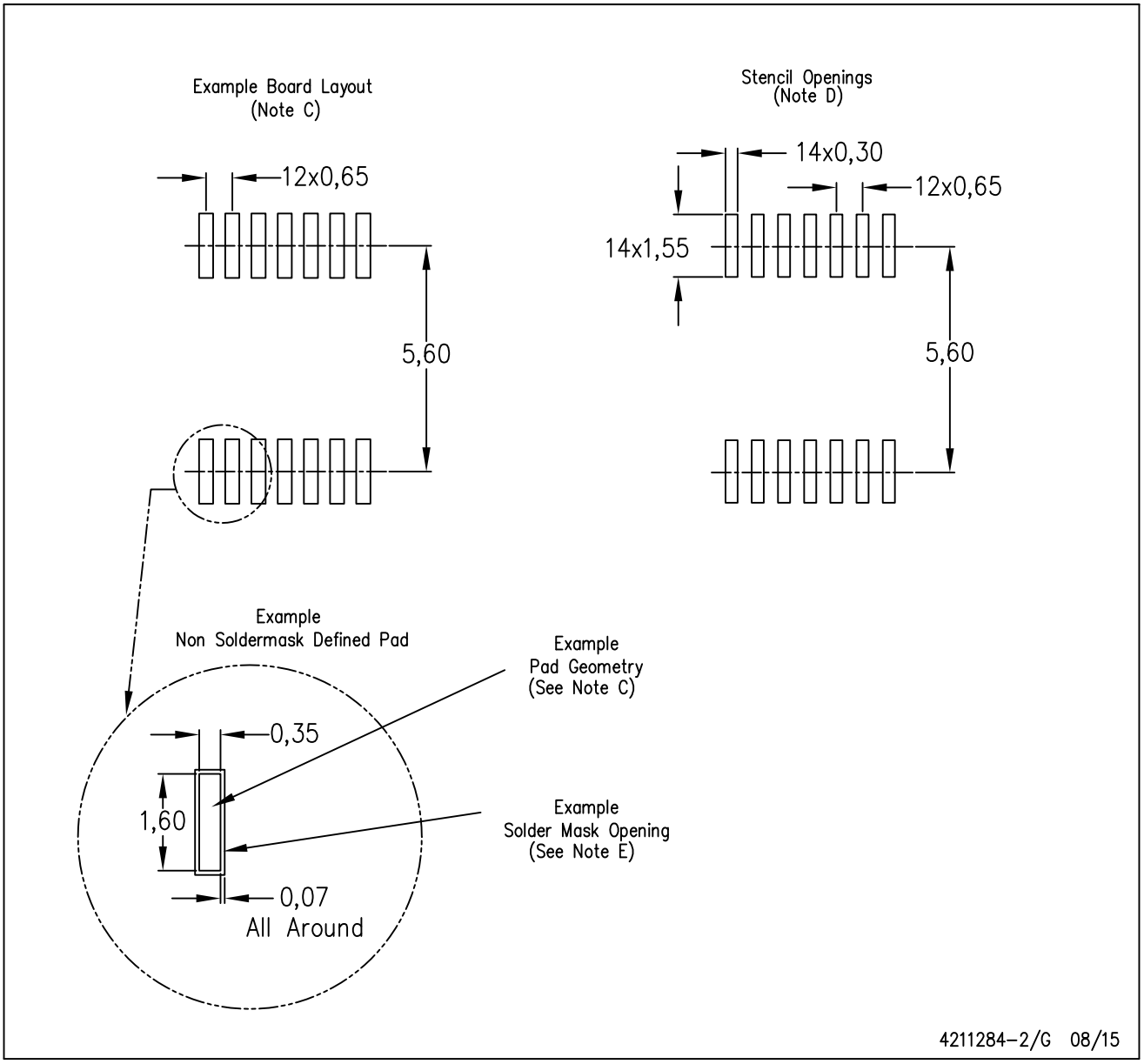
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
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B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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